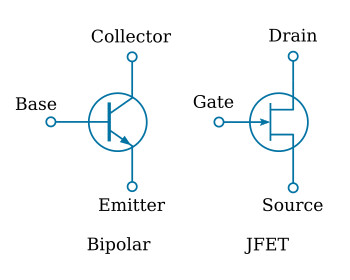
**Electronic Circuit**

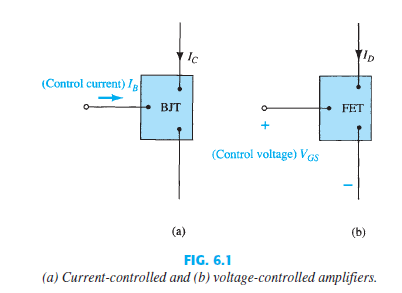
**Lecture 7 ( Week)**

**Field effect transistor and MOSFET**

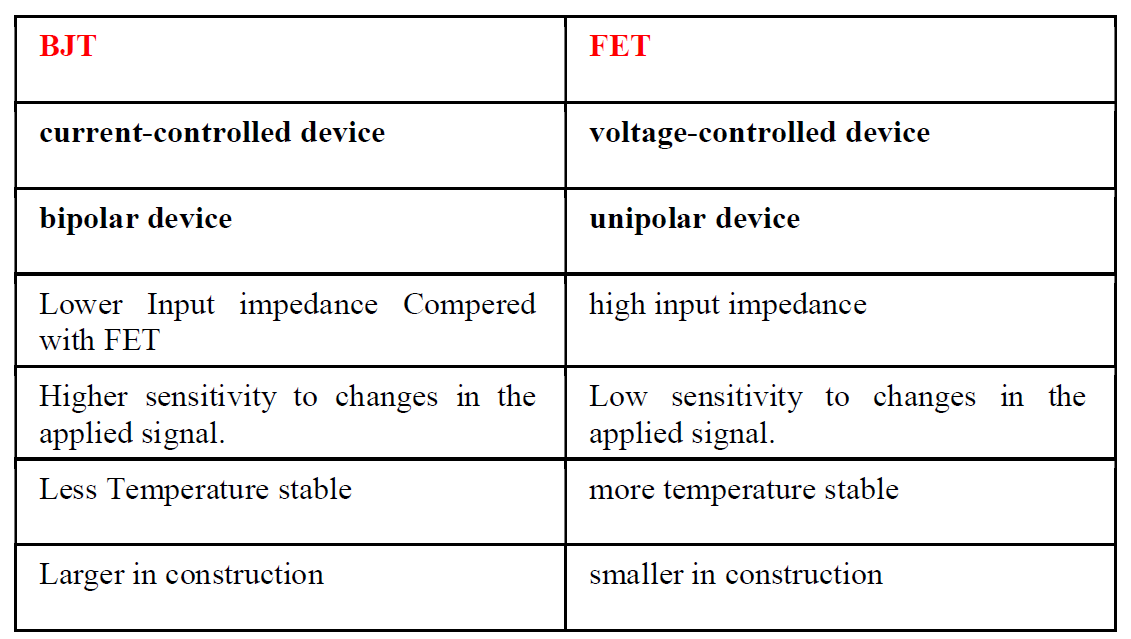


6.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor. Although there are important differences between the two types of devices, there are also many similarities, which will be pointed out in the sections to follow. The primary difference between the two types of transistors is the fact that: The BJT transistor is a current-controlled device as depicted in Fig. 6.1, whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b.



هذا الشكل من الترانزستور(ترانزستور تأثير المجال) هو الاحدث والاكثر استخدما ويعمل بنوع واحد من حاملات الشحنة . وكما لاحظنا سابقا بان تيار الجامع تم التحكم به عن طريق تيار القاعدة فان تيار الساحب يتم التحكم به عن طريق البوابة. سندرس نوعان من الترانزستور الاول هو ترانزستور تاثير المجال ذو الوصلة والثاني هو ترانزستور تاثير المجال ذو الاوكسيد المعدني. مع ملاحظة ان هذا النوع من الترانزستور يتحكم بالتيار من خلال فرق الجهد.



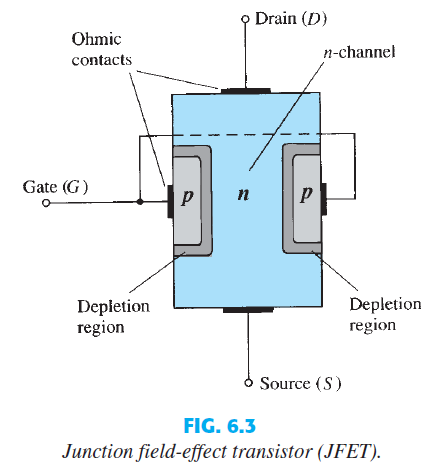
6.2. CONSTRUCTION AND CHARACTERISTICS OF JFETs

1-the JFET (junction field-effect transistor ) is a three-terminal device with one terminal capable of controlling the current between the other two

2-the major part of the structure is the n -type material, which forms the channel between the embedded layers of p -type material

3-the drain and the source are connected to the ends of the n -type channel and the gate to the two layers of p -type material

في هذا النوع من الترانزستور هناك منطقتان للشحنات الموجبة تخترق المنطقة السالبة لتكون القناة وكلا المنطقتين مربوطة الى طرف البوابة. يلاحظ ان الربط يكون بحالة الانحياز الامامي بالنسبة للقناة وانحياز عكسي على البوابة حيث يعمل الانحياز العكسي المطبق على البوابة على تضييق القناة والتحكم بكمية التيار المار من الالكترونات



for the JFET transistor can defined the following

1-The input circuit ( gate to source) of a Jfet is reverse bias, that means the device has high input impedance

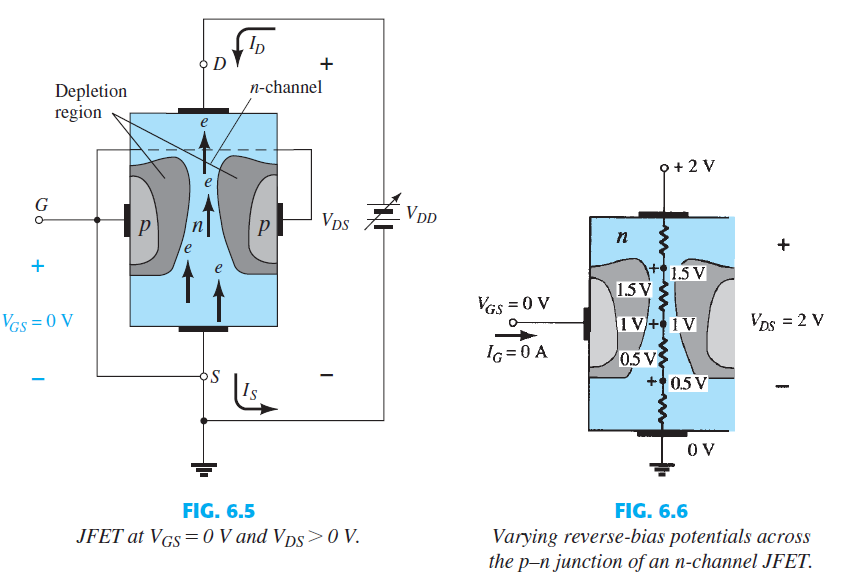
2-the drain is so biased with respect to the source , ID flows from source to drain

3- in all Jfet ID=IS When:

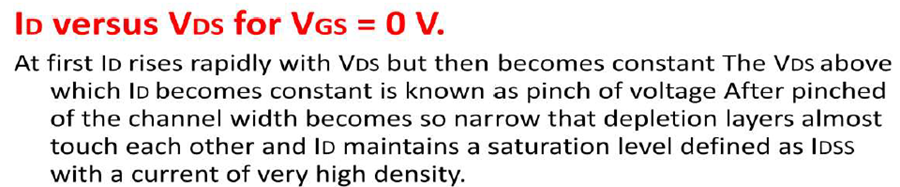
***VGS*** = **0V, *VDS* Some Positive Value**



عندما يكون فرق الجهد على البوابة يساوي صفر تعبر الالكترونات عن طريق القناة من المصدر الى الساحب ويكون تيار الساحب يساوي تيار المصدر لكن عند تطبيق فرق جهد معين على البوابة تبدا القناة تضيق مما يؤثر على كمية التيار المار خلال القناة.



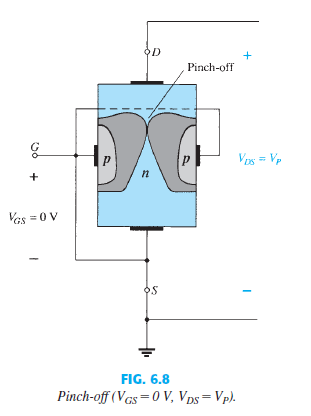
The current ID will establish the voltage levels through the channel the greater the applied reverse bias in p type material , the wider is the depletion region.



**Pinch-off (VGS = 0 V, VDS = VP).**

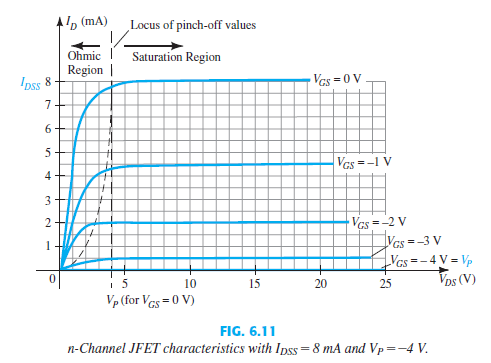
IDSS is the maximum drain current for a JFET and is defined by the conditions VGS = 0 V and VDS > VP.

في البدء يزداد تيار الساحب مع زيادة الفولتية المطبقة بين الساحب والمصدر لكن بعدها يثبت التيار وعندها تسمى الفولتية بفولتية غلق القناة. بعد هذه الفولتية تكون القناة ضيقة جدا. وعند زيادة الفولتية فوق فولتية غلق القناة ينتج تيار يسمى IDSS وهو اعلى تيار ينتجه الترانزستور عندما تكون الفولتية تساوي صفر



**When VGS <0 V**

VGS is The voltage from gate to source a negative voltage is applied between G and S



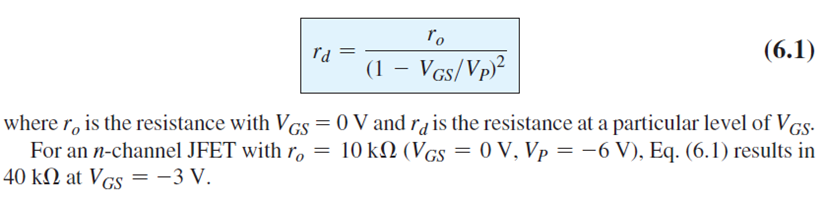
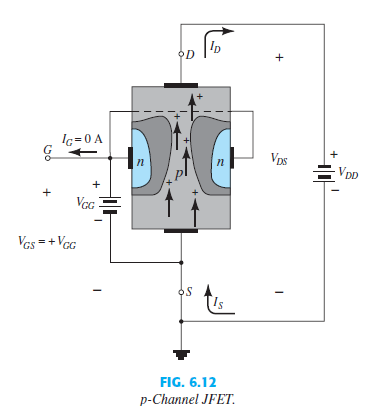
المخطط يوضح التحكم بتيار الساحب عن طريق فولتية البوابة الى المصدر حيث يكون التيار اعلى ما يمكن في حالة الفولتية تساوي صفر ثم تتراجع قيمة التيار مع زيادة فرق الجهد العكسي المطبق على البوابة.

The resulting saturation level for ID has been reduced and in fact will continue to decrease as VGS is made more and more negative and a pinch-off voltage continues to drop as VGS becomes more and more negative and the device has been (Turned Off) In summary:

The level of VGS that results in ID = 0 mA is defined by VGS =VP, with VP being a negative voltage for n channel devices and a positive voltage for p-channel JFETs.

**Voltage-Controlled Resistor**

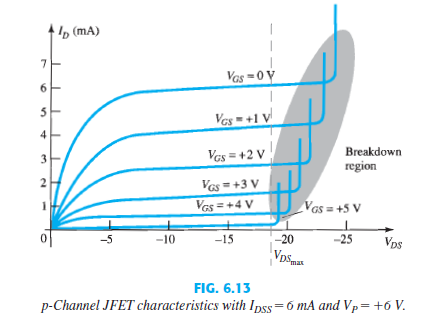
The region to the left of the pinch-off locus of Fig. 6.11 is referred to as the ohmic or voltage-controlled resistance region. possibly for an automatic gain control system whose resistance is controlled by the applied gate-to-source voltage



p -Channel Devices

The defined current directions are reversed Applied voltage is positive

voltages from gate to source and the double-subscript notation for VDS will result in negative voltages for VDS



Summary

A- The maximum current is defined as IDSS and occurs when VGS=0 V and VDS≥ VP

B- For gate-to-source voltages VGS is less than (more negative than) the pinchoff

level, the drain current is 0 A ( ID 0 A )

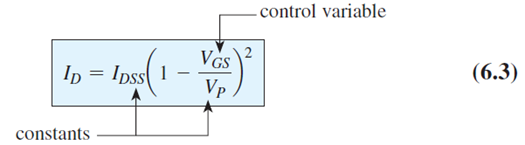
C- For all levels of VGS between 0 V and the pinch-off level, the current ID will

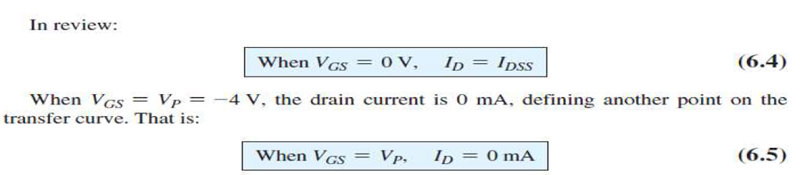
range between IDSS and 0 A, respectively.

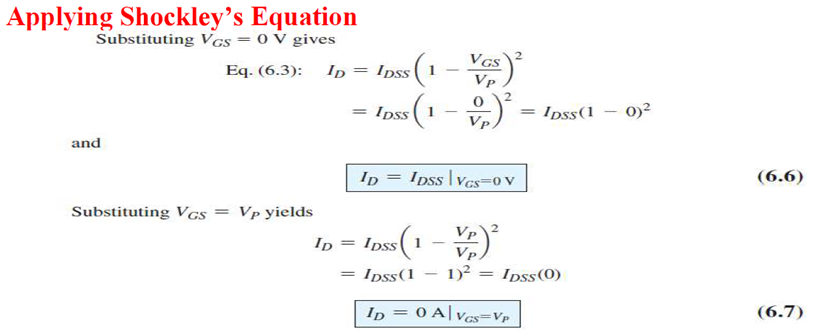
D- A similar list can be developed for p-channel JFETs.

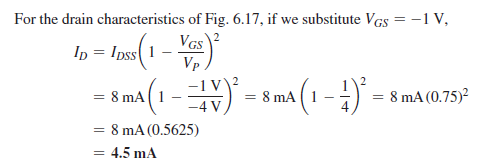
**6.3 TRANSFER CHARACTERISTICS**

The relationship between ID and VGS is defined by Shockley’s equation:

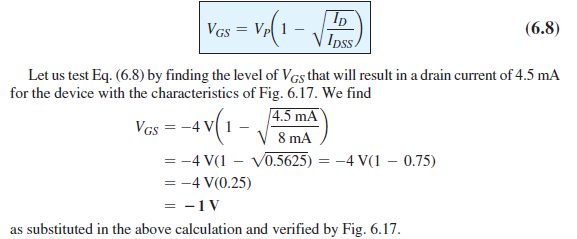


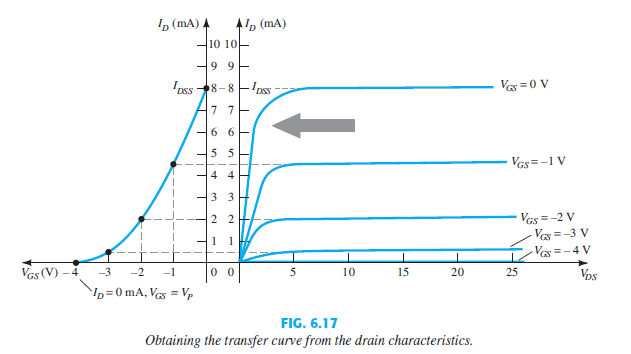






By using basic algebra we can obtain [from Eq. (6.3)] an equation for the resulting level of VGS for a given level of ID. The derivation is quite straightforward and results in equation (6.8).

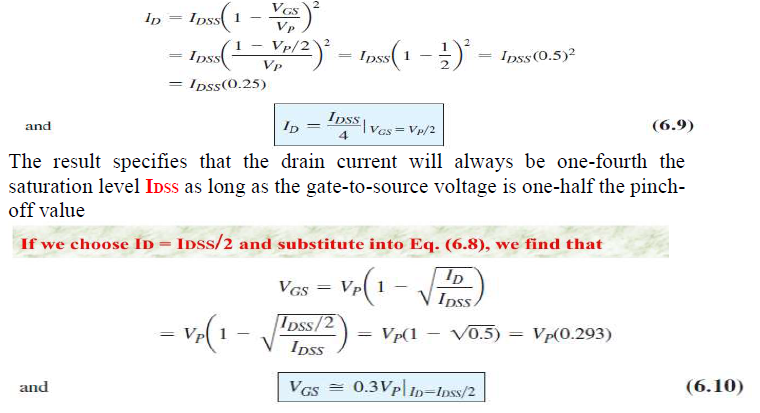


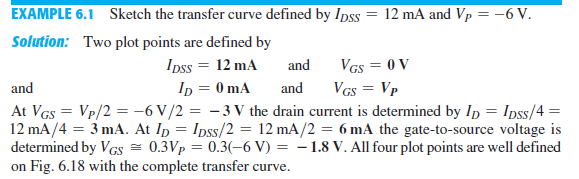


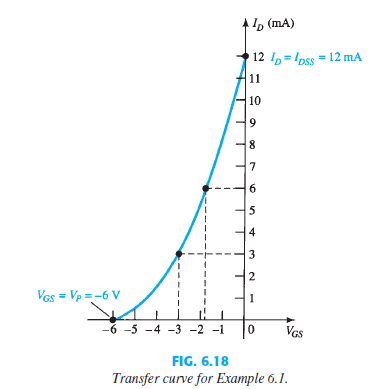
**Shorthand Method:**

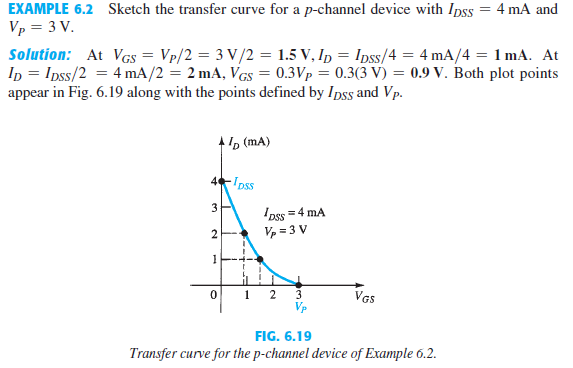
If we specify VGS to be one-half the pinch-off value VP, the resulting level of

ID will be the following, as determined by Shockley’s equation:









**DEPLETION-TYPE MOSFET:**

The name MOSFET stands for metal oxide semiconductor field –effect transistor

Basic Construction:

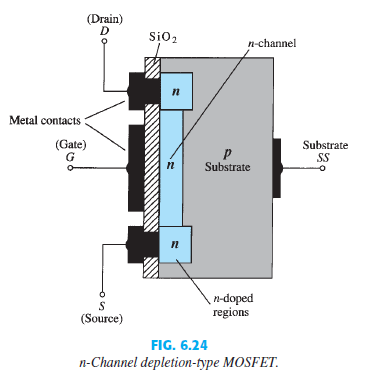
1-A slab of p -type material is formed from a silicon base and is referred to as the substrate.

2- In some cases the substrate is internally connected to the source terminal

3-The source and drain terminals are connected through metallic contacts to n -doped regions linked by an n -channel as shown in the figure

4-The gate is also connected to a metal contact surface but remains insulated from the n -channel by a very thin silicon dioxide (SiO2) layer. SiO2 is a type of insulator referred to as a dielectric

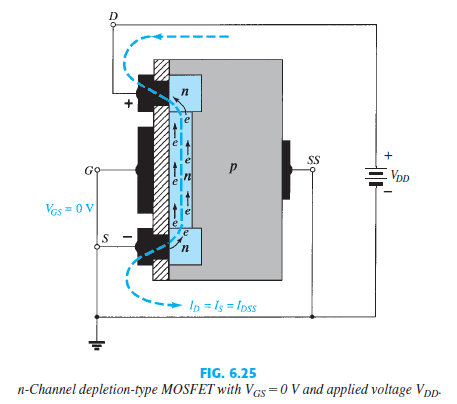
There is no direct electrical connection between the gate terminal and the channel of a MOSFET.



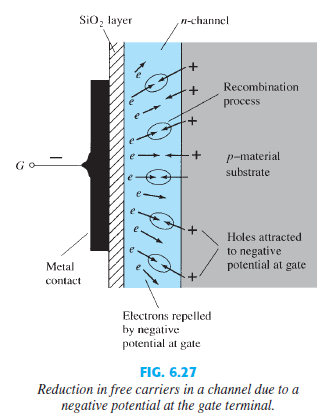
It is the insulating layer of SiO 2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

**Basic Operation and Characteristics:**

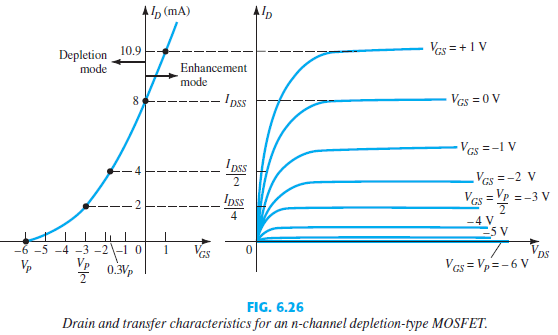
In Fig. 6.25 the gate-to-source voltage is set to 0 V. The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with VGS= 0V continues to be labeled IDSS .

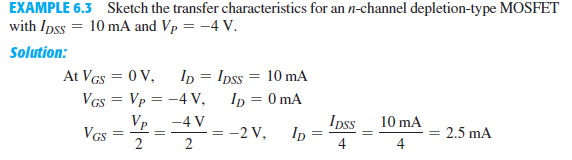


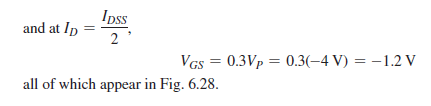
**In Fig. 6.27, VGS is set at a negative voltage such as -1 V**. The negative potential at the gate will tend to pressure electrons toward the p -type substrate (like charges repel) and attract holes from the p -type substrate (opposite charges attract) as shown in Fig. 6.27. Depending on the magnitude of the negative bias established by VGS, The resulting level of drain current is therefore reduced with increasing negative bias for VGS.

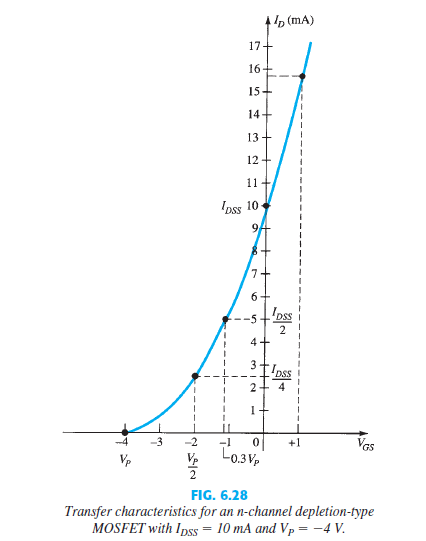


**In Fig. 6.26 for VGS = -1 V, -2 V, and so on**, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET. **For positive values of VGS** , the positive gate will draw additional electrons (free carriers) from the p –type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles As the gate-to-source voltage continues to increase in the positive direction, Fig. 6.26 reveals that the drain current will increase

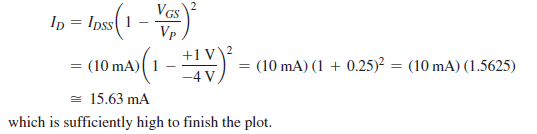




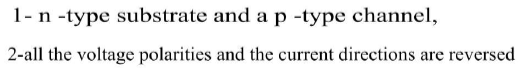


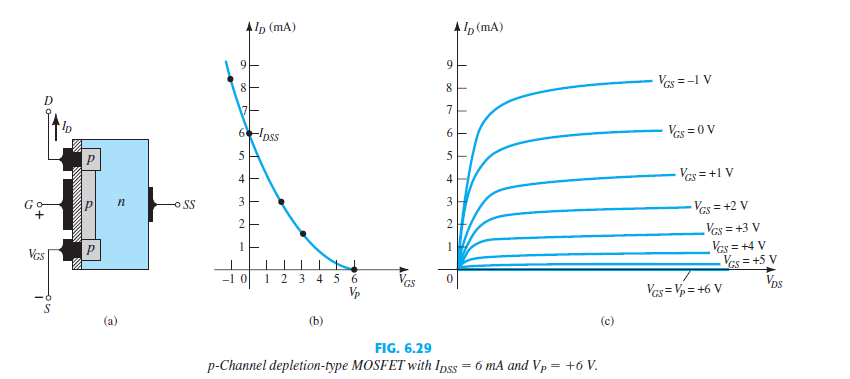


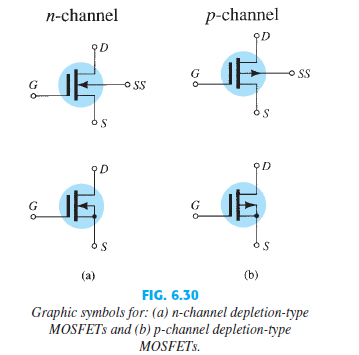
Before plotting the positive region of VGS, keep in mind that ID increases very rapidly with increasing positive values of VGS . In other words, be conservative with the choice of values to be substituted into Shockley’s equation. In this case, we try +1 V as follows:



**p -Channel Depletion-Type MOSFET**







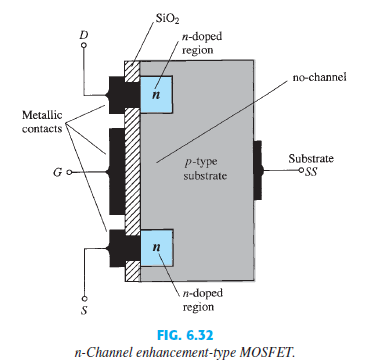
**ENHANCEMENT-TYPE MOSFET:**

**Basic Construction:**

1-p -type material is formed from a silicon base and is again referred to as the substrate

2-the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

3-The drain current is now cut off until the gate-to-source voltage reaches a specific magnitude.



**Basic Operation and Characteristics:**

1. If VGS is set at 0V and a voltage applied between the drain and the source of the device of Fig. 6.32, the absence of an n -channel (with its generous number of free carriers) will result in a current of effectively 0A

2-In Fig.6.33, both VDS and VGS have been set at some positive voltage greater than 0V, establishing the drain and the gate at a positive potential with respect to the source

3-The positive potential at the gate will pressure the holes (since like charges repel) in the p -substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the p -substrate, as shown in the figure. The result is a depletion region near the SiO2 insulating layer void of holes. However, the electrons in the p -substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO2 layer.

4- with VGS increases in magnitude, the concentration of electrons near the SiO2 surface increases until eventually the induced n -type region can support a measurable flow between drain and source

