Al-Mustaqbal University
Department of Medical Instrumentation Techniques Engineering
Class ٢$^{nd}$
Subject: Electronic Circuits
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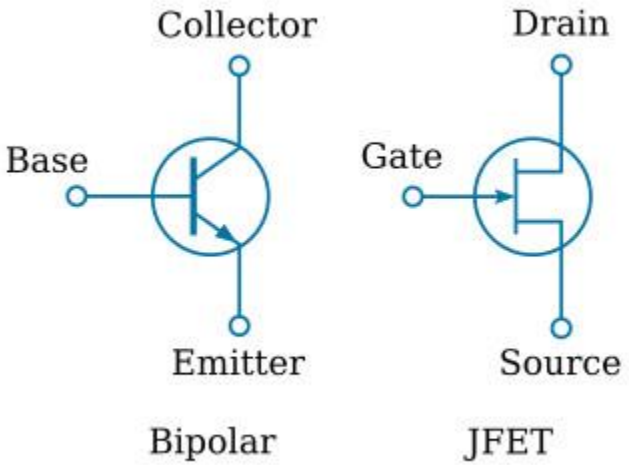
1st term – LEC7-Field effect transistor and MOSFET

# Electronic Circuit

## Lecture 7 (10$^{th}$ Week)

## Field effect transistor and MOSFET

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## ٦.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor. Although there are important differences between the two types of devices, there are also many similarities, which will be pointed out in the sections to follow. The primary difference between the two types of transistors is the fact that: The BJT transistor is a current-controlled device as depicted in Fig. 6.1, whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b.

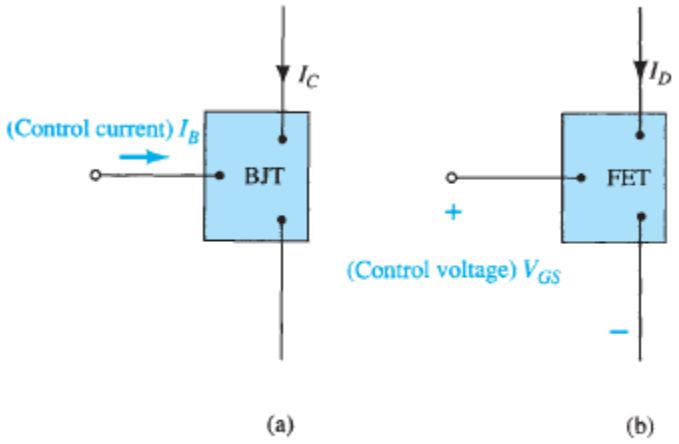



**FIG. 6.1**
*(a) Current-controlled and (b) voltage-controlled amplifiers.*

هذا الشكل من الترانزستور(ترانزستور تأثير المجال) هو الاحدث والاكثر استخدما ويعمل بنوع واحد من حاملات الشحنة . وكما لاحظنا سابقا بان تيار الجامع تم التحكم به عن طريق تيار القاعدة فان تيار الساحب يتم التحكم به عن طريق البوابة. سندرس نوعان من الترانزستور الاول هو ترانزستور تاثير المجال ذو الوصلة والثاني هو ترانزستور تاثير المجال ذو الاوكسيد المعدني. مع ملاحظة ان هذا النوع من الترانزستور يتحكم بالتيار من خلال فرق الجهد.

| BJT | FET |
|---|---|
| **current-controlled device** | **voltage-controlled device** |
| **bipolar device** | **unipolar device** |
| Lower Input impedance Compered with FET | high input impedance |
| Higher sensitivity to changes in the applied signal. | Low sensitivity to changes in the applied signal. |
| Less Temperature stable | more temperature stable |
| Larger in construction | smaller in construction |

## ٦.2. CONSTRUCTION AND CHARACTERISTICS OF JFETs

1-the JFET (junction field-effect transistor ) is a three-terminal device with one terminal capable of controlling the current between the other two

2-the major part of the structure is the n -type material, which forms the channel between the embedded layers of p -type material

3-the drain and the source are connected to the ends of the n -type channel and the gate to the two layers of p -type material

في هذا النوع من الترانزستور هناك منطقتان للشحنات الموجبة تخترق المنطقة السالبة لتكون القناة وكلا المنطقتين مربوطة الى طرف البوابة. يلاحظ ان الربط يكون بحالة الانحياز الامامي بالنسبة للقناة وانحياز عكسي على البوابة حيث يعمل الانحياز العكسي المطبق على البوابة على تضييق القناة والتحكم بكمية التيار المار من الالكترونات

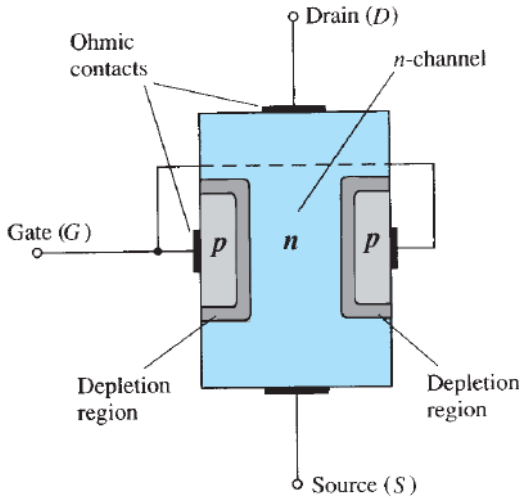



**FIG. 6.3**
*Junction field-effect transistor (JFET).*

for the JFET transistor can defined the following

1-The input circuit ( gate to source) of a Jfet is reverse bias, that means the device has high input impedance

2-the drain is so biased with respect to the source , $I_D$ flows from source to drain

3- in all Jfet $I_D=I_S$ When:

***VGS* = 0V, *VDS* Some Positive Value**

- a positive voltage $V_{DS}$ is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0$ V.

عندما يكون فرق الجهد على البوابة يساوي صفر تعبر الالكترونات عن طريق القناة من المصدر الى الساحب ويكون تيار الساحب يساوي تيار المصدر لكن عند تطبيق فرق جهد معين على البوابة تبدا القناة تضيق مما يؤثر على كمية التيار المار خلال القناة.

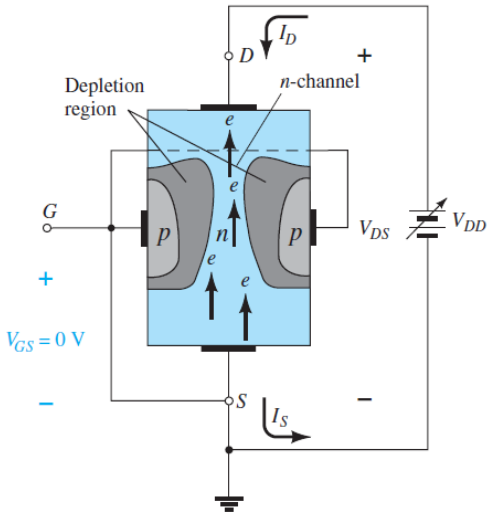



**FIG. 6.5**
*JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.*

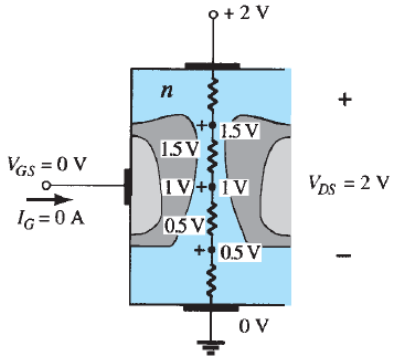



**FIG. 6.6**
*Varying reverse-bias potentials across the p–n junction of an n-channel JFET.*

The current ID will establish the voltage levels through the channel the greater the applied reverse bias in p type material , the wider is the depletion region.

## ID versus VDS for VGS = 0 V.

At first ID rises rapidly with VDS but then becomes constant The VDS above which ID becomes constant is known as pinch of voltage After pinched of the channel width becomes so narrow that depletion layers almost touch each other and ID maintains a saturation level defined as IDSS with a current of very high density.

## Pinch-off (VGS = 0 V, VDS = VP).

IDSS is the maximum drain current for a JFET and is defined by the conditions VGS = 0 V and VDS > VP.

في البدء يزداد تيار الساحب مع زيادة الفولتية المطبقة بين الساحب والمصدر لكن بعدها يثبت التيار وعندها تسمى الفولتية بفولتية غلق القناة. بعد هذه الفولتية تكون القناة ضيقة جدا. وعند زيادة الفولتية فوق فولتية غلق القناة ينتج تيار يسمى IDSS وهو اعلى تيار ينتجه الترانزستور عندما تكون الفولتية تساوي صفر

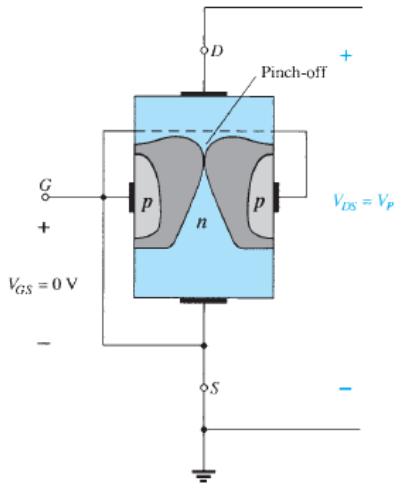



**FIG. 6.8**
*Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).*

## When VGS <0 V

VGS is The voltage from gate to source a negative voltage is applied between G and S

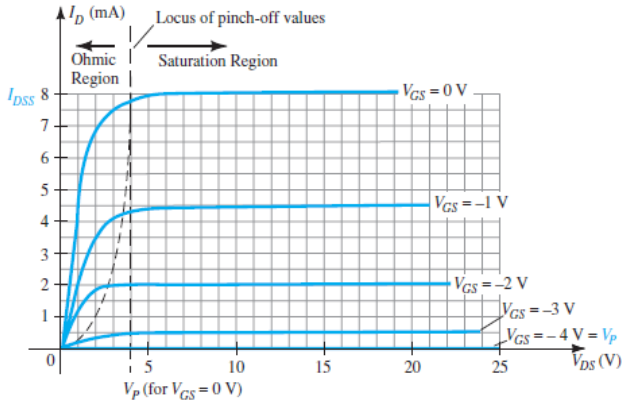



**FIG. 6.11**
*n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.*

المخطط يوضح التحكم بتيار الساحب عن طريق فولتية البوابة الى المصدر حيث يكون التيار اعلى ما يمكن في حالة الفولتية تساوي صفر ثم تتراجع قيمة التيار مع زيادة فرق الجهد العكسي المطبق على البوابة.

The resulting saturation level for ID has been reduced and in fact will continue to decrease as VGS is made more and more negative and a pinch-off voltage continues to drop as VGS becomes more and more negative and the device has been (Turned Off) In summary:

The level of VGS that results in ID = 0 mA is defined by VGS =VP, with VP being a negative voltage for n channel devices and a positive voltage for p-channel JFETs.

## Voltage-Controlled Resistor

The region to the left of the pinch-off locus of Fig. 6.11 is referred to as the ohmic or voltage-controlled resistance region. possibly for an automatic gain control system whose resistance is controlled by the applied gate-to-source voltage

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2} \qquad (6.1)$$

where $r_o$ is the resistance with $V_{GS} = 0$ V and $r_d$ is the resistance at a particular level of $V_{GS}$.
For an $n$-channel JFET with $r_o = 10\ \text{k}\Omega$ ($V_{GS} = 0$ V, $V_P = -6$ V), Eq. (6.1) results in 40 kΩ at $V_{GS} = -3$ V.

p -Channel Devices

The defined current directions are reversed Applied voltage is positive

voltages from gate to source and the double-subscript notation for VDS will result in negative voltages for VDS

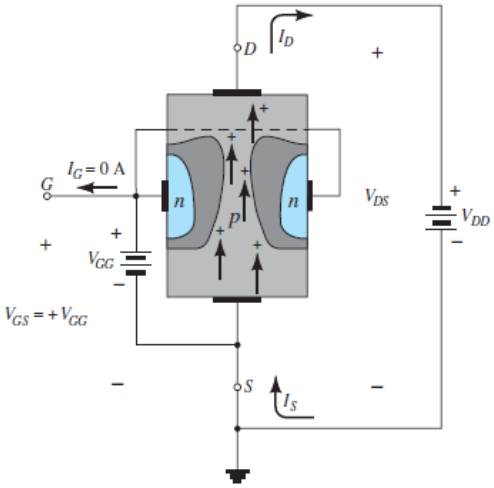



FIG. 6.12
*p-Channel JFET.*

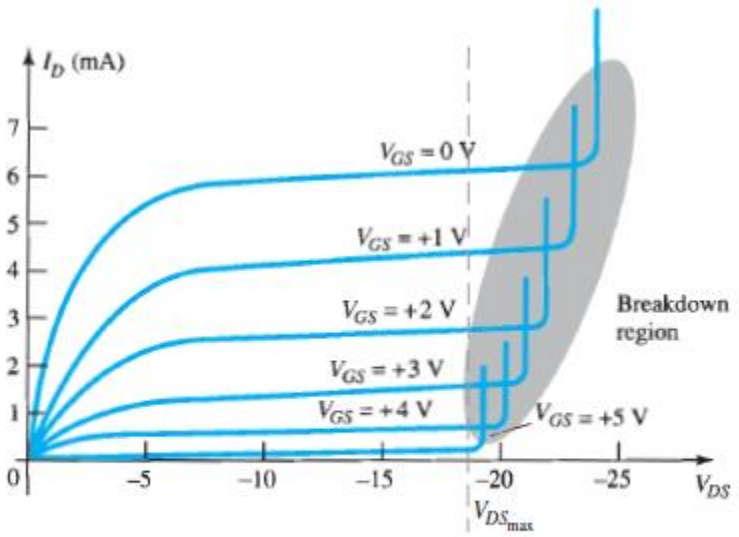



**FIG. 6.13**
*p-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.*

## Summary

A- The maximum current is defined as IDSS and occurs when VGS=0 V and VDS≥ VP

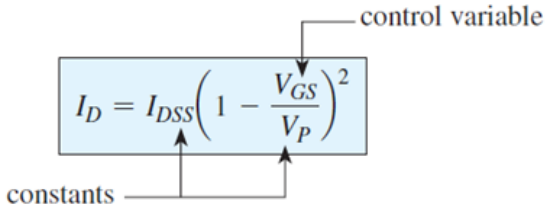
B- For gate-to-source voltages VGS is less than (more negative than) the pinchoff level, the drain current is 0 A ( ID 0 A )

C- For all levels of VGS between 0 V and the pinch-off level, the current ID will range between IDSS and 0 A, respectively.

D- A similar list can be developed for p-channel JFETs.

## 6.3 TRANSFER CHARACTERISTICS

The relationship between $I_D$ and $V_{GS}$ is defined by Shockley's equation:




$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (6.3)$$

In review:

$$\text{When } V_{GS} = 0\text{ V}, \quad I_D = I_{DSS} \qquad (6.4)$$

When $V_{GS} = V_P = -4$ V, the drain current is 0 mA, defining another point on the transfer curve. That is:

$$\text{When } V_{GS} = V_P, \quad I_D = 0\text{ mA} \qquad (6.5)$$

### Applying Shockley's Equation

Substituting $V_{GS} = 0$ V gives

$$\text{Eq. (6.3):} \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}(1 - 0)^2$$

and

$$I_D = I_{DSS}\,|_{V_{GS}=0\text{ V}} \qquad (6.6)$$

Substituting $V_{GS} = V_P$ yields

$$I_D = I_{DSS}\left(1 - \frac{V_P}{V_P}\right)^2 = I_{DSS}(1 - 1)^2 = I_{DSS}(0)$$

$$I_D = 0\text{ A}\,|_{V_{GS}=V_P} \qquad (6.7)$$

For the drain characteristics of Fig. 6.17, if we substitute $V_{GS} = -1$ V,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 8\text{ mA}\left(1 - \frac{-1\text{ V}}{-4\text{ V}}\right)^2 = 8\text{ mA}\left(1 - \frac{1}{4}\right)^2 = 8\text{ mA}\,(0.75)^2$$
$$= 8\text{ mA}\,(0.5625)$$
$$= \mathbf{4.5\text{ mA}}$$

By using basic algebra we can obtain [from Eq. (6.3)] an equation for the resulting level of VGS for a given level of ID. The derivation is quite straightforward and results in equation (6.8).

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \qquad \textbf{(6.8)}$$

Let us test Eq. (6.8) by finding the level of $V_{GS}$ that will result in a drain current of 4.5 mA for the device with the characteristics of Fig. 6.17. We find

$$\begin{aligned} V_{GS} &= -4\text{ V}\left(1 - \sqrt{\frac{4.5\text{ mA}}{8\text{ mA}}}\right) \\ &= -4\text{ V}(1 - \sqrt{0.5625}) = -4\text{ V}(1 - 0.75) \\ &= -4\text{ V}(0.25) \\ &= \mathbf{-1\text{ V}} \end{aligned}$$

as substituted in the above calculation and verified by Fig. 6.17.

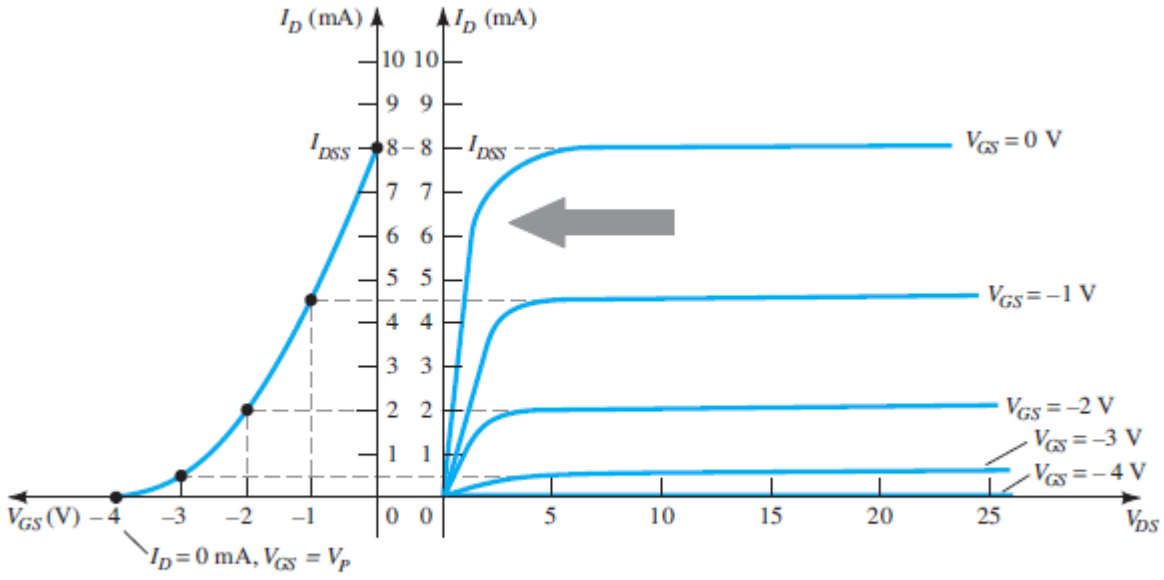



**FIG. 6.17**
*Obtaining the transfer curve from the drain characteristics.*

## Shorthand Method:

If we specify $V_{GS}$ to be one-half the pinch-off value $V_P$, the resulting level of $I_D$ will be the following, as determined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(\frac{1 - V_P/2}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.5)^2$$
$$= I_{DSS}(0.25)$$

and

$$\boxed{I_D = \frac{I_{DSS}}{4}\Big|_{V_{GS} = V_P/2}} \qquad (6.9)$$

The result specifies that the drain current will always be one-fourth the saturation level IDSS as long as the gate-to-source voltage is one-half the pinch-off value

**If we choose ID = IDSS/2 and substitute into Eq. (6.8), we find that**

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$
$$= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)$$

and

$$\boxed{V_{GS} \cong 0.3V_P\big|_{I_D = I_{DSS}/2}} \qquad (6.10)$$

**EXAMPLE 6.1** Sketch the transfer curve defined by $I_{DSS} = 12$ mA and $V_P = -6$ V.

***Solution:*** Two plot points are defined by

$$I_{DSS} = \mathbf{12\ mA} \quad \text{and} \quad V_{GS} = \mathbf{0\ V}$$

and

$$I_D = \mathbf{0\ mA} \quad \text{and} \quad V_{GS} = \boldsymbol{V_P}$$

At $V_{GS} = V_P/2 = -6\text{ V}/2 = \mathbf{-3\ V}$ the drain current is determined by $I_D = I_{DSS}/4 = 12\text{ mA}/4 = \mathbf{3\ mA}$. At $I_D = I_{DSS}/2 = 12\text{ mA}/2 = \mathbf{6\ mA}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = \mathbf{-1.8\ V}$. All four plot points are well defined on Fig. 6.18 with the complete transfer curve.

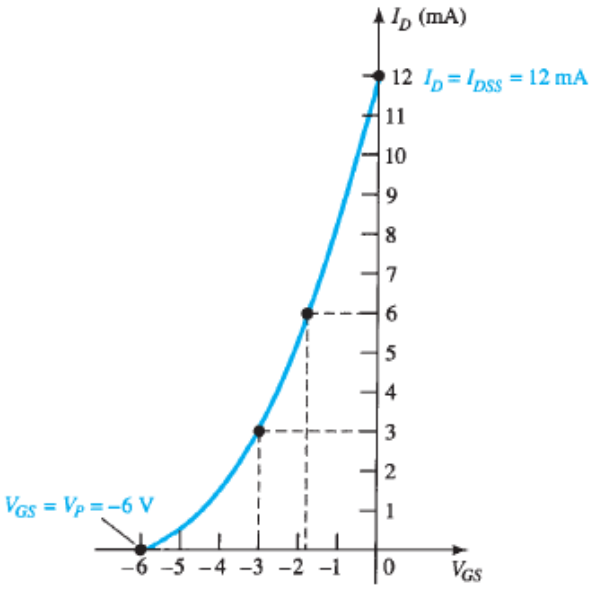



**FIG. 6.18**
*Transfer curve for Example 6.1.*

**EXAMPLE 6.2** Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4$ mA and $V_P = 3$ V.

***Solution:*** At $V_{GS} = V_P/2 = 3\text{ V}/2 = \mathbf{1.5\text{ V}}$, $I_D = I_{DSS}/4 = 4\text{ mA}/4 = \mathbf{1\text{ mA}}$. At $I_D = I_{DSS}/2 = 4\text{ mA}/2 = \mathbf{2\text{ mA}}$, $V_{GS} = 0.3V_P = 0.3(3\text{ V}) = \mathbf{0.9\text{ V}}$. Both plot points appear in Fig. 6.19 along with the points defined by $I_{DSS}$ and $V_P$.

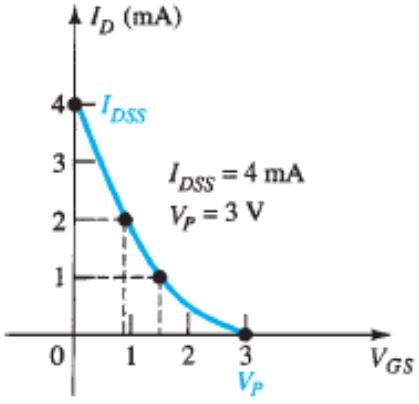



**FIG. 6.19**
*Transfer curve for the p-channel device of Example 6.2.*

## DEPLETION-TYPE MOSFET:

The name MOSFET stands for metal oxide semiconductor field –effect transistor

Basic Construction:

1-A slab of p -type material is formed from a silicon base and is referred to as the substrate.

2- In some cases the substrate is internally connected to the source terminal

3-The source and drain terminals are connected through metallic contacts to n -doped regions linked by an n -channel as shown in the figure

4-The gate is also connected to a metal contact surface but remains insulated from the n -channel by a very thin silicon dioxide (SiO2) layer. SiO2 is a type of insulator referred to as a dielectric

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

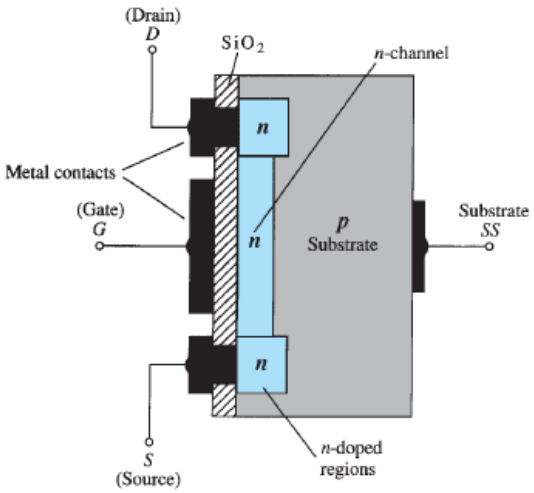



FIG. 6.24
*n-Channel depletion-type MOSFET.*

It is the insulating layer of SiO 2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

**Basic Operation and Characteristics:**

In Fig. 6.25 the gate-to-source voltage is set to 0 V .The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with $V_{GS}$ = 0V continues to be labeled $I_{DSS}$ .

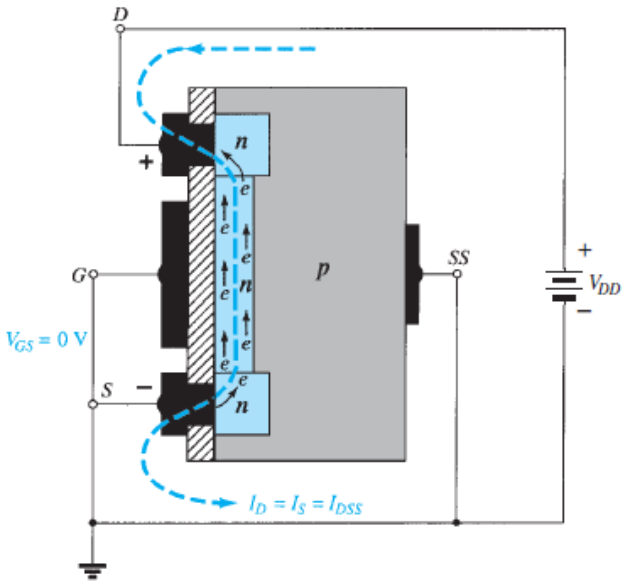



**FIG. 6.25**
*n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage $V_{DD}$.*

**In Fig. 6.27, VGS is set at a negative voltage such as -1 V**. The negative potential at the gate will tend to pressure electrons toward the p -type substrate (like charges repel) and attract holes from the p -type substrate (opposite charges attract) as shown in Fig. 6.27. Depending on the magnitude of the negative bias established by $V_{GS}$, The resulting level of drain current is therefore reduced with increasing negative bias for $V_{GS.}$

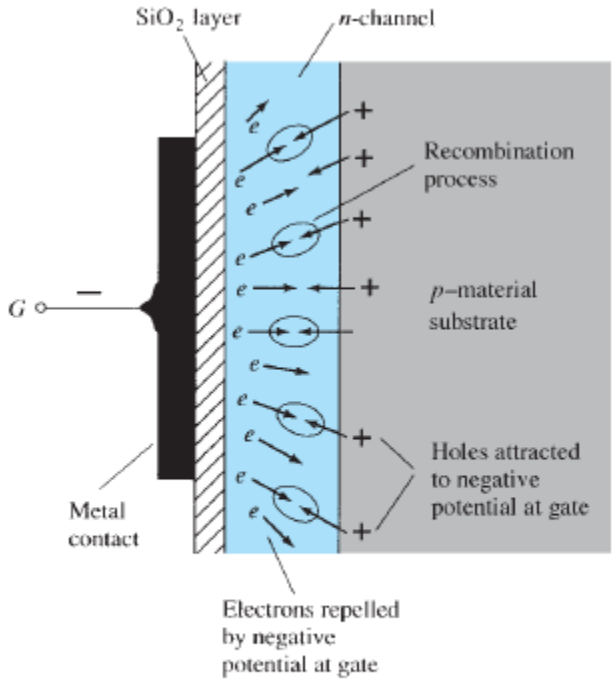



**FIG. 6.27**
*Reduction in free carriers in a channel due to a negative potential at the gate terminal.*

**In Fig. 6.26 for VGS = -1 V, -2 V, and so on**, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET. **For positive values of VGS** , the positive gate will draw additional electrons (free carriers) from the p –type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles As the gate-to-source voltage continues to increase in the positive direction, Fig. 6.26 reveals that the drain current will increase

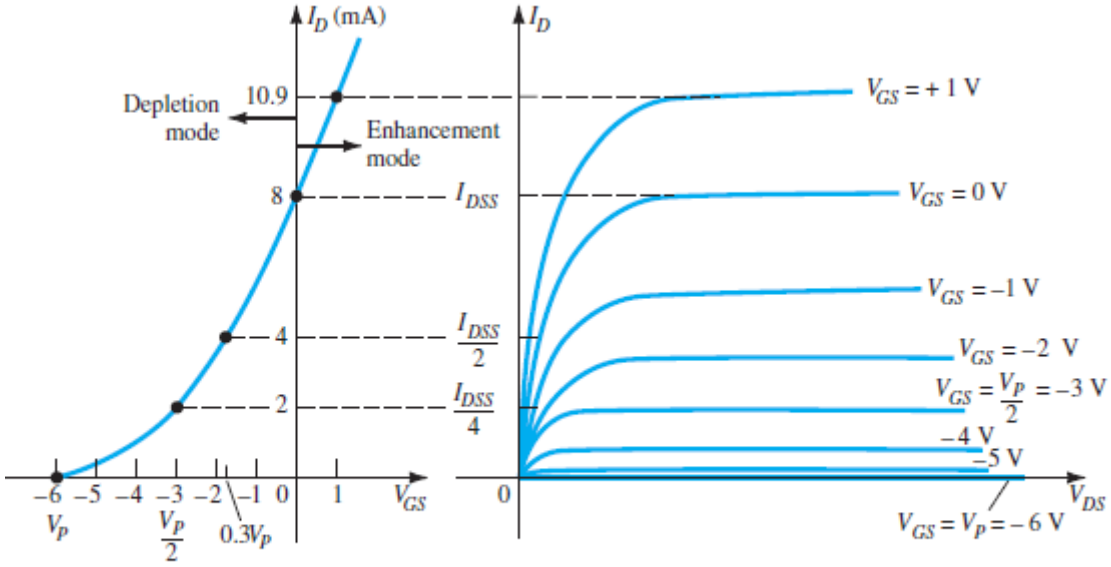



**FIG. 6.26**
*Drain and transfer characteristics for an n-channel depletion-type MOSFET.*

**EXAMPLE 6.3** Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

***Solution:***

$$\text{At } V_{GS} = 0 \text{ V}, \quad I_D = I_{DSS} = 10 \text{ mA}$$
$$V_{GS} = V_P = -4 \text{ V}, \quad I_D = 0 \text{ mA}$$
$$V_{GS} = \frac{V_P}{2} = \frac{-4 \text{ V}}{2} = -2 \text{ V}, \quad I_D = \frac{I_{DSS}}{4} = \frac{10 \text{ mA}}{4} = 2.5 \text{ mA}$$

and at $I_D = \frac{I_{DSS}}{2}$,

$$V_{GS} = 0.3V_P = 0.3(-4 \text{ V}) = -1.2 \text{ V}$$

all of which appear in Fig. 6.28.

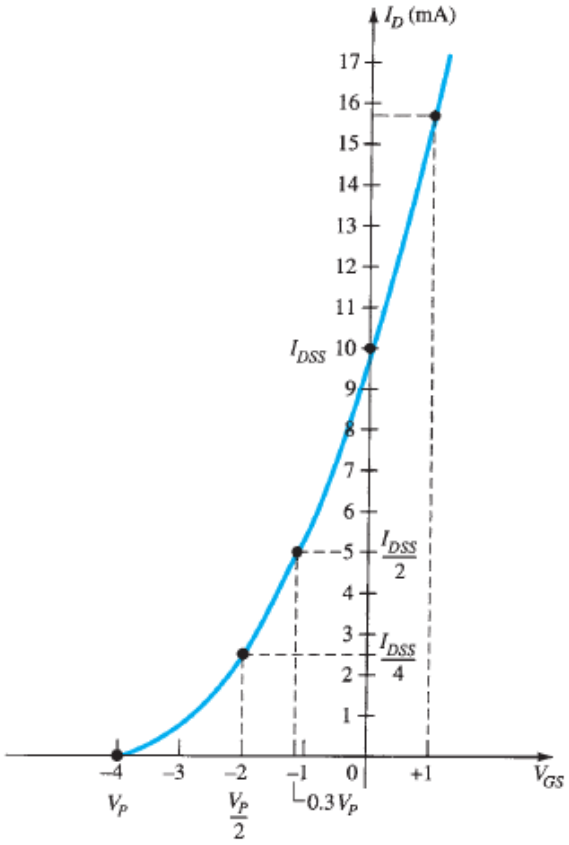



**FIG. 6.28**
*Transfer characteristics for an n-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.*

Before plotting the positive region of $V_{GS}$, keep in mind that $I_D$ increases very rapidly with increasing positive values of $V_{GS}$ . In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we try +1 V as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= (10\text{ mA})\left(1 - \frac{+1\text{ V}}{-4\text{ V}}\right)^2 = (10\text{ mA})\,(1 + 0.25)^2 = (10\text{ mA})\,(1.5625)$$

$$\cong 15.63\text{ mA}$$

which is sufficiently high to finish the plot.

## p -Channel Depletion-Type MOSFET

1- n -type substrate and a p -type channel,

2-all the voltage polarities and the current directions are reversed

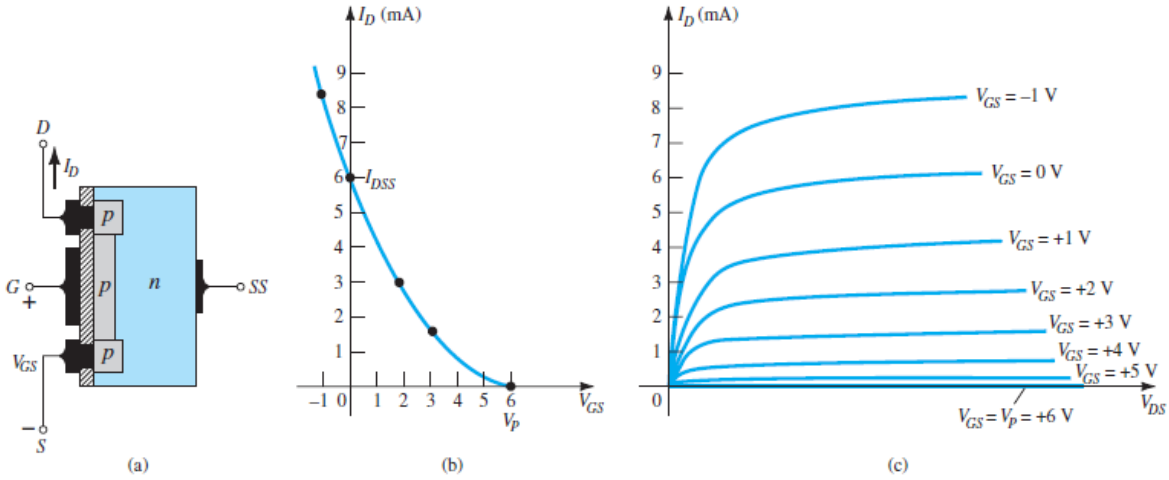



**FIG. 6.29**
*p-Channel depletion-type MOSFET with $I_{DSS}$ = 6 mA and $V_P$ = +6 V.*

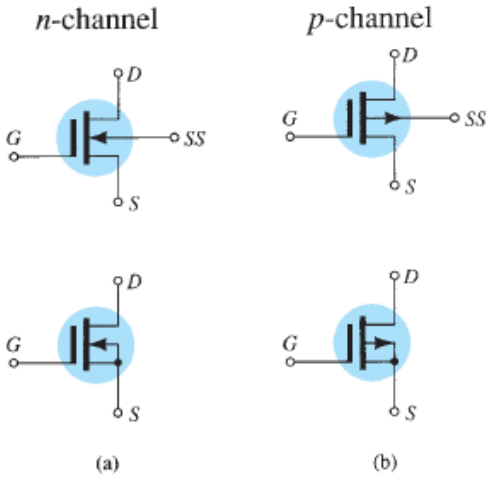



**FIG. 6.30**
*Graphic symbols for: (a) n-channel depletion-type MOSFETs and (b) p-channel depletion-type MOSFETs.*

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## ENHANCEMENT-TYPE MOSFET:

### Basic Construction:

1-p -type material is formed from a silicon base and is again referred to as the substrate

2-the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

3-The drain current is now cut off until the gate-to-source voltage reaches a specific magnitude.

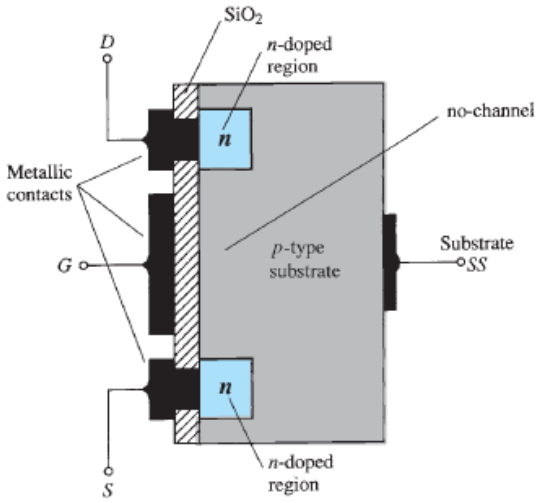


**FIG. 6.32**
*n-Channel enhancement-type MOSFET.*

### Basic Operation and Characteristics:

1- If VGS is set at 0V and a voltage applied between the drain and the source of the device of Fig. 6.32, the absence of an n -channel (with its generous number of free carriers) will result in a current of effectively 0A

2-In Fig.6.33, both VDS and VGS have been set at some positive voltage greater than 0V, establishing the drain and the gate at a positive potential with respect to the source

3-The positive potential at the gate will pressure the holes (since like charges repel) in the p -substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the p -substrate, as shown in the figure. The result is a depletion region near the SiO2 insulating layer void of holes. However, the electrons in the p -substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO2 layer.

4- with VGS increases in magnitude, the concentration of electrons near the SiO2 surface increases until eventually the induced n -type region can support a measurable flow between drain and source

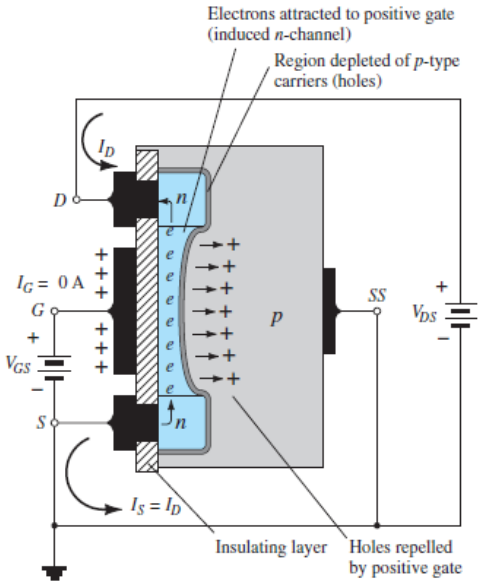


**FIG. 6.33**
*Channel formation in the n-channel enhancement-type MOSFET.*

The level of $V_{GS}$ that results in the significant increase in drain current is called the **threshold voltage** and is given the symbol $V_T$ . As $V_{GS}$ is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold $V_{GS}$ constant and increase the level of $V_{DS}$ , the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of $I_D$ is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 6.34 . Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 6.34 , we find that

$$V_{DG} = V_{DS} - V_{GS} \qquad (6.13)$$

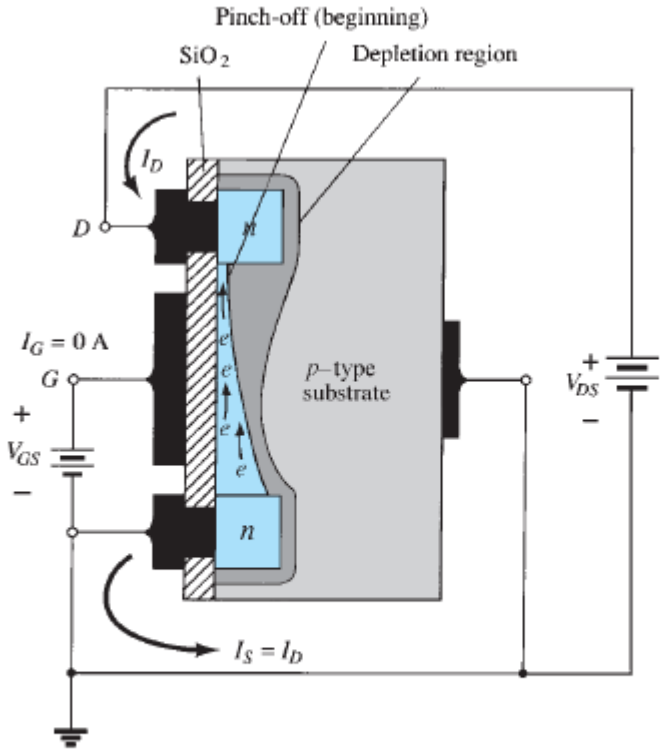


**FIG. 6.34**
*Change in channel and depletion region with increasing level of $V_{DS}$ for a fixed value of $V_{GS}$.*

The drain characteristics of Fig. 6.35 reveal that for the device of Fig. 6.34 with $V_{GS} = 8$ V, saturation occurs at a level of $V_{DS} = 6$ V. In fact, the saturation level for $V_{DS}$ is related to the level of applied $V_{GS}$ by

$$V_{DS_{sat}} = V_{GS} - V_T \tag{6.14}$$

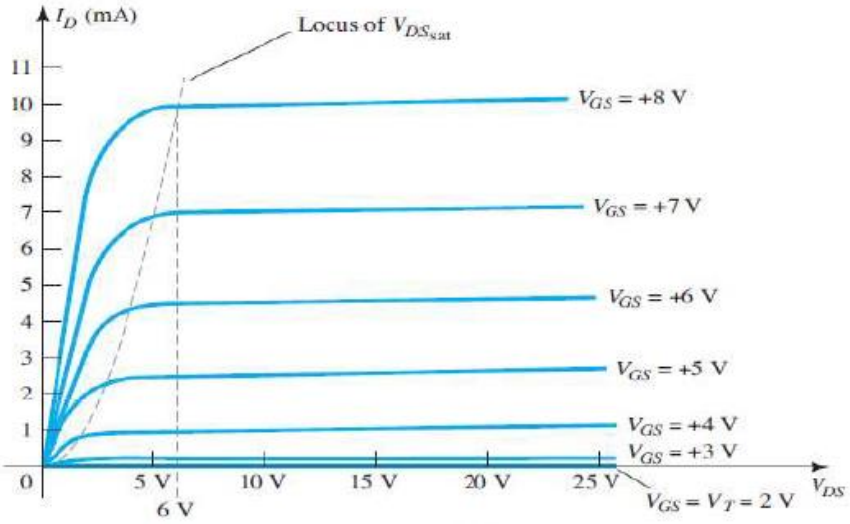


**FIG. 6.35**
*Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V².*

**For values of VGS less than the threshold level, the drain current of an enhancement type MOSFET is 0 mA.**

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2 \tag{6.15}$$

$V_{GS}$. The $k$ term is a constant that is a function of the construction of the device. The value of $k$ can be determined from the following equation [derived from Eq. (6.15)], where $I_{D(on)}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \tag{6.16}$$

Substituting $I_{D(on)} = 10$ mA when $V_{GS(on)} = 8$ V from the characteristics of Fig. 6.35 yields

$$k = \frac{10 \text{ mA}}{(8 \text{ V} - 2 \text{ V})^2} = \frac{10 \text{ mA}}{(6 \text{ V})^2} = \frac{10 \text{ mA}}{36 \text{ V}^2}$$
$$= \mathbf{0.278 \times 10^{-3} \text{ A/V}^2}$$

# p -Channel Enhancement-Type MOSFETs

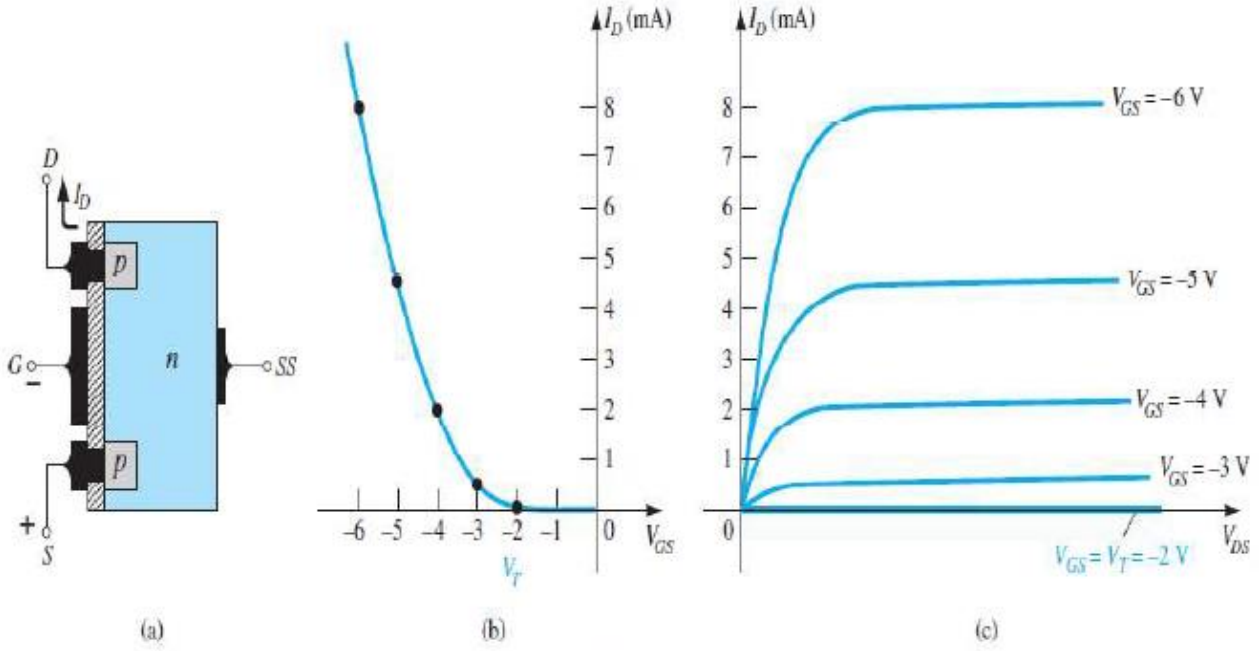


**FIG. 6.38**
*p-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}$ A/V$^2$.*

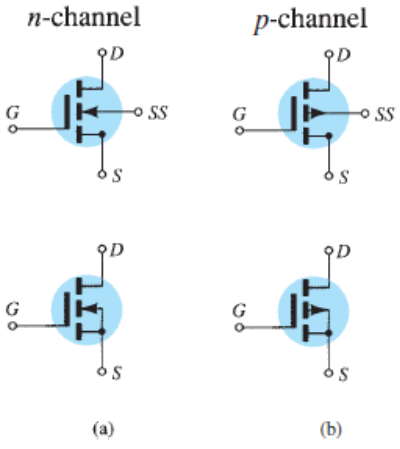


**FIG. 6.39**
*Symbols for: (a) n-channel enhancement-type MOSFETs and (b) p-channel enhancement-type MOSFETs.*

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**EXAMPLE 6.4** Using the data provided on the specification sheet of Fig. 6.40 and an average threshold voltage of $V_{GS(Th)} = 3$ V, determine:

a. The resulting value of $k$ for the MOSFET.
b. The transfer characteristics.

***Solution:***

a. Eq. (6.16): $$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$
$$= \frac{3\text{ mA}}{(10\text{ V} - 3\text{ V})^2} = \frac{3\text{ mA}}{(7\text{ V})^2} = \frac{3 \times 10^{-3}}{49}\text{A/V}^2$$
$$= \mathbf{0.061 \times 10^{-3}\,A/V^2}$$

b. Eq. (6.15): $$I_D = k(V_{GS} - V_T)^2$$
$$= 0.061 \times 10^{-3}(V_{GS} - 3\text{ V})^2$$

For $V_{GS} = 5$ V,
$$I_D = 0.061 \times 10^{-3}(5\text{ V} - 3\text{ V})^2 = 0.061 \times 10^{-3}(2)^2$$
$$= 0.061 \times 10^{-3}(4) = 0.244\text{ mA}$$

For $V_{GS} = 8, 10, 12$, and 14 V, $I_D$ will be 1.525, 3 (as defined), 4.94, and 7.38 mA, respectively. The transfer characteristics are sketched in Fig. 6.41.

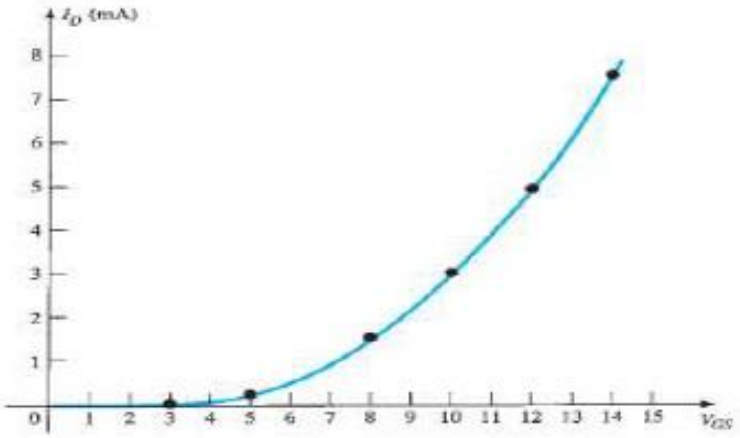


**FIG. 6.41**
*Solution to Example 6.4.*