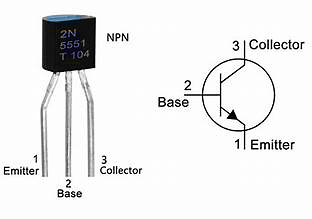
**Electronic Circuit**

**Lecture 5 ( Week)**

**DC biasing (BJT)**



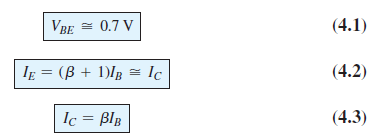
4.1 INTRODUCTION

The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality,

any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.

The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion.

The following important basic relationships for a transistor:



في هذا الفصل سنتعلم وضع الترانزستور في وضع التشغيل عن طريق تحديد قيم الجهد والتيار المستمر في هذا الترانزستور حتى يكون جاهز لتكبير الاشارة. هنالك اكثر من طريقة لعمل ذلك سنتعرف عليها لاحقا.

4.2 OPERATING POINT

The term biasing appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.

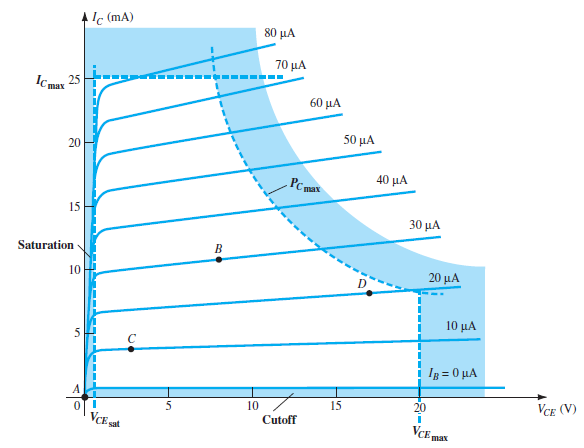


FIG.1: Various operating points within the limits of operation of a transistor

يمكن تمييز عدة مناطق في منحنى خصائص الترانستور ولكي يعمل الترانستور كمكبر يجب ان يكون في المنطقة الفعالة وعلية يجب مراعاة اختيار مصدر الجهد والمقاومات والربط بطريقة تضمن بقاء انحياز الترانستور في المنطقة الفعالة.

**For the BJT to be biased in its linear or active operating region the following must be true:**

1. The base emitter junction must be forward-biased (P-region voltage more positive), with a resulting forward-bias voltage of about 0.6 V to 0.7 V.

2. The base collector junction must be reverse-biased (N-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.

[Note that for forward bias the voltage across the p n junction is p - positive, whereas for reverse bias it is opposite (reverse) with n -positive.]

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

**1. Linear-region operation:**

Base emitter junction forward-biased

Base collector junction reverse-biased

**2. Cutoff-region operation:**

Base emitter junction reverse-biased

Base collector junction reverse-biased

**3. Saturation-region operation:**

Base emitter junction forward-biased

Base collector junction forward-biased

**4.3 FIXED-BIAS CONFIGURATION**

The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration.

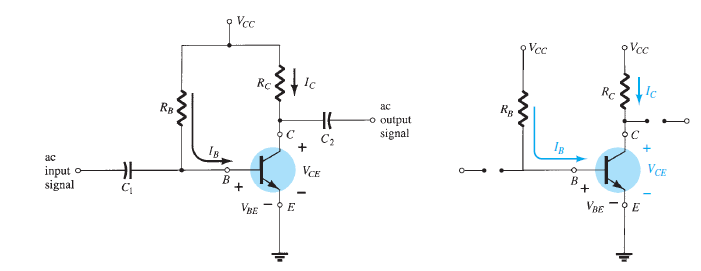


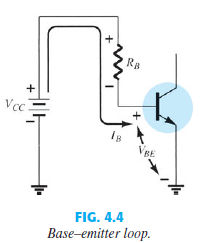
FIG. 2: Fixed-bias circuit. FIG. 3: DC equivalent of Fig.2

في هذه الدائرة يتم اولا تحليل دائرة الدخل لحاسب تيار القاعدة ومن ثم تحليل دائرة الخرج لحساب تيار الجامع وفولتية الخرج

**Forward Bias of Base Emitter:**

Consider first the base emitter circuit loop of Fig. 4.4 . Writing Kirchhoff’s voltage equation in the clockwise direction for the loop, we obtain

+VCC - IBRB - VBE = 0



Note the polarity of the voltage drop across RB as established by the indicated direction of IB . Solving the equation for the current IB results in the following

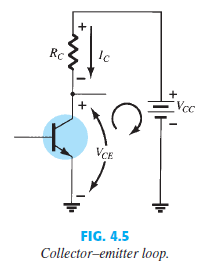


نلاحظ ان قيمة تيار القاعدة يعتمد على قيمة المقاومة وكذلك على قيمة فولتية المصدر منقوص منها ال0.7 فولت

**Collector Emitter Loop:**

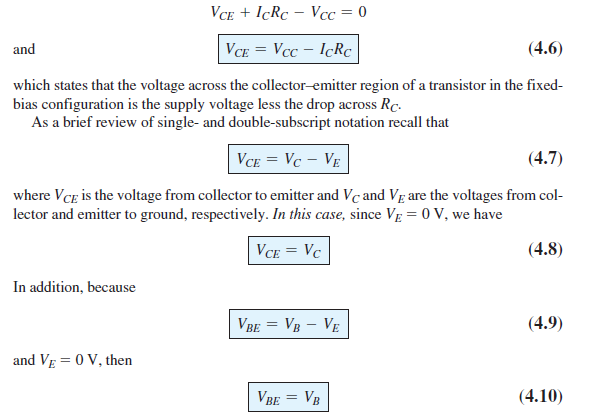
The collector emitter section of the network appears in Fig. 4.5 with the indicated direction of current IC and the resulting polarity across RC . The magnitude of the collector current is related directly to IB through

نلاحظ ان قيمة تيار الجامع يعتمد على قيمة تيار القاعدة مضروب في قيمة البيتا





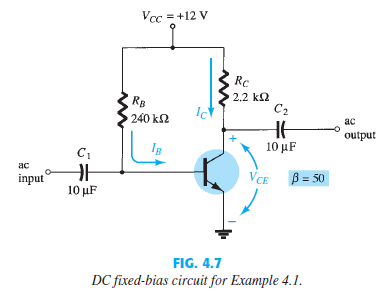
Applying Kirchhoff’s voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 results in the following:

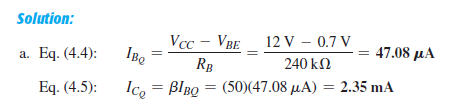


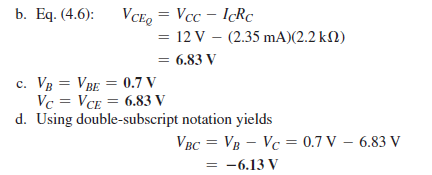
EXAMPLE 4.1

Determine the following for the fixed-bias configuration of Fig. 4.7 .

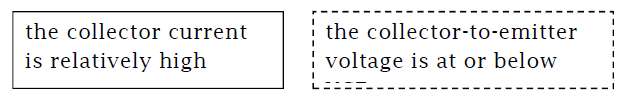
1. IBQ and ICQ. b. VCEQ. c. VB and VC . d. VBC .

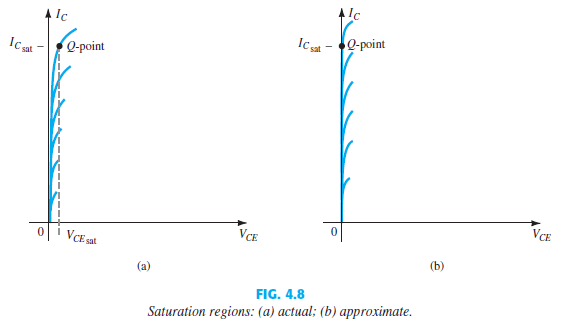






**Transistor Saturation**

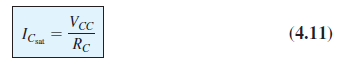
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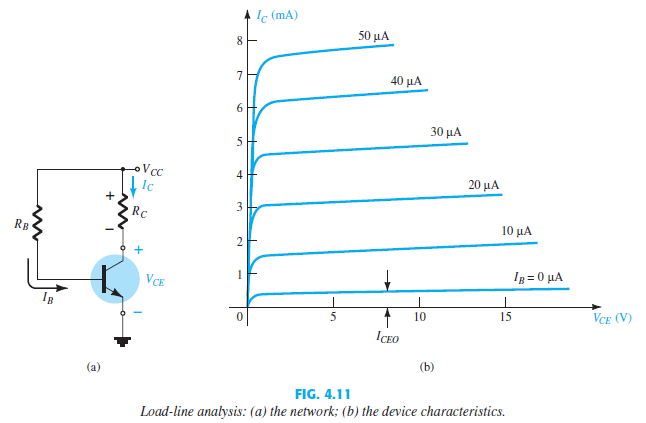
FIG. 4.9 Determining ICsat

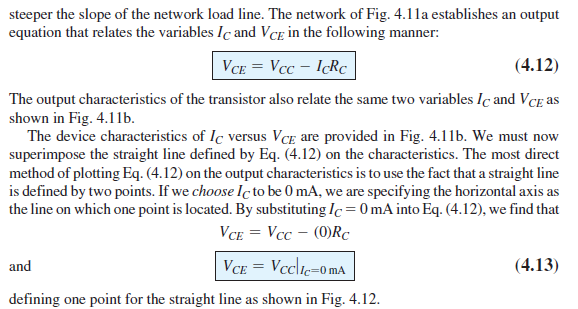
**The resulting saturation current for the fixed-bias configuration is**

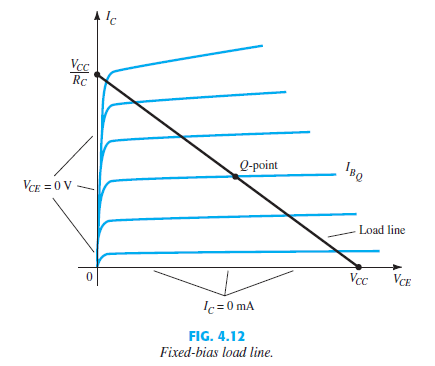
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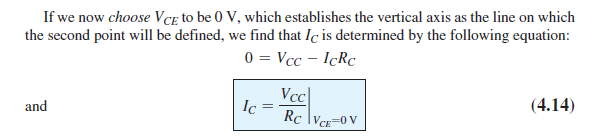
**تيار التشبع هو اعلى تيار ممكن الحصول عليه وذلك عندما تكون الفولتية تقريبا صفر**

**Load-Line Analysis:**

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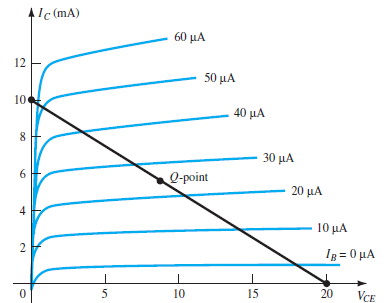


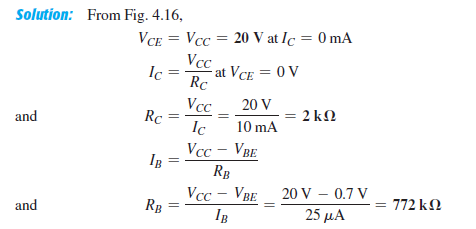




EXAMPLE 4.2:

Given the load line of Fig. 4.16 and the defined Q -point, determine the required values of VCC , RC , and RB for a fixed-bias configuration.





4.4 EMITTER-BIAS CONFIGURATION:

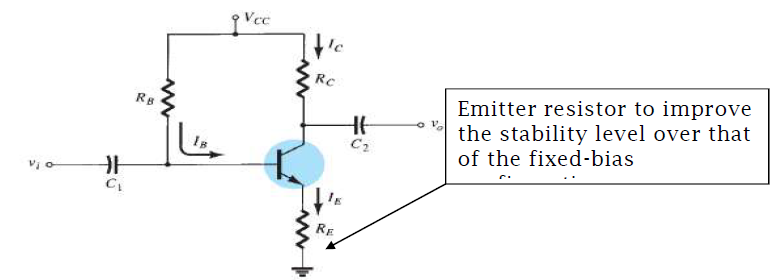
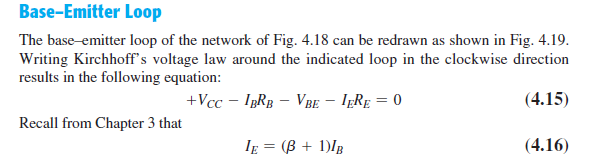
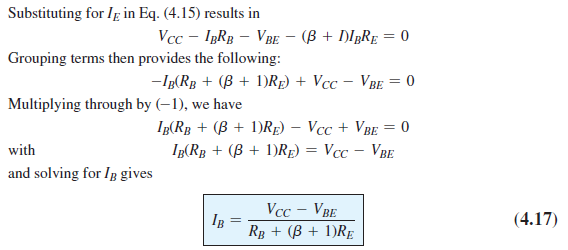
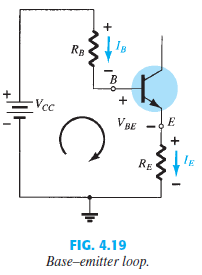
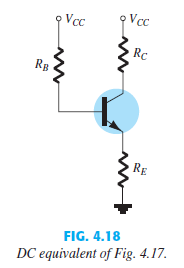
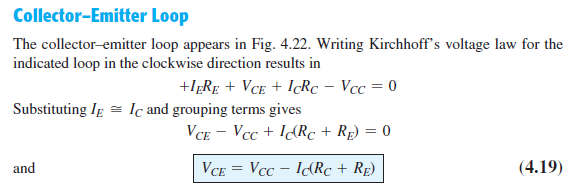


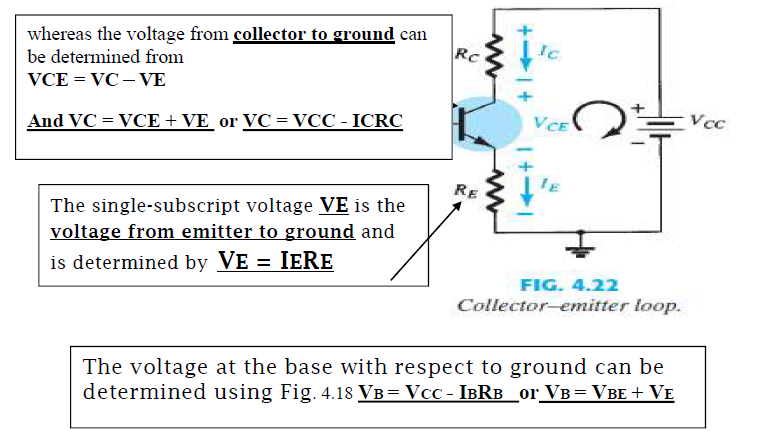
FIG. 4.17 BJT bias circuit with emitter resistor.







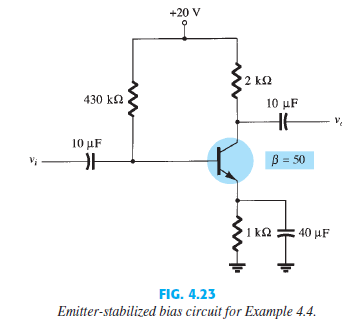


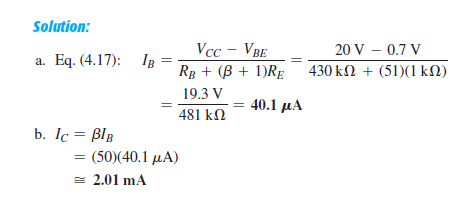


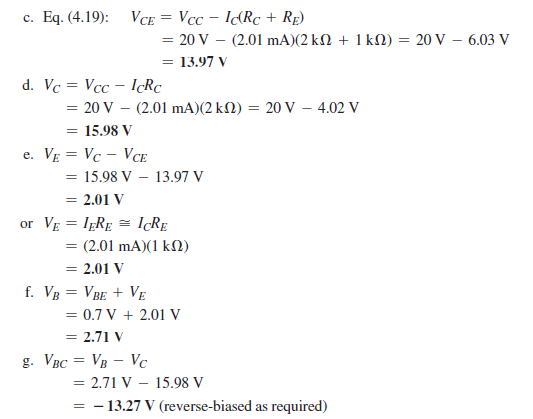
EXAMPLE 4.3 :

For the emitter-bias network of Fig. 4.23 , determine:

a. IB . b. IC . c. VCE . d. VC . e. VE . f. VB . g.VBC

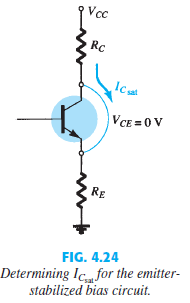


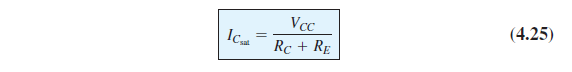


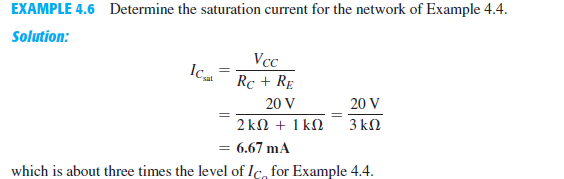


Saturation Level:

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.24 and calculate the resulting collector current. For Fig. 4.24







Load-Line Analysis:

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of I B as determined by Eq. (4.17) defines the level of I B on the characteristics of Fig. 4.25 (denoted IBQ). The collector–emitter loop equation that defines the load line is

VCE = VCC - IC(RC + RE)

