Diode Clamping Circuits

Basic Definition:

The clamping circuit (***clamper***) is one will "clamp" a signal to a different dc level. The circuit must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of$R$ and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval (T/2) the diode is nonconducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants. Therefore, the condition required for the capacitor to hold its voltage during the discharge period between pulses of the input signal is

$$5\tau = 5RC >> \frac{T}{2} = \frac{1}{2f} \qquad [4.1]$$

Example 4-1:

Determine the output (v_o) for the circuit of Fig. 4-1 for the input (v_i) shown.

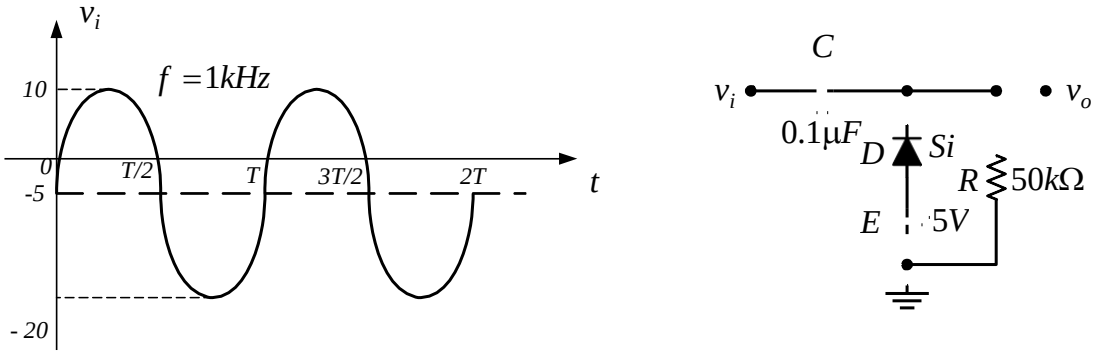
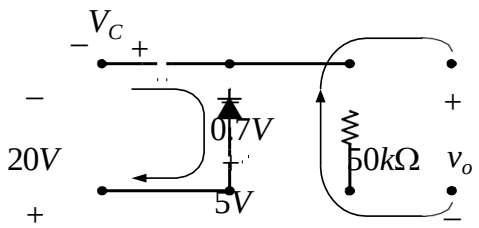


Fig. 4-1

***Solution*:**

The analysis of clamping circuits are started by considering that the part of the input signal that will forward bias the diode. For the circuit of Fig. 4-1, the diode is forward bias ("on" state) during the negative half period of the input signal (v_i) and the capacitor will charge up instantaneously to a voltage level determined by the circuit of Fig. 4-2.



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For the input section KVL will result in

$$-20 + V_C + 0.7 - 5 = 0 \quad \Rightarrow \quad V_C = 24.3 \text{ V}.$$

The output voltage (v_o) can be determined by KVL in the output section

$$+5 - 0.7 - v_o = 0 \quad \Rightarrow \quad v_o = 4.3 \text{ V}.$$

Now check that the capacitor will hold on or not its establish voltage level during the period (positive half period in case of Example 4-1) when the diode is in the "off" state (reverse bias). The total time constant 5τ of the discharging circuit ofFig. 4-3 is determined by the product $5RC$ and has the magnitude

$$5\tau = 5RC = 5\,(50\times10^{3})\,(0.1\times10^{-6}) = 25 \text{ ms}.$$

The frequency (f) is 1 kHz, resulting in a period of 1 ms and an interval of 0.5 ms between levels, that is

$$T/2 = 1/(\,2f\,) = 1/(2 \times 1\times10^{3}) = 0.5 \text{ ms}.$$

We find that

$$5\,\tau \;>>\; T/2 \text{ (25ms / 0.5ms = 50 times).}$$

So that, it is certainly a good approximation that the capacitor will hold its voltage (24.3 V) during the discharge period between pulses of the input signal.

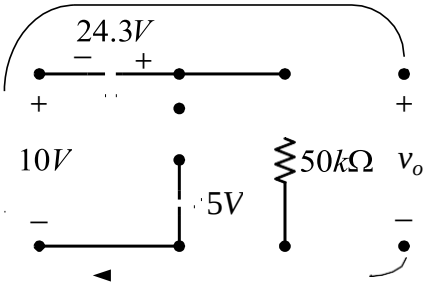


Fig. 4-3

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o, and applying KVL around the outside loop of circuit will result in

$$+10 + 24.3 - v_o = 0 \quad \Rightarrow \quad v_o = 34.3 \text{ V}.$$

The resulting output appears in Fig. 4-4, where the input and the output swing are the same.

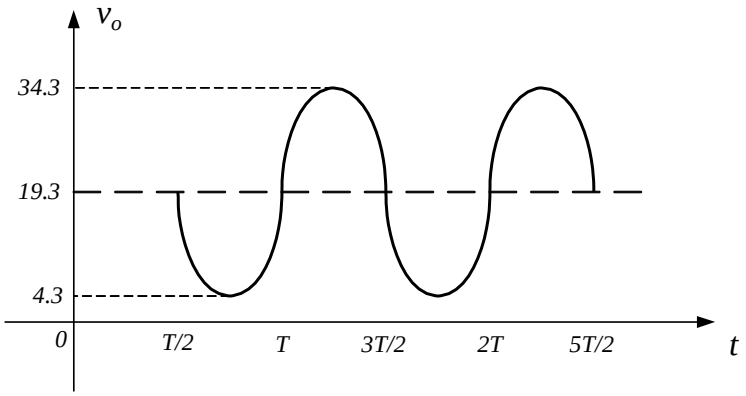


Fig. 4-4

Example 4-2:

Using silicon diode, design a clamper circuit that will produce output $v_o = 10Sin\omega t - 5$ V when the input is $v_i = 10Sin\omega t + 5$ V. Draw the circuit diagram and the input and output signals.

Solution:

From the input (v_i) and output (v_o) signals, we have a negative biased clamper. Therefore, the diode is forward bias ("on" state) during the positive half period of the input signal (v_i). The output voltage (v_o) at this positive period can be determined by KVL in the output section of the circuit shown in Fig. 4-5.

$E + 0.7 - v_o = 0 \Rightarrow E = 5 - 0.7 = 4.3$ V.

For the input section KVL will result in

$15 - V_C - 5 = 0 \Rightarrow V_C = 10$ V.

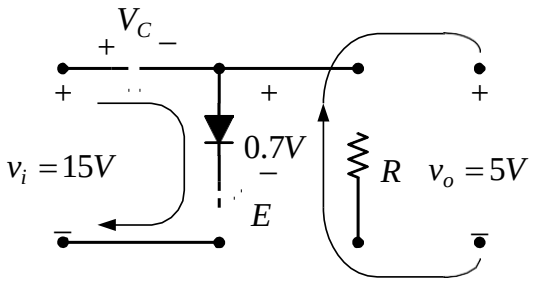
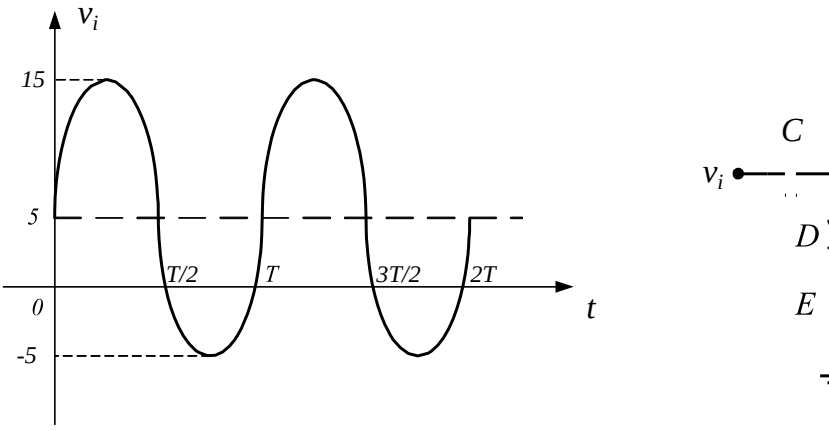
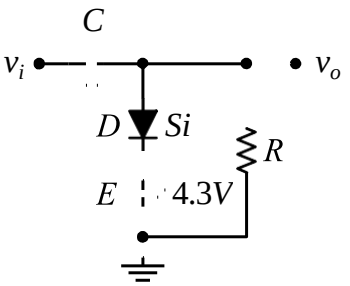


Fig. 4-5

The circuit diagram and the input and output signals are shown in Fig. 4-6.





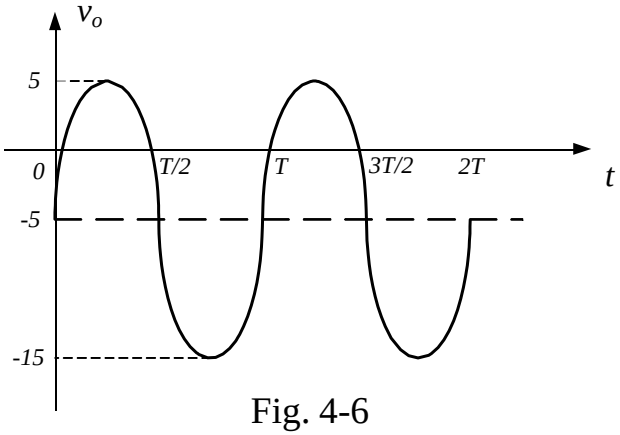
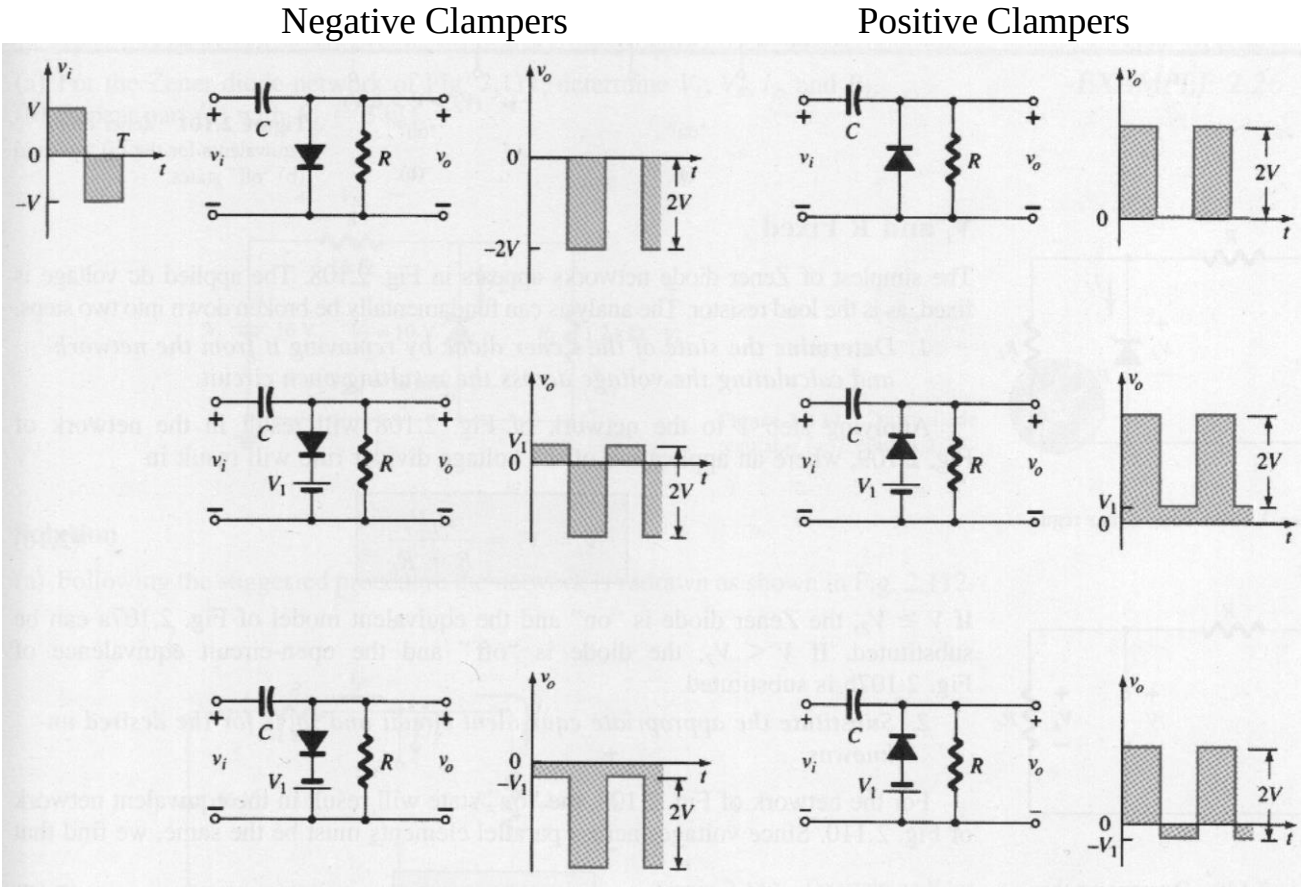


Fig. 4-6

Summary:

A number of clamping circuits and their effect on the square-wave input signal are shown in Fig. 4-7.



Clampers with ideal diodes and $5\tau = 5RC >> T/2$

Fig. 4-7

Exercise:

Sketch the output (v_o) for the circuit of Fig. 4-8 for the input (v_i) shown. Assume ideal diodes.

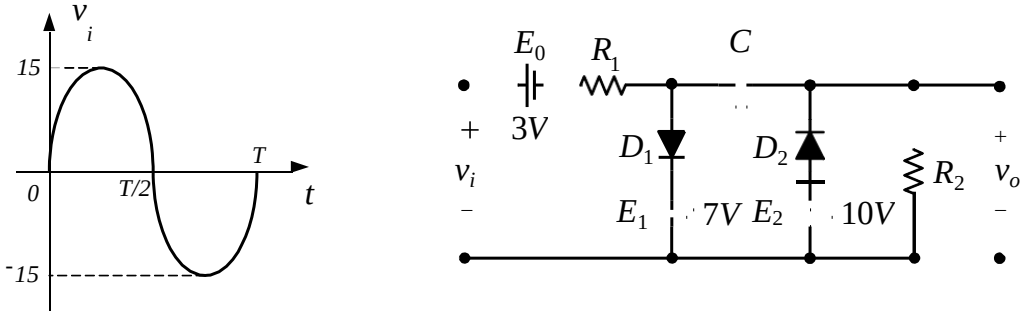


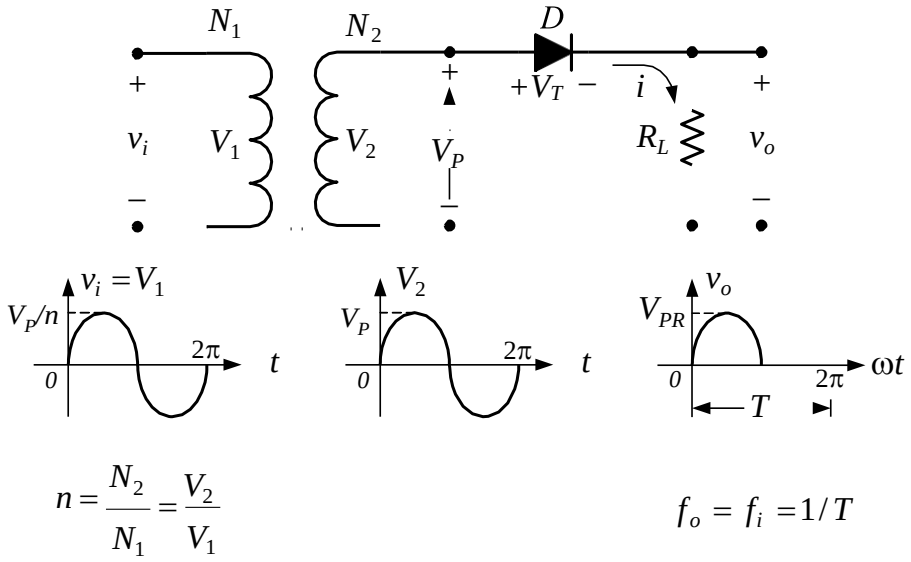
Fig. 4-8

Diode Rectifier Circuits

Basic Definition:

A diode circuit that converts an ac voltage to a pulsating dc voltage and permits current to flow in one direction only is called "***rectifier***" and the ac-to-dc conversion process is termed "***rectification***".

Half-Wave Rectifier (HWR):



$$n = \frac{N_2}{N_1} = \frac{V_2}{V_1}$$

$$f_o = f_i = 1/T$$

Fig. 5-1

For the half-wave rectifier circuit of Fig. 5-1:

◄ The average (dc) value of a half-wave rectified sine-wave voltage (V_{dc}) is

$$V_{dc} = \frac{1}{T}\int_0^T v_o(\omega t)\cdot d\omega t = \frac{1}{2\pi}\int_0^{\pi} V_{PR} Sin\omega t \cdot d\omega t = \frac{V_{PR}}{\pi}$$

For V_P close to V_T,

$$\boxed{V_{dc} = 0.318(V_P - V_T)} \qquad [5.1a]$$

For $V_P >> V_T$,

$$\boxed{V_{dc} = 0.318V_P} \qquad [5.1b]$$

◄ The root mean square (rms) value of the load voltage (V_{rms}) is

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v_o^2(\omega t)\cdot d\omega t} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} V_{PR}^2 Sin^2\omega t \cdot d\omega t} = \frac{V_{PR}}{2}$$

For V_P close to V_T,

$$\boxed{V_{rms} = 0.5(V_P - V_T)}$$

For $V_P >> V_T$,

$$\boxed{V_{rms} = 0.5V_P}$$

[5.2a]

[5.2b]

◄ The rms value of the ac component (or ***the ripple voltage***) of the rectified signal [$V_r(rms)$] is

$$V_r(rms) = \sqrt{V_{rms}^2 - V_{dc}^2} = \sqrt{(0.5V_{PR})^2 - (0.318V_{PR})^2} = 0.385V_{PR}$$

For V_P close to V_T,

$$\boxed{V_r(rms) = 0.385(V_P - V_T)} \qquad [5.3a]$$

For $V_P >> V_T$,

$$\boxed{V_r(rms) = 0.385V_P} \qquad [5.3b]$$

◄ The percent ripple (r) in the rectified waveform (also called ***the ripple factor***) is

$$r = \frac{V_r(rms)}{V_{dc}} \times 100\% = \frac{0.385V_{PR}}{0.318V_{PR}} \times 100\% = 121\%$$

◄ Efficiency (η) = [$P_{dc}(load) / P_{total}(circuit)$] × 100%

$$\eta = \frac{I_{dc}^2 R_L}{I_{rms}^2 (r_d + R_L)} \times 100\% = \frac{(0.318I_P)^2 R_L}{(0.5I_P)^2 (r_d + R_L)} \times 100\% = \frac{40.5}{1 + r_d / R_L}\%$$

For ideal diode (r_d = 0 Ω), $\eta = \eta_{max}$ = 40.5 %

◄ The peak inverse voltage (*PIV*) of the diode is

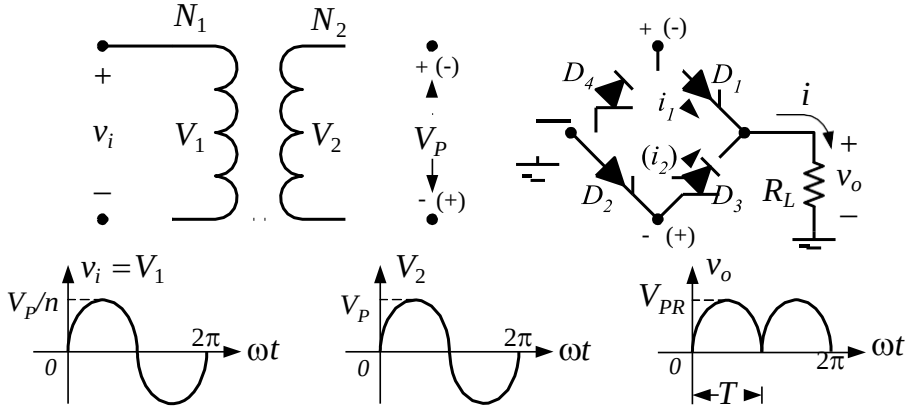
$$\boxed{PIV = V_P} \qquad [5.4]$$

◄ The frequency of the output rectified signal (f_o) is

$$\boxed{f_o = f_i} \qquad [5.5]$$

Full-Wave Rectifiers (FWRs):

1. A Bridge Full-Wave Rectifier:



$$n = \frac{N_2}{N_1} = \frac{V_2}{V_1}$$

$$f_o = 2\, f_i$$

$$i = i_1 + i_2$$

Fig. 5-2

For the bridge full-wave rectifier circuit of Fig. 5-2:

◄ $V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_{PR} Sin\omega t \cdot d\omega t = \frac{2V_{PR}}{\pi}$

For V_P close to $2V_T$,

$$\boxed{V_{dc} = 0.636(V_P - 2V_T)} \qquad [5.6a]$$

For $V_P >> 2V_T$,

$$\boxed{V_{dc} = 0.636V_P} \qquad [5.6b]$$

◄ $V_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} V_{PR}^2 Sin^2\omega t \cdot d\omega t} = \frac{V_{PR}}{\sqrt{2}}$

For V_P close to $2V_T$,

$$\boxed{V_{rms} = 0.707(V_P - 2V_T)} \qquad [5.7a]$$

For $V_P >> 2V_T$,

$$\boxed{V_{rms} = 0.707V_P} \qquad [5.7b]$$

◄ $V_r(rms) = \sqrt{V_{rms}^2 - V_{dc}^2} = \sqrt{(0.707V_{PR})^2 - (0.636V_{PR})^2} = 0.308V_{PR}$

For V_P close to $2V_T$,

$$\boxed{V_r(rms) = 0.308(V_P - 2V_T)} \qquad [5.8a]$$

For $V_P >> 2V_T$,

$$\boxed{V_r(rms) = 0.308V_P} \qquad [5.8b]$$

◄ $r = \frac{V_r(rms)}{V_{dc}} \times 100\% = \frac{0.308V_{PR}}{0.636V_{PR}} \times 100\% = 48.4\%$

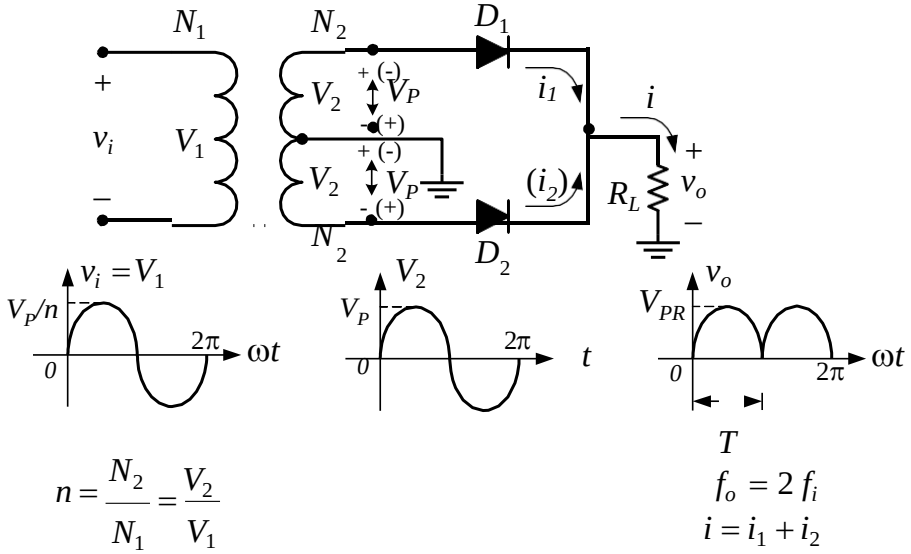
◄ $\eta = \frac{I_{dc}^2 R_L}{I_{rms}^2(2r_d + R_L)} \times 100\% = \frac{(0.636I_P)^2 R_L}{(0.707I_P)^2(2r_d + R_L)} \times 100\% = \frac{81}{1 + 2r_d / R_L}\%$

For ideal diode (r_d = 0 Ω), $\eta = \eta_{max}$ = 81 %

◄ $\boxed{PIV = V_P - 2V_T}$ [5.9]

◄ $\boxed{f_o = 2\,f_i}$ [5.10]

2. A Center-Tapped (CT) Full-Wave Rectifier:



$$n = \frac{N_2}{N_1} = \frac{V_2}{V_1}$$

$$f_o = 2\,f_i$$

$$i = i_1 + i_2$$

Fig. 5-3

For the center-tapped full-wave rectifier circuit of Fig. 5-3:

◄ $$V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_{PR} Sin\omega t \cdot d\omega t = \frac{2V_{PR}}{\pi}$$

For V_P close to V_T,

$$\boxed{V_{dc} = 0.636(V_P - V_T)} \qquad [5.11a]$$

For $V_P >> V_T$,

$$\boxed{V_{dc} = 0.636V_P} \qquad [5.11b]$$

◄ $$V_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} V_{PR}^2 Sin^2\omega t \cdot d\omega t} = \frac{V_{PR}}{\sqrt{2}}$$

For V_P close to V_T,

$$\boxed{V_{rms} = 0.707(V_P - V_T)} \qquad [5.12a]$$

For $V_P >> V_T$,

$$\boxed{V_{rms} = 0.707V_P} \qquad [5.12b]$$

◄ $$V_r(rms) = \sqrt{V_{rms}^2 - V_{dc}^2} = \sqrt{(0.707V_{PR})^2 - (0.636V_{PR})^2} = 0.308V_{PR}$$

For V_P close to V_T,

$$\boxed{V_r(rms) = 0.308(V_P - V_T)}$$

$$\boxed{V_r(rms) = 0.308V_P}$$

[5.13a]

For $V_P >> V_T$,

[5.13b]

◄ $r = \dfrac{V_r(rms)}{V_{dc}} \times 100\% = \dfrac{0.308V_{PR}}{0.636V_{PR}} \times 100\% = 48.4\%$

◄ $\eta = \dfrac{I_{dc}^2 R_L}{I_{rms}^2 (r_d + R_L)} \times 100\% = \dfrac{(0.636I_P)^2 R_L}{(0.707I_P)^2 (r_d + R_L)} \times 100\% = \dfrac{81}{1 + r_d / R_L}\%$

For ideal diode ($r_d = 0\ \Omega$), $\eta = \eta_{max} = 81\ \%$

◄ $\boxed{PIV = 2V_P - V_T}$ [5.14]

◄ $\boxed{f_o = 2f_i}$ [5.15]

Summary:

Different parameters for the HWR and FWR circuits are listed in Table 5-1.

Table 5-1

Parameter	HWR	FWR	
		Bridge	CT
V_{PR}	$V_P - V_T$	$V_P - 2V_T$	$V_P - V_T$
V_{dc}	$0.318V_{PR}$	$0.636V_{PR}$	
V_{rms}	$0.5V_{PR}$	$0.707V_{PR}$	
V_r	$0.385V_{PR}$	$0.308V_{PR}$	
r	121%	48.4%	
η_{max}	40.5%	81%	
PIV	V_P	$V_P - 2V_T$	$2V_P - V_T$
f_o	f_i	$2f_i$	

Example 5-1:

The input voltage to a full-wave rectifier employing a center-tapped step-down transformer and two silicon diodes is 220 V rms, and the transformer has turns ratio $n = 0.125$. Draw the rectifier circuit diagram when it is connected to a $100\ \Omega$ load, and find

1. the average value of the voltage across the load.
2. the average power dissipated by the load, and
3. the minimum *PIV* rating required for each diode.

Solution:

The rectifier circuit diagram is shown in Fig. 5-4.

1. $V_P = \sqrt{2} v_i n = \frac{}{\sqrt{2}} * 220 * 0.125 = 38.9V.$

$V_{dc} = 0.636(V_P - V_T) = 0.636(38.9 - 0.7) = 24.3V.$

2. $V_{rms} = 0.707(V_P - V_T) = 0.707(38.9 - 0.7) = 27.0V.$

$P_{av} = \frac{V_{rms}^2}{R_L} = \frac{(27.0)^2}{100} = 7.3W.$

3. $PIV \geq (2V_P - V_T) = (2 * 38.9 - 0.7) = 77.1V.$

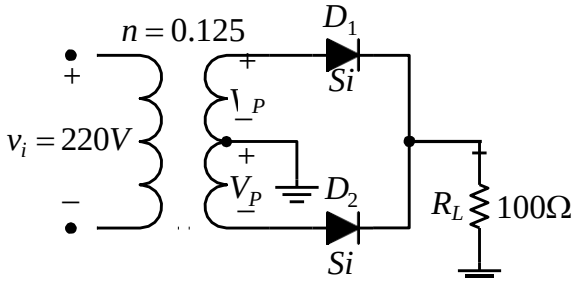


Fig. 5-4