Diode Clamping Circuits

Basic Definition:

The clamping circuit (***clamper***) is one will "clamp" a signal to a different dc level. The circuit must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval $(T/2)$ the diode is nonconducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants. Therefore, the condition required for the capacitor to hold its voltage during the discharge period between pulses of the input signal is

$$\boxed{5\tau = 5RC >> \frac{T}{2} = \frac{1}{2f}} \qquad [4.1]$$

Example 4-1:

Determine the output (v_o) for the circuit of Fig. 4-1 for the input (v_i) shown.

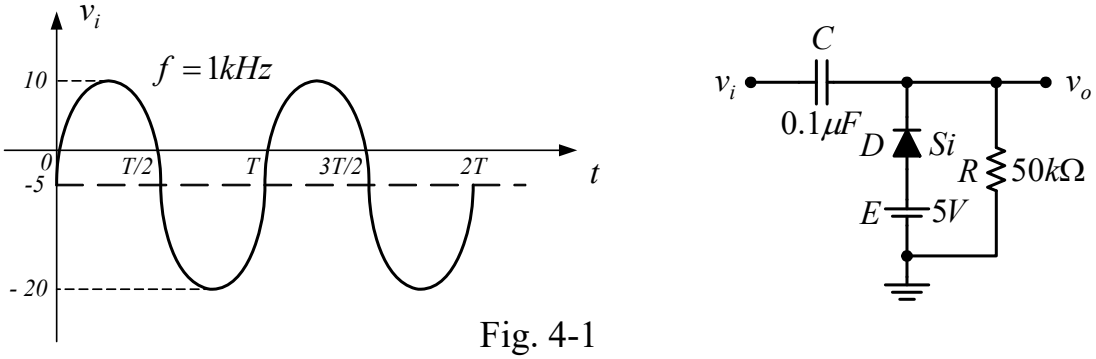


Fig. 4-1

***Solution*:**

The analysis of clamping circuits are started by considering that the part of the input signal that will forward bias the diode. For the circuit of Fig. 4-1, the diode is forward bias ("on" state) during the negative half period of the input signal (v_i) and the capacitor will charge up instantaneously to a voltage level determined by the circuit of Fig. 4-2.

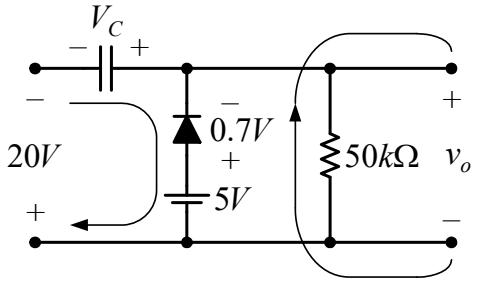


Fig. 4-2

For the input section KVL will result in

$$-20 + V_C + 0.7 - 5 = 0 \quad \Rightarrow \quad V_C = 24.3 \text{ V}.$$

The output voltage (v_o) can be determined by KVL in the output section

$$+5 - 0.7 - v_o = 0 \quad \Rightarrow \quad v_o = 4.3 \text{ V}.$$

Now check that the capacitor will hold on or not its establish voltage level during the period (positive half period in case of Example 4-1) when the diode is in the "off" state (reverse bias). The total time constant 5τ of the discharging circuit of Fig. 4-3 is determined by the product $5RC$ and has the magnitude

$$5\tau = 5RC = 5\,(50\times10^3)\,(0.1\times10^{-6}) = 25 \text{ ms}.$$

The frequency (f) is 1 kHz, resulting in a period of 1 ms and an interval of 0.5 ms between levels, that is

$$T/2 = 1/(2f) = 1/(2 \times 1\times10^3) = 0.5 \text{ ms}.$$

We find that

$$5\tau >> T/2 \quad (25\text{ms} / 0.5\text{ms} = 50 \text{ times}).$$

So that, it is certainly a good approximation that the capacitor will hold its voltage (24.3 V) during the discharge period between pulses of the input signal.

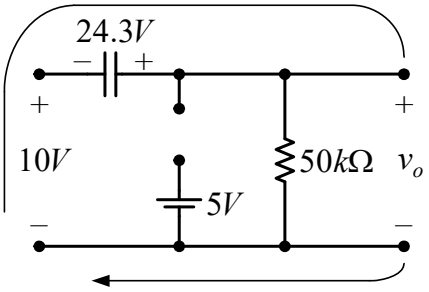


Fig. 4-3

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o, and applying KVL around the outside loop of circuit will result in

$$+10 + 24.3 - v_o = 0 \quad \Rightarrow \quad v_o = 34.3 \text{ V}.$$

The resulting output appears in Fig. 4-4, where the input and the output swing are the same.

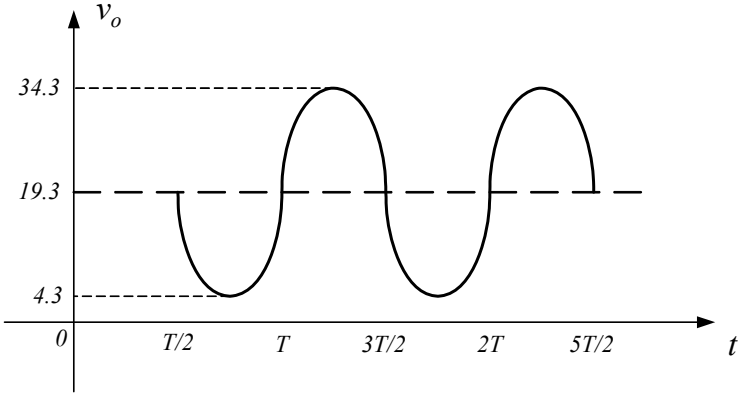


Fig. 4-4

Example 4-2:

Using silicon diode, design a clamper circuit that will produce output $v_o = 10Sin\omega t - 5$ V when the input is $v_i = 10Sin\omega t + 5$ V. Draw the circuit diagram and the input and output signals.

Solution:

From the input (v_i) and output (v_o) signals, we have a negative biased clamper. Therefore, the diode is forward bias ("on" state) during the positive half period of the input signal (v_i). The output voltage (v_o) at this positive period can be determined by KVL in the output section of the circuit shown in Fig. 4-5.

$E + 0.7 - v_o = 0 \quad => \quad E = 5 - 0.7 = 4.3$ V.

For the input section KVL will result in

$15 - V_C - 5 = 0 \quad => \quad V_C = 10$ V.

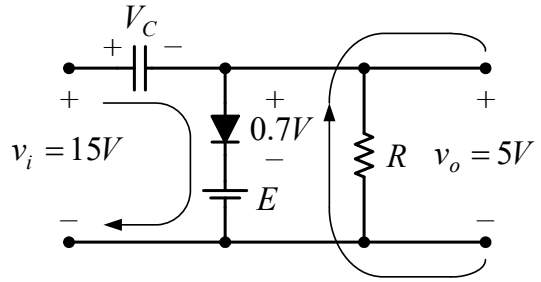


Fig. 4-5

The circuit diagram and the input and output signals are shown in Fig. 4-6.

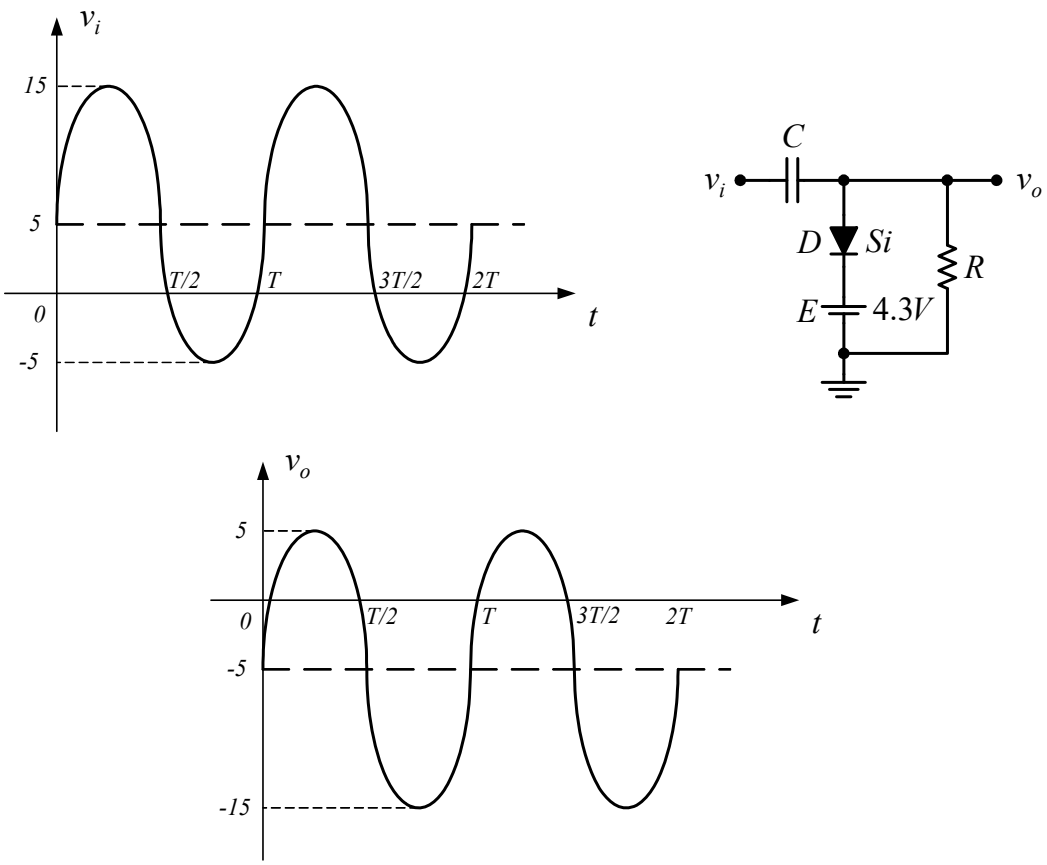
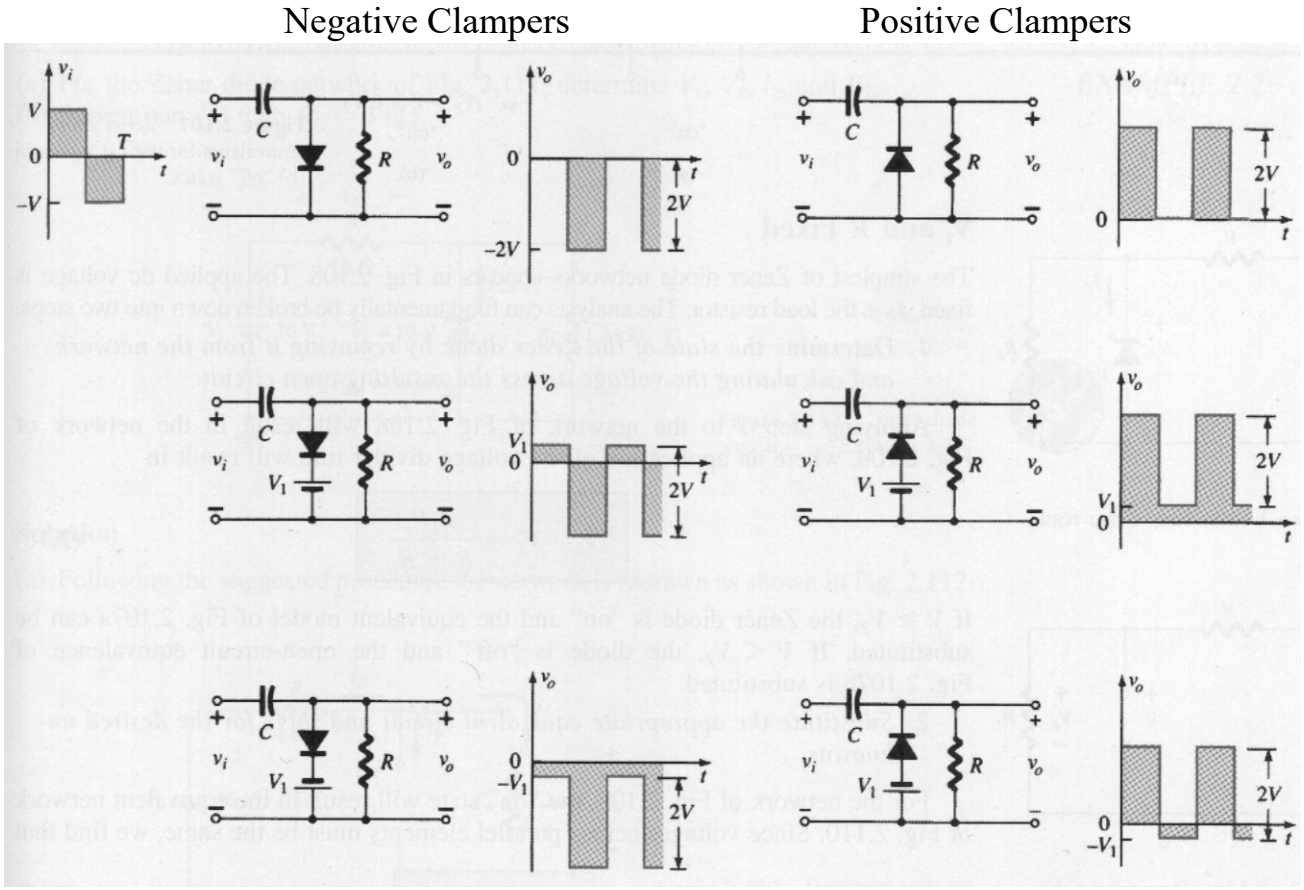


Fig. 4-6

Summary:

A number of clamping circuits and their effect on the square-wave input signal are shown in Fig. 4-7.



Clampers with ideal diodes and $5\tau = 5RC >> T/2$

Fig. 4-7

Exercise:

Sketch the output (v_o) for the circuit of Fig. 4-8 for the input (v_i) shown. Assume ideal diodes.

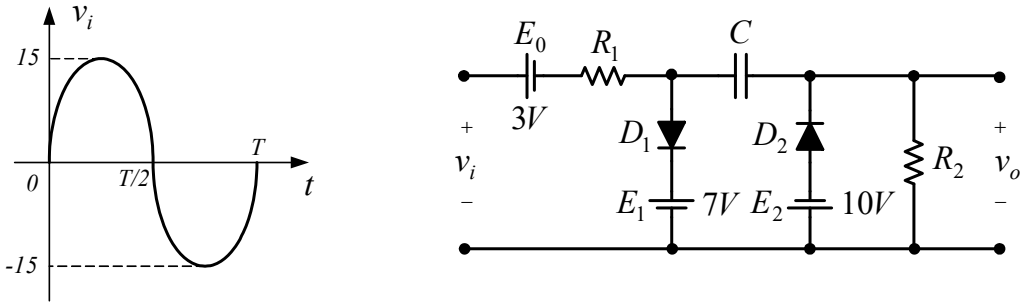


Fig. 4-8

Diode Rectifier Circuits

Basic Definition:

A diode circuit that converts an ac voltage to a pulsating dc voltage and permits current to flow in one direction only is called "***rectifier***" and the ac-to-dc conversion process is termed "***rectification***".

Half-Wave Rectifier (HWR):

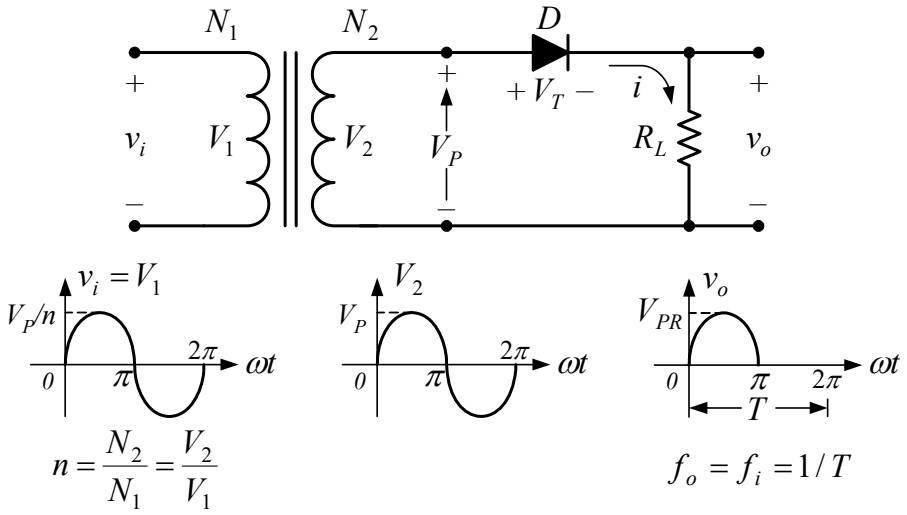


Fig. 5-1

For the half-wave rectifier circuit of Fig. 5-1:

◀ The average (dc) value of a half-wave rectified sine-wave voltage (V_{dc}) is

$$V_{dc} = \frac{1}{T}\int_0^T v_o(\omega t)\cdot d\omega t = \frac{1}{2\pi}\int_0^\pi V_{PR} Sin\,\omega t \cdot d\omega t = \frac{V_{PR}}{\pi}$$

For V_P close to V_T,

$$\boxed{V_{dc} = 0.318(V_P - V_T)} \qquad [5.1a]$$

For $V_P >> V_T$,

$$\boxed{V_{dc} = 0.318V_P} \qquad [5.1b]$$

◀ The root mean square (rms) value of the load voltage (V_{rms}) is

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v_o^2(\omega t)\cdot d\omega t} = \sqrt{\frac{1}{2\pi}\int_0^\pi V_{PR}^2 Sin^2\,\omega t \cdot d\omega t} = \frac{V_{PR}}{2}$$

For V_P close to V_T,

$$\boxed{V_{rms} = 0.5(V_P - V_T)} \qquad [5.2a]$$

For $V_P >> V_T$,

$$\boxed{V_{rms} = 0.5V_P} \qquad [5.2b]$$

◀ The rms value of the ac component (or ***the ripple voltage***) of the rectified signal [$V_r(rms)$] is

$$V_r(rms) = \sqrt{V_{rms}^2 - V_{dc}^2} = \sqrt{(0.5V_{PR})^2 - (0.318V_{PR})^2} = 0.385V_{PR}$$

For V_P close to V_T,

$$\boxed{V_r(rms) = 0.385(V_P - V_T)} \qquad [5.3a]$$

For $V_P >> V_T$,

$$\boxed{V_r(rms) = 0.385V_P} \qquad [5.3b]$$

◀ The percent ripple (r) in the rectified waveform (also called ***the ripple factor***) is

$$r = \frac{V_r(rms)}{V_{dc}} \times 100\% = \frac{0.385V_{PR}}{0.318V_{PR}} \times 100\% = 121\%$$

◀ Efficiency (η) = [$P_{dc}(load)$ / $P_{total}(circuit)$] × 100%

$$\eta = \frac{I_{dc}^2 R_L}{I_{rms}^2 (r_d + R_L)} \times 100\% = \frac{(0.318I_P)^2 R_L}{(0.5I_P)^2 (r_d + R_L)} \times 100\% = \frac{40.5}{1 + r_d / R_L}\%$$

For ideal diode ($r_d = 0\ \Omega$), $\eta = \eta_{max} = 40.5\ \%$

◀ The peak inverse voltage (PIV) of the diode is

$$\boxed{PIV = V_P} \qquad [5.4]$$

◀ The frequency of the output rectified signal (f_o) is

$$\boxed{f_o = f_i} \qquad [5.5]$$

Full-Wave Rectifiers (FWRs):

1. A Bridge Full-Wave Rectifier:

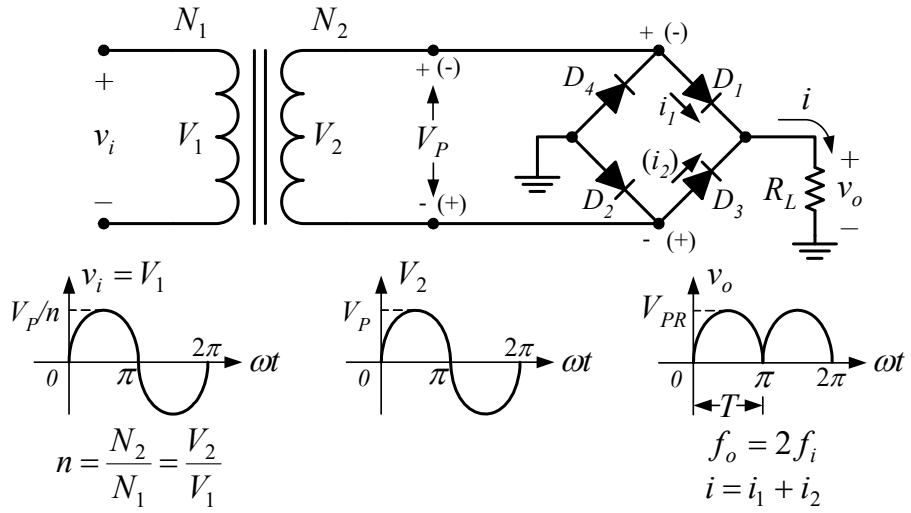


Fig. 5-2

For the bridge full-wave rectifier circuit of Fig. 5-2:

◀ $V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_{PR} Sin\omega t \cdot d\omega t = \frac{2V_{PR}}{\pi}$

For V_P close to $2V_T$,

$$\boxed{V_{dc} = 0.636(V_P - 2V_T)} \qquad [5.6a]$$

For $V_P >> 2V_T$,

$$\boxed{V_{dc} = 0.636V_P} \qquad [5.6b]$$

◀ $V_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} V_{PR}^2 Sin^2\omega t \cdot d\omega t} = \frac{V_{PR}}{\sqrt{2}}$

For V_P close to $2V_T$,

$$\boxed{V_{rms} = 0.707(V_P - 2V_T)} \qquad [5.7a]$$

For $V_P >> 2V_T$,

$$\boxed{V_{rms} = 0.707V_P} \qquad [5.7b]$$

◀ $V_r(rms) = \sqrt{V_{rms}^2 - V_{dc}^2} = \sqrt{(0.707V_{PR})^2 - (0.636V_{PR})^2} = 0.308V_{PR}$

For V_P close to $2V_T$,

$$\boxed{V_r(rms) = 0.308(V_P - 2V_T)} \qquad [5.8a]$$

For $V_P >> 2V_T$,

$$\boxed{V_r(rms) = 0.308V_P} \qquad [5.8b]$$

◀ $r = \frac{V_r(rms)}{V_{dc}} \times 100\% = \frac{0.308V_{PR}}{0.636V_{PR}} \times 100\% = 48.4\%$

◀ $\eta = \frac{I_{dc}^2 R_L}{I_{rms}^2(2r_d + R_L)} \times 100\% = \frac{(0.636I_P)^2 R_L}{(0.707I_P)^2(2r_d + R_L)} \times 100\% = \frac{81}{1 + 2r_d / R_L}\%$

For ideal diode ($r_d = 0\ \Omega$), $\eta = \eta_{max} = 81\ \%$

◀ $\boxed{PIV = V_P - 2V_T}$ [5.9]

◀ $\boxed{f_o = 2f_i}$ [5.10]

2. A Center-Tapped (CT) Full-Wave Rectifier:

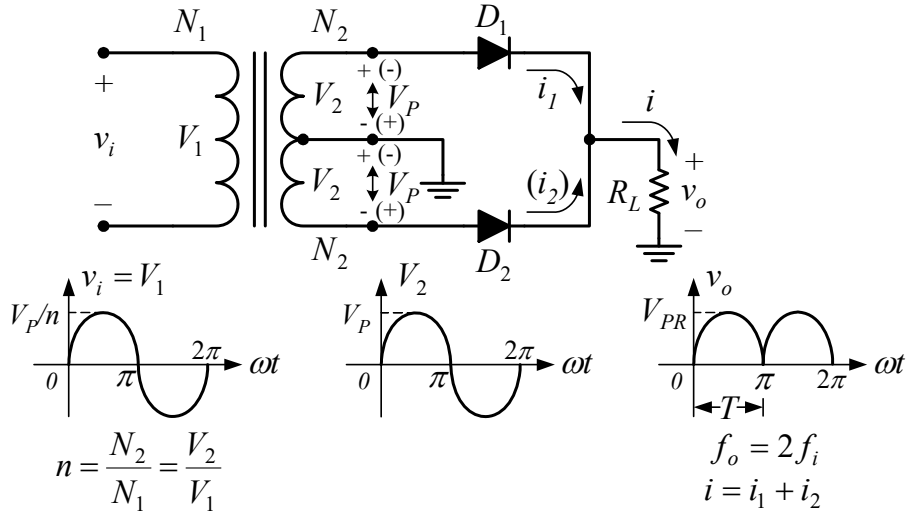


Fig. 5-3

For the center-tapped full-wave rectifier circuit of Fig. 5-3:

◀ $$V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_{PR} Sin\omega t \cdot d\omega t = \frac{2V_{PR}}{\pi}$$

For V_P close to V_T,

$$\boxed{V_{dc} = 0.636(V_P - V_T)} \qquad [5.11a]$$

For $V_P >> V_T$,

$$\boxed{V_{dc} = 0.636V_P} \qquad [5.11b]$$

◀ $$V_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} V_{PR}^2 Sin^2\omega t \cdot d\omega t} = \frac{V_{PR}}{\sqrt{2}}$$

For V_P close to V_T,

$$\boxed{V_{rms} = 0.707(V_P - V_T)} \qquad [5.12a]$$

For $V_P >> V_T$,

$$\boxed{V_{rms} = 0.707V_P} \qquad [5.12b]$$

◀ $$V_r(rms) = \sqrt{V_{rms}^2 - V_{dc}^2} = \sqrt{(0.707V_{PR})^2 - (0.636V_{PR})^2} = 0.308V_{PR}$$

For V_P close to V_T,

$$\boxed{V_r(rms) = 0.308(V_P - V_T)} \qquad [5.13a]$$

For $V_P >> V_T$,

$$\boxed{V_r(rms) = 0.308V_P} \qquad [5.13b]$$

◀ $$r = \frac{V_r(rms)}{V_{dc}} \times 100\% = \frac{0.308V_{PR}}{0.636V_{PR}} \times 100\% = 48.4\%$$

◀ $$\eta = \frac{I_{dc}^2 R_L}{I_{rms}^2 (r_d + R_L)} \times 100\% = \frac{(0.636I_P)^2 R_L}{(0.707I_P)^2 (r_d + R_L)} \times 100\% = \frac{81}{1 + r_d / R_L}\%$$

For ideal diode ($r_d = 0\ \Omega$), $\eta = \eta_{max} = 81\ \%$

◀ $$\boxed{PIV = 2V_P - V_T}$$ [5.14]

◀ $$\boxed{f_o = 2f_i}$$ [5.15]

Summary:

Different parameters for the HWR and FWR circuits are listed in Table 5-1.

Table 5-1

Parameter	HWR	FWR	
		Bridge	CT
V_{PR}	$V_P - V_T$	$V_P - 2V_T$	$V_P - V_T$
V_{dc}	$0.318V_{PR}$	$0.636V_{PR}$	
V_{rms}	$0.5V_{PR}$	$0.707V_{PR}$	
V_r	$0.385V_{PR}$	$0.308V_{PR}$	
r	121%	48.4%	
η_{max}	40.5%	81%	
PIV	V_P	$V_P - 2V_T$	$2V_P - V_T$
f_o	f_i	$2f_i$	

Example 5-1:

The input voltage to a full-wave rectifier employing a center-tapped step-down transformer and two silicon diodes is 220 V rms, and the transformer has turns ratio n = 0.125. Draw the rectifier circuit diagram when it is connected to a 100 Ω load, and find

1. the average value of the voltage across the load.
2. the average power dissipated by the load, and
3. the minimum *PIV* rating required for each diode.

Solution:

The rectifier circuit diagram is shown in Fig. 5-4.

1. $V_P = \sqrt{2} v_i n = \sqrt{2} * 220 * 0.125 = 38.9V.$
   $V_{dc} = 0.636(V_P - V_T) = 0.636(38.9 - 0.7) = 24.3V.$

2. $V_{rms} = 0.707(V_P - V_T) = 0.707(38.9 - 0.7) = 27.0V.$
   $P_{av} = \dfrac{V_{rms}^2}{R_L} = \dfrac{(27.0)^2}{100} = 7.3W.$

3. $PIV \geq (2V_P - V_T) = (2 * 38.9 - 0.7) = 77.1V.$

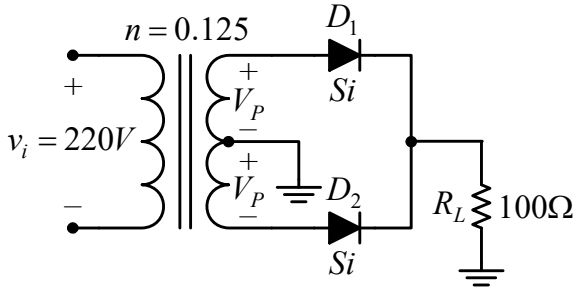
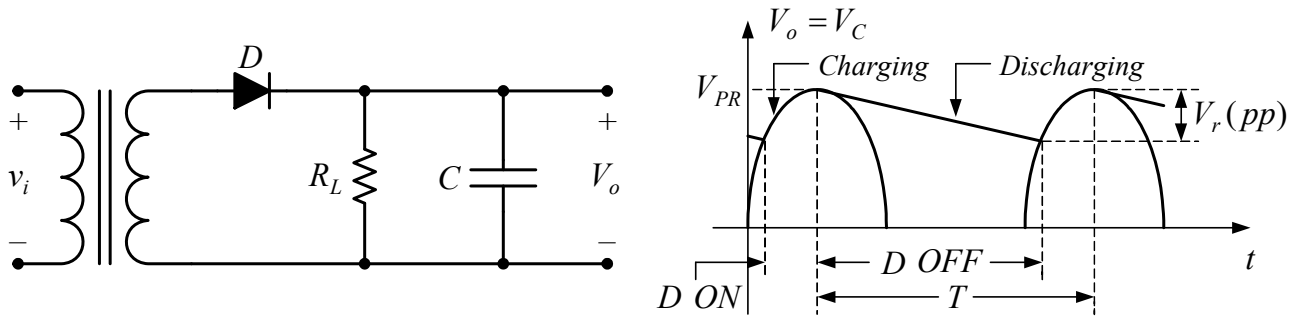


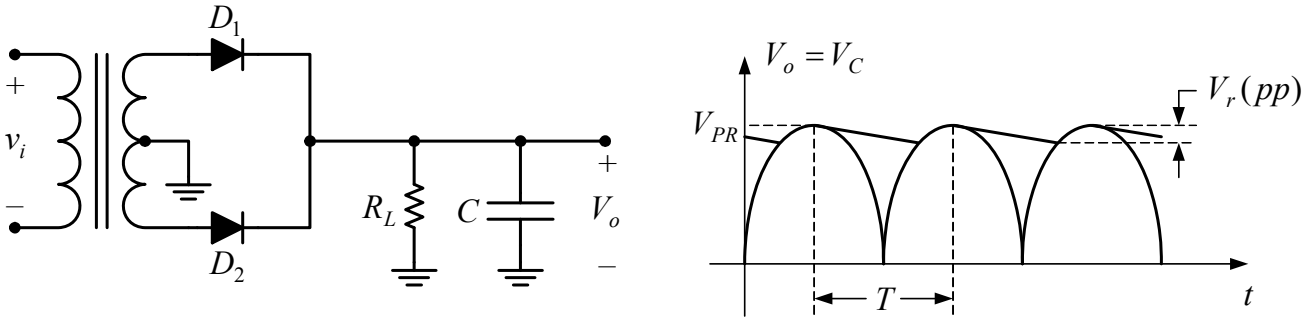
Fig. 5-4

Capacitor Filters:

A low-pass filter is connected across the output of a rectifier to suppress the ac components and to pass the dc component. A rudimentary low-pass filter used in power supplies consists simply of a capacitor (C) connected across the rectifier output, that is, in parallel with the load (R_L), as illustrated in Fig. 5-5.



Half-wave rectifier with capacitor filter



Full-wave rectifier with capacitor filter

Fig. 5-5

Operation:

- During the positive first quarter-cycle of the input, the diode is forward-biased (when $V_i > V_C$), allowing the capacitor to charge quickly to within a diode drop of the input peak (V_{PR}).
- When the input begins to decrease below its peak, the capacitor retain its charge and the diode becomes reverse-biased (when $V_C > V_i$).
- During the remaining part of the cycle, capacitor C can discharge slowly only through load resistance R_L at a rate determine by R_LC time constant (τ).
- The voltage fluctuation in the filtered waveforms is called the peak-to-peak ripple voltage [$V_r(pp)$]. In general, $V_r(pp)$ in FWR is smaller than it is in HWR for same R_L and C values (see Fig. 5-5).

Ripple of a Capacitor Filter:

We will now derive an expression for the ripple in the output of a rectifier having a capacitor filter (C) and load resistance (R_L). The derivation that follows is applicable to both HWR and FWR. We can assume that the ripple voltage in a ***lightly loaded filter*** (R_LC time constant (τ) is large) is a sawtooth wave as illustrated in Fig. 5-6.

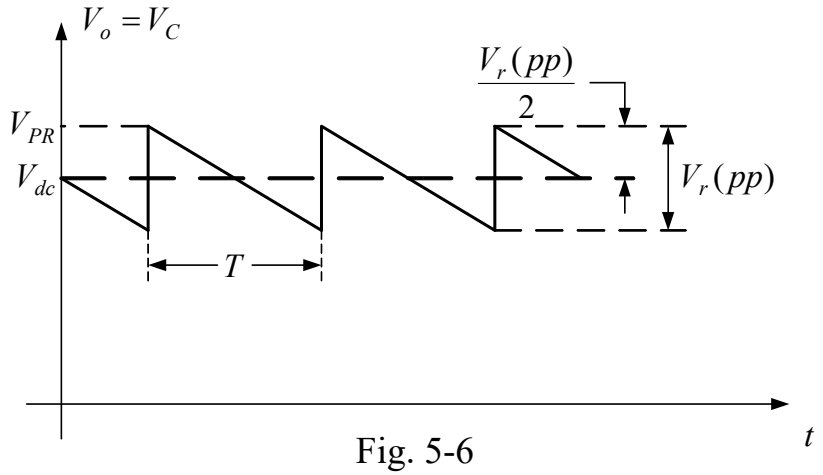


Fig. 5-6

This approximation is equivalent to assuming that the capacitor charges instantaneously and that its voltage decays linearly, instead of exponentially. Assuming that the voltage decays linearly is equivalent to assuming that the discharge current (I) is constant and equal to $I = V_{dc} / R_L$ where V_{dc} is the dc value of the filtered waveform. The total charge in capacitor voltage is $V_r(pp)$ volts, and this charge occurs over the period of time T. Therefore, since $\Delta Q = I.\Delta t$,

$$V_r(pp) = \frac{\Delta Q}{C} = \frac{(V_{dc} / R_L)T}{C}$$

Since $T=1/f_r$, where f_r is the frequency of the fundamental component of the ripple, that is, $f_r = f_o = f_i$ for HWR and $f_r = f_o = 2f_i$ for FWR. So that

$$\boxed{V_r(pp) = \frac{V_{dc}}{f_r R_L C}} \qquad [5.16]$$

or

$$\boxed{V_{dc} = V_r(pp) \cdot f_r R_L C} \qquad [5.17]$$

From Fig. 5-6, it is apparent that

$$V_{dc} = V_{PR} - \frac{V_r(pp)}{2}$$

Subsuming from Eq. [5.16], we obtain

$$V_{dc} = V_{PR} - \frac{V_{dc}}{2 f_r R_L C}$$

Solving for V_{dc}, we obtain an expression for the dc voltage (V_{dc}) in terms of the peak rectifier voltage (V_{PR}):

$$\boxed{V_{dc} = \frac{V_{PR}}{1 + \frac{1}{2 f_r R_L C}}} \qquad [5.18]$$

The rms value of a sawtooth waveform having peak-to-peak value $V_r(pp)$ is known to be

$$\boxed{V_r(rms) = \frac{V_r(pp)}{2\sqrt{3}}} \qquad [5.19]$$

Therefore, from Eqs. [5.17] and [5.19], the percent ripple is

$$r = \frac{V_r(rms)}{V_{dc}} \times 100\% = \frac{V_r(pp)/(2\sqrt{3})}{V_r(pp) f_r R_L C} \times 100\%$$

$$\boxed{r = \frac{1}{2\sqrt{3} f_r R_L C} \times 100\%} \qquad [5.20]$$

Equation [5.20] confirms our analysis of the capacitor filter: a large $R_L C$ time constant (τ) results in a small ripple voltage, and vice versa. The light-load assumption on which our derivation is based is generally valid for percent ripple (r) less than 6.5%. From a design standpoint, the values of f_r and R_L, are usually fixed, and the designer's task is to select a value of C that keeps the ripple below a prescribed value.

Example 5-2:

A full-wave rectifier is operated from a 50 Hz line and has a filter capacitor connected across its output. What minimum value of capacitance is required if the load is 1.2 kΩ and the ripple must be no greater than 2.4%?

Solution:

$$r = \frac{1}{2\sqrt{3} f_r R_L C} \times 100\%$$

$$0.024 = \frac{1}{2\sqrt{3} * 2 * 50 * 1.2 * 10^3 * C} \Rightarrow$$

$$C \geq 100 \mu F.$$

Exercises:

1. A full-wave bridge rectifier isolated from the 220 V rms power line by a transformer. Assuming the diode voltage drops are 0.7 V.
   i. What turns ratio should the transformer have in order to produce an average current of 1 A in a 10 Ω load?
   ii. What is the average current in each diode under the conditions of (i)?
   iii. What minimum *PIV* rating should each diode have?
   iv. How much power is dissipated by each diode?

2. A full-wave bridge rectifier is operated from a 50 Hz, 220 V rms line. It has a 100 μF filter capacitor and a 2 k Ω load. Neglect diode voltage drops.
   i. What is the percent ripple?
   ii. What is the average current in the load?

Voltage-Multiplier Circuits

Basic Concepts:

Diodes and capacitors can be connected in various configurations to produce filtered, rectified voltages that are integer multiples of the peak value of an input sine wave. The principle of operation of these circuits is similar to that of the clamping circuits discussed previously. By using a transformer to change the amplitude of an ac voltage before it is applied to a voltage multiplier, a wide range of dc levels can be produced using this technique. One advantage of a voltage multiplier is that high voltages can be obtained without using a high-voltage transformer.

Voltage Doubler:

1. Half-Wave Voltage Doubler:

Figure 6-1 shows a half-wave voltage doubler circuit.

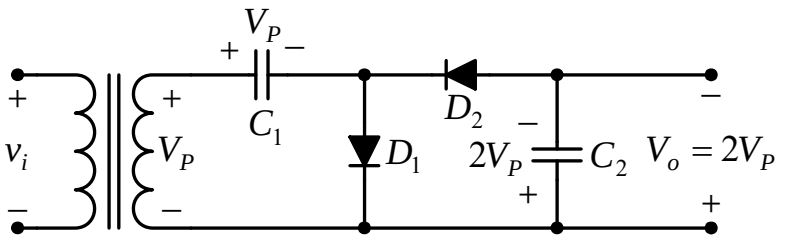


Fig. 6-1

Operation:

- During the positive half-cycle,
  D_1 ON and D_2 OFF => Charging C_1 up to V_P.
- During the negative half-cycle,
  D_2 ON and D_1 OFF => Charging C_2 to $2V_P$.
- The output (V_o) of the half-wave voltage doubler is

$$\boxed{V_o = V_{C_2} = |2V_P|} \qquad [6.1]$$

If a load is connected to the output of the half-wave voltage doubler, the voltage across capacitor C_2 drops during the positive half-cycle (at the input) and the capacitor is recharged up to $2V_P$ during the negative half-cycle. The output waveform across capacitor C_2 is that of a half-wave signal filtered by a capacitor filter.

The peak inverse voltage (*PIV*) rating of each diode in the half-wave voltage doubler circuit must be at least $2V_P$.

2. Full-Wave Voltage Doubler:

Figure 6-2 shows a full-wave voltage doubler circuit.

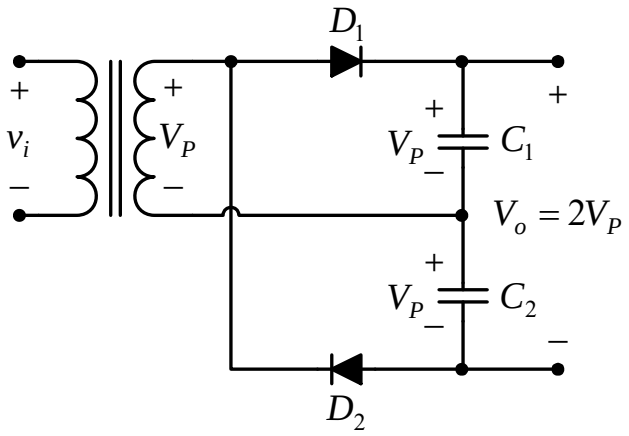


Fig. 6-2

Operation:

- During the positive half-cycle,
  D_1 ON and D_2 OFF => Charging C_1 up to V_P.
- During the negative half-cycle,
  D_2 ON and D_1 OFF => Charging C_2 up to V_P.
- The output (V_o) of the full-wave voltage doubler is

$$\boxed{V_o = V_{C_1} + V_{C_2} = 2V_P} \qquad [6.2]$$

If load current is drawn from the full-wave voltage doubler circuit, the voltage across the capacitors C_1 and C_2 is the across a capacitor fed by a full-wave rectifier. One difference is that of C_1 and C_2 in series, which is less than capacitance of either C_1 and C_2 alone. The lower capacitor value will provide poorer filtering action than the single-capacitor filter circuit.

The peak inverse voltage across each diode is $2V_P$, as it is for filter capacitor circuit.

Voltage Tripler and Quadrupler:

Figure 6-3 shows an extension of the half-wave voltage doubler, which develops three and four times the peak input voltage. It should be obvious from the pattern of the circuit connection how additional diodes and capacitors may be connected so that the output voltage may also be five, six, seven, and so on, times the basic peak voltage (V_P).

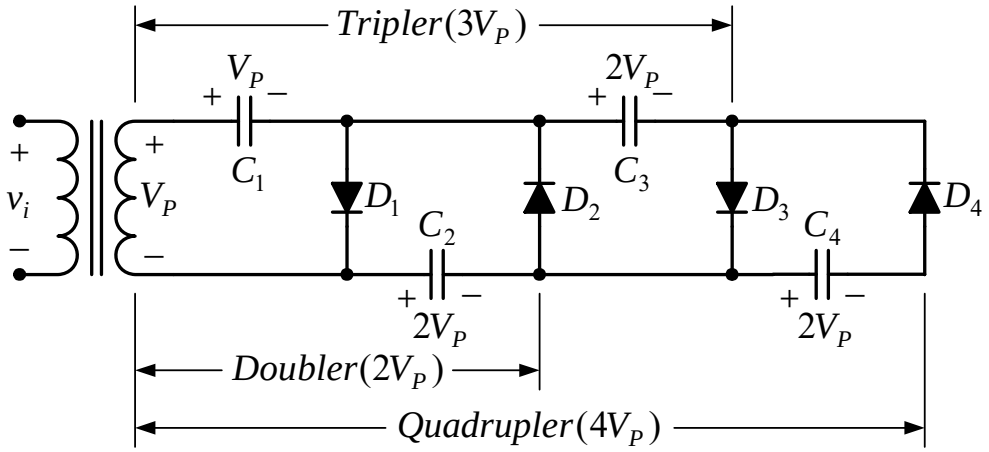


Fig. 6-3

Operation:

- During the positive half-cycle,
  D_1 ON and D_2, D_3, D_4 OFF => Charging C_1 up to V_P.
- During the negative half-cycle,
  D_2 ON and D_1, D_3, D_4 OFF => Charging C_2 to $2V_P$.
- During the next positive half-cycle,
  D_1, D_3 ON and D_2, D_4 OFF => C_2 charges C_3 to $2V_P$.
- During the next negative half-cycle,
  D_2, D_4 ON and D_1, D_3 OFF => C_3 charges C_4 to $2V_P$.
- The voltage across the combination of C_1 and C_3 is $3V_P$ and that across C_2 and C_4 is $4V_P$.

The *PIV* rating of each diode in the circuit must be at least $2V_P$.

Exercises:

1. A certain voltage doubler has 35 V *rms* on its input. What is the output voltage? Sketch the circuit, indicating the output terminals and *PIV* for the diode.

2. Repeat Exercise 1 for a voltage tripler and quadrupler.

3. The output voltage of a quadrupler is 620 V. What minimum *PIV* rating must each diode have?

Zener Diodes and Applications

Zener Diodes:

Diodes which are designed with plate power-dissipation capabilities to operate in the breakdown region may be employed as voltage-reference or constant-voltage devices. Such are known as ***avalanche***, ***breakdown***, or ***zener diodes***. The zener diode is made for operation in the breakdown region. By varying the doping level, a manufacturer can produce zener diodes with breakdown voltages from about 2 to 250 V.

When the applied reverse voltage reaches the breakdown value, minority carries in the depletion layer are accelerated and reach high enough velocities to dislodge valence electrons from outer orbits. The newly liberated electrons can then gain high enough velocities to free other valence electrons. In this way, we get an avalanche of free electrons. Avalanche occurs for reverse voltages greater than 6 V or so.

The zener effect is different. When a diode is heavily doped, the depletion layer is very narrow. Because of this, the electric field across the depletion layer is very intense. When the field strength reaches approximately 3×10^7 V/m, the field is intense enough to pull electrons out of valence orbits. The creation of free electrons in this way is called zener breakdown (also known as high-field emission).

The zener effect is predominant for breakdown voltages less than 4 V, the avalanche effect is predominant for breakdown voltages greater than 6 V, and both effects are present between 4 and 6 V. Originally, people thought the zener effect was the only breakdown mechanism in diodes. For this reason, the name "zener diode" came into widespread use before the avalanche effect was discovered. All diodes optimized for operation in the breakdown region are therefore still called zener diodes.

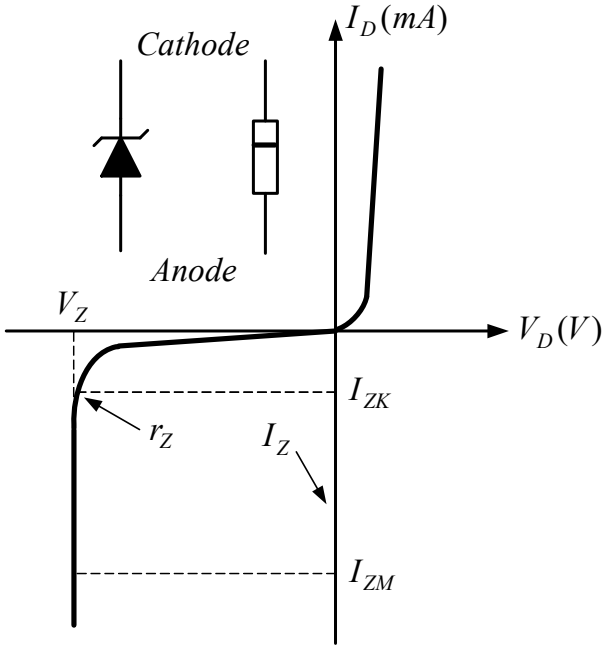


Fig. 7-1

Fig. 7-1 shows the schematic symbol and the current-voltage curve of a zener diode. Negligible reverse current flows until we reach the breakdown voltage V_Z. In a zener diode, the breakdown has a very sharp knee, followed by an almost vertical increase in current. Note that the voltage is approximately constant, equal to V_Z over most of the breakdown region. Data sheets usually specify the value of V_Z at a particular knee current I_{ZK} which is beyond the knee (see Fig. 7-1).

The power dissipation of a zener diode equals the product of its voltage and current. In symbols,

$$P_Z = V_Z \cdot I_Z$$

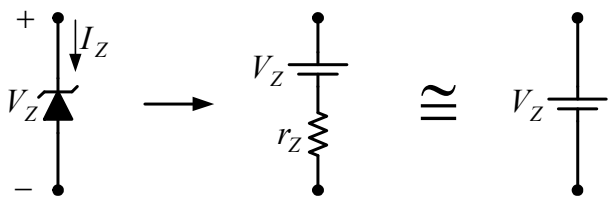
As long as P_Z is less than the power rating $P_{Z(max)}$, the zener diode will not be destroyed. Commercially available zener diodes have power ratings from 0.25 W to more than 50 W. Data sheets often specify the maximum current a zener diode can handle without exceeding its power rating. This maximum current is designated I_{ZM} (see Fig. 7-1). The relation between I_{ZM} and power rating is given by

$$\boxed{I_{ZM} = \frac{P_{Z(\max)}}{V_Z}} \qquad [7.1]$$

When a zener diode is operating in the breakdown region, a small increase in voltage produces a large increase in current. This implies that a zener diode has a small dynamic resistance (r_Z, see Fig. 7-1). We can calculate this zener resistance by

$$r_Z = \frac{\Delta v}{\Delta i}$$

The complete equivalent circuit of the zener diode in the zener region includes a small dynamic resistance (r_Z) and dc battery equal to the zener potential (V_Z), as shown in Fig. 7-2a. For all applications to follow, however, we shall assume as a first approximation that the external resistors are much larger in magnitude than the zener-equivalent resistor and that the equivalent circuit is simply the dc battery that equal to V_Z as indicated in Fig. 7-2b.



(a) (b)

Fig. 7-2

Zener Diode Applications:

1. AC Voltage Regulators (Limiters or Clippers):

Two back-to-back zeners can be used as an ac regulator or a simple square-wave generator as shown in Examples 7-1 and 7-2 respectively.

Example 7-1:

Sinusoidal ac regulator, see Fig. 7-3.

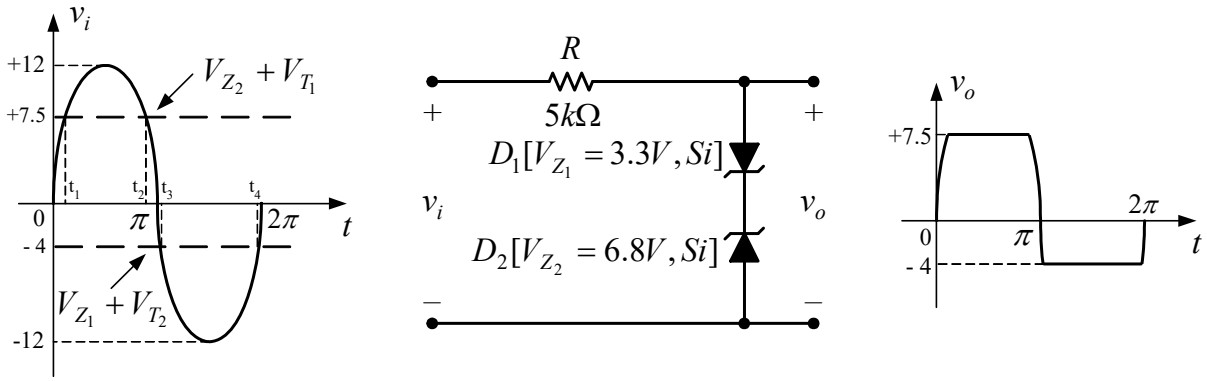


Fig. 7-3

For $t = 0 \rightarrow t_1$ and $t_2 \rightarrow \pi$; D_1 ON and D_2 OFF => $v_o = v_i$.
For $t = t_1 \rightarrow t_2$; D_1 ON and D_2 BREAKDOWN => $v_o = V_{Z_2} + V_{T_1}$.
For $t = \pi \rightarrow t_3$ and $t_4 \rightarrow 2\pi$; D_2 ON and D_1 OFF => $v_o = v_i$.
For $t = t_3 \rightarrow t_4$; D_2 ON and D_1 BREAKDOWN => $v_o = V_{Z_1} + V_{T_2}$.

Example 7-2:

Simple square-wave generator, see Fig. 7-4.

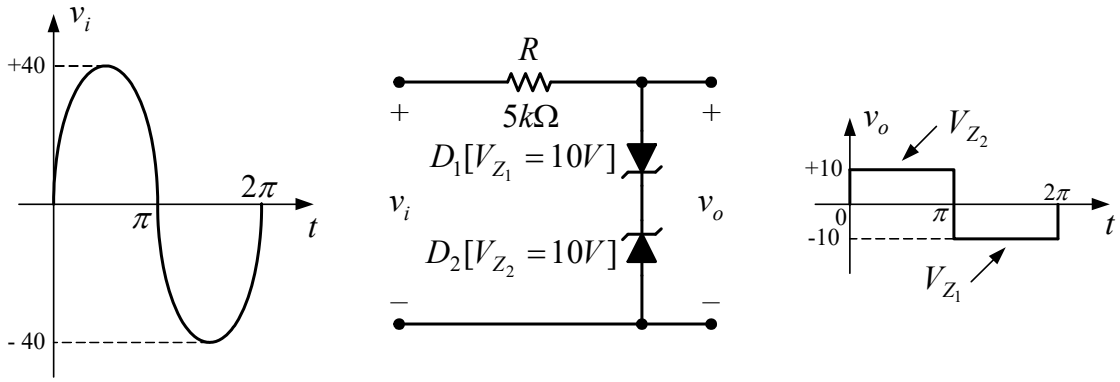


Fig. 7-4

2. DC Voltage Reference:

Two or more reference levels can be established by placing zener diodes in series as shown in Fig. 7-5. As long as V_i is grater than the sum of V_{Z_1} and V_{Z_2}, both diodes will be in the breakdown state and the three reference voltages will be available.

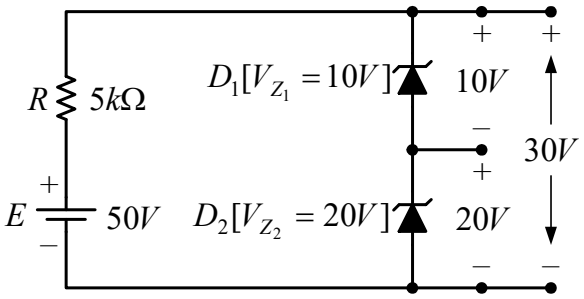


Fig. 7-5

3. DC Voltage Regulators:

a. Fixed R_L, Variable V_i:

For the regulator circuit shown in Fig. 7-6;

$$I_L = \frac{V_Z}{R_L} \ (Constant) \qquad [7.2a]$$

$$I_{S(\min)} = I_{ZK} + I_L$$
$$V_{i(\min)} = I_{S(\min)} R_S + V_Z \qquad [7.2b]$$

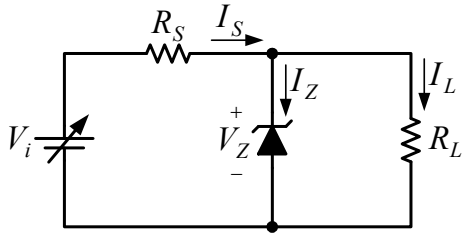


Fig. 7-6

$$I_{S(\max)} = I_{ZM} + I_L$$
$$V_{i(\max)} = I_{S(\max)} R_S + V_Z \qquad [7.2c]$$

b. Fixed V_i, Variable R_L:

For the regulator circuit shown in Fig. 7-7;

$$I_S = \frac{V_i - V_Z}{R_S} \ (Constant) \qquad [7.3a]$$

$$I_{L(\min)} = I_S - I_{ZM}$$
$$R_{L(\max)} = \frac{V_Z}{I_{L(\min)}} \qquad [7.3b]$$

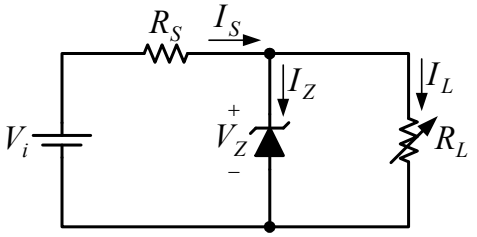


Fig. 7-7

$$I_{L(\max)} = I_S - I_{ZK}$$
$$R_{L(\min)} = \frac{V_Z}{I_{L(\max)}} \qquad [7.3c]$$

c. Variable V_i and R_L:

For the regulator circuit shown in Fig. 7-8;

$$I_{ZK} = I_{S(\min)} - I_{L(\max)}$$
$$I_{S(\min)} = \frac{V_{i(\min)} - V_Z}{R_S} \qquad [7.4a]$$
$$I_{L(\max)} = \frac{V_Z}{R_{L(\min)}}$$

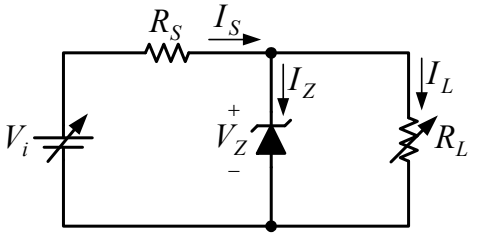


Fig. 7-8

$$I_{ZM} = I_{S(\max)} - I_{L(\min)}$$
$$I_{S(\max)} = \frac{V_{i(\max)} - V_Z}{R_S} \qquad [7.4b]$$
$$I_{L(\min)} = \frac{V_Z}{R_{L(\max)}}$$

Example 7-3:

The reverse current in a certain 12 V, 2.4 W zener diode must be at least 5 mA to ensure that the diode remains in breakdown. The diode is to be used in the regulator circuit shown in Fig. 7-9, where V_i can vary from 18 V to 24 V. Find a suitable value for R_S and the minimum rated power dissipation that R_S should have.

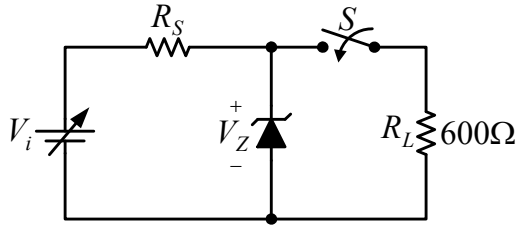


Fig. 7-9

Solution:

$I_{ZK} = 5mA$ and $I_{ZM} = \dfrac{P_Z}{V_Z} = \dfrac{2.4}{12} = 200mA.$

$I_{L(\min)} = 0A$ (when the switch S is open, $R_L = R_{L(\max)} = \infty\Omega$).

$I_{L(\max)} = \dfrac{V_Z}{R_{L(\min)}} = \dfrac{12}{600} = 20mA$ (when the switch S is closed, $R_L = R_{L(\min)} = 600\Omega$).

$I_{ZK} = I_{S(\min)} - I_{L(\max)} \quad => \quad 5*10^{-3} = I_{S(\min)} - 20*10^{-3} \quad => \quad I_{S(\min)} = 25mA.$

$I_{ZM} = I_{S(\max)} - I_{L(\min)} \quad => \quad 200*10^{-3} = I_{S(\max)} - 0 \quad => \quad I_{S(\max)} = 200mA.$

$$R_{S(\max)} = \frac{V_{i(\min)} - V_Z}{I_{S(\min)}} = \frac{18-12}{25*10^{-3}} = 240\Omega.$$

$$R_{S(\min)} = \frac{V_{i(\max)} - V_Z}{I_{S(\max)}} = \frac{24-12}{200*10^{-3}} = 60\Omega.$$

Thus, we require $60\Omega \le R_S \le 240\Omega$.

Choosing or calculating $R_S = \sqrt{R_{S(\min)} \cdot R_{S(\max)}} = \sqrt{60*240} = 120\Omega.$

$$I_{S(\max)} = \frac{V_{i(\max)} - V_Z}{R_S} = \frac{24-12}{120} = 100mA.$$

$$P_{R_S} \ge I^2_{S(\max)} \cdot R_S = \left(100*10^{-3}\right)^2 * 120 = 1.2W.$$

Exercises:

1. Sketch the output (v_o) for the circuit of Fig. 7-10 for the input shown (v_i) when $|V_m|$ equal to (i) 5 V, and (ii) 15 V.

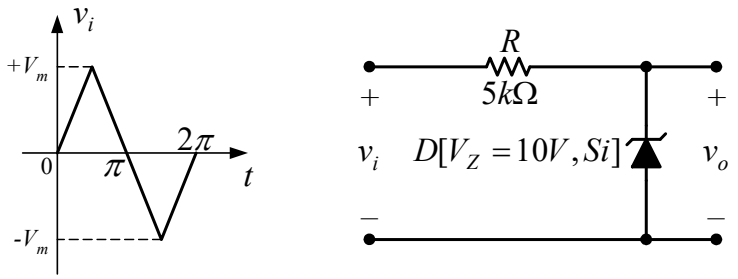


Fig. 7-10

2. Design the voltage regulator circuit of Fig. 7-11 to maintain V_L at 12 V across R_L with V_i that will vary between 16 and 20 V. That is, determine the proper value of R_S and the power rating of the zener diode (P_Z).

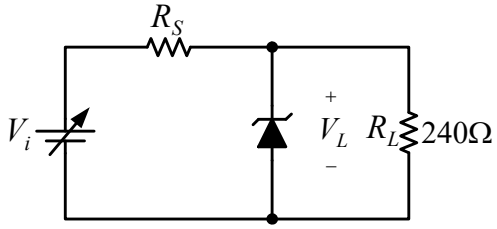


Fig. 7-11

3. The 6-V zener diode in Fig. 7-12 has a maximum rated power dissipated of 690 mW. Its reverse current must be at least 3 mA to keep it in breakdown. Find a suitable value for R_S if V_i can vary from 9 V to 12 V and R_L can vary from 500 Ω to 1.2 kΩ.

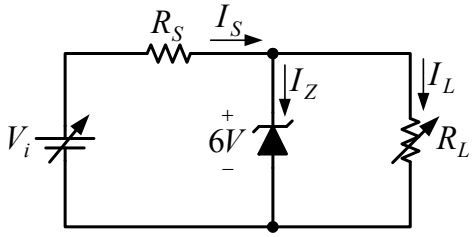


Fig. 7-12

4. If R_S in Exercise 3 is set equal to its maximum permissible value, what is the maximum permissible value of V_i?

5. If R_S in Exercise 3 is set equal to its minimum permissible value, what is the minimum permissible value of R_L?

6. If R_S in Exercise 3 is set equal to 120 Ω, what is the minimum rated power dissipated that R_S should have?