4. Voltage-Feedback Bias Circuit:

Fig. 9-7a shows a voltage-feedback bias circuit.

Analysis:

◀ For the input (base-emitter circuit) loop as shown in Fig. 9-7b:

$$+V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I'_C = I_C + I_B = I_E \cong I_C = \beta I_B$$

$$+V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

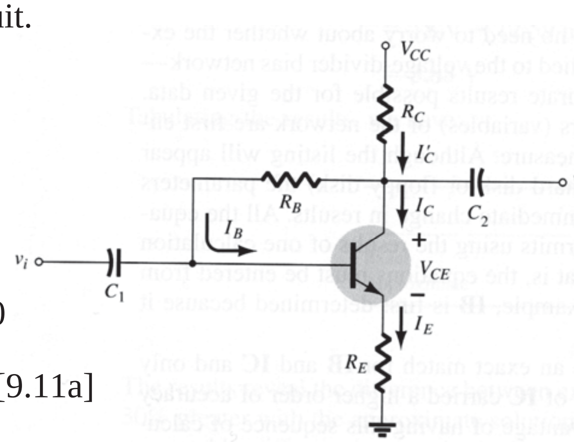
$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}} \qquad [9.11a]$$

◀ For the output (collector-emitter circuit) loop as shown in Fig. 9-7c:

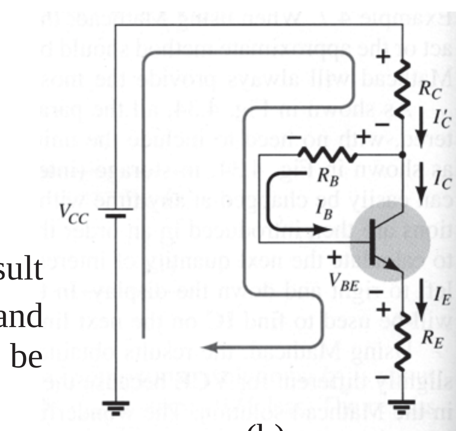
$$+I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

$$I'_C = I_E \cong I_C$$

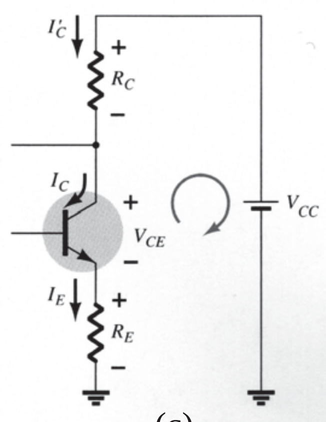
$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \qquad [9.11b]$$



(a)



(b)



(c)

Fig. 9-7

Load-Line Analysis:

Continuing with the approximation $I'_C = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The levels of I_{BQ} will be defined by the chosen base configuration.

Design:

For an optimum design:

$$\boxed{\begin{aligned} V_{CEQ} &= \frac{1}{2}V_{CC} \\ I_{CQ} &= \frac{1}{2}I_{C(sat)} = \frac{V_{CC}}{2(R_C + R_E)} \\ V_E &= \frac{1}{10}V_{CC} \\ R_B &\le \beta(R_C + R_E) \end{aligned}} \qquad [9\text{-}12]$$

Other Biasing Circuits:

Example 9-2: (*Negative Supply*)

Determine V_C and V_B for the circuit of Fig. 9-8.

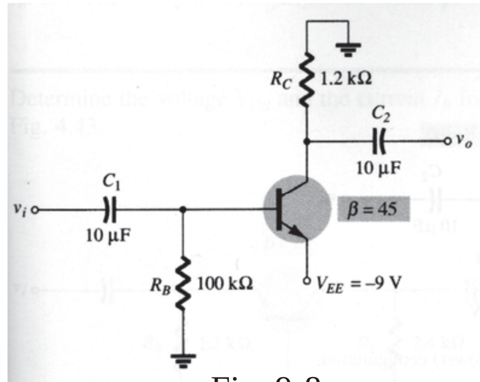


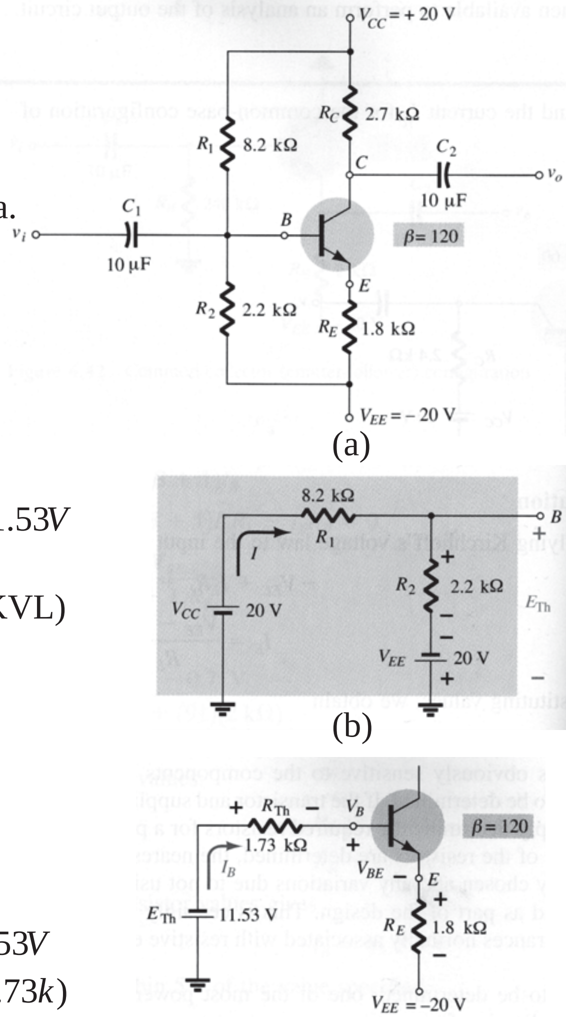
Fig. 9-8

Solution:

$$-I_B R_B - V_{BE} + V_{EE} = 0 \qquad \text{(KVL)}$$
$$I_B = \frac{V_{EE} - V_{BE}}{R_B} = \frac{9 - 0.7}{100k} = 83\mu A$$
$$I_C = \beta I_B = (45)(83\mu) = 3.735mA$$
$$V_C = -I_C R_C = -(3.735m)(1.2k) = -4.48V$$
$$V_B = -I_B R_B = -(83\mu)(100k) = -8.3V$$

Example 9-3: (*Two Supplies*)

Determine V_C and V_B for the circuit of Fig. 9-9a.



(a)

(b)

(c)

Fig. 9-9

Solution:

From Fig. 9-9b:

$$R_{Th} = R_1 \| R_2 = 8.2k \| 2.2k = 1.73k\Omega$$
$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20 + 20}{8.2k + 2.2k} = 3.85mA$$
$$E_{Th} = IR_2 - V_{EE} = (3.85m)(2.2k) - 20 = -11.53V$$

From Fig. 9-9c:

$$-E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E + V_{EE} = 0 \qquad \text{(KVL)}$$
$$I_E = (\beta + 1) I_B$$
$$I_B = \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$
$$= \frac{20 - 11.53 - 0.7}{1.73k + (121)(1.8k)} = 35.39\mu A$$
$$I_C = \beta I_B = (120)(35.39\mu) = 4.25mA$$
$$V_C = V_{CC} - I_C R_C = 20 - (4.25m)(2.7k) = 8.53V$$
$$V_B = -E_{Th} - I_B R_{Th} = -(11.53) - (35.39\mu)(1.73k)$$
$$= -11.59V$$

Example 9-4: (*Common-Base*)

Determine V_{CB} and I_B for the common-base configuration of Fig. 9-10.

Solution:

Applying KVL to the input circuit:

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{4 - 0.7}{1.2k} = 2.75mA$$

Applying KVL to the output circuit:

$$+V_{CB} + I_C R_C - V_{CC} = 0$$

$$V_{CB} = V_{CC} - I_C R_C$$

with $I_C \cong I_E$

$$V_{CB} = 10 - (2.75m)(2.4k) = 3.4V$$

$$I_B = \frac{I_C}{\beta} = \frac{2.75m}{60} = 45.8\mu A$$

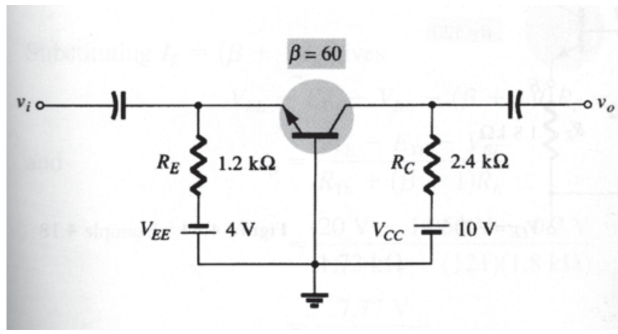


Fig. 9-10

Example 9-5: (*Common-Collector*)

Determine I_E and V_{CE} for the common-collector (emitter-follower) configuration of Fig. 9-11.

Solution:

Applying KVL to the input circuit:

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$I_E = (\beta + 1) I_B$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$= \frac{20 - 0.7}{240k + (91)(2k)} = 45.73\mu A$$

$$I_E = (\beta + 1) I_B = (91)(45.73\mu) = 4.16mA$$

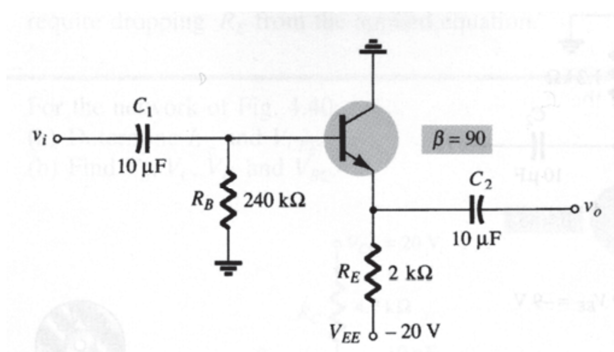


Fig. 9-11

Applying KVL to the output circuit:

$$-V_{EE} + I_E R_E + V_{CE} = 0$$

$$V_{CE} = V_{EE} - I_E R_E = 20 - (4.16m)(2k) = 11.68V$$

Example 9-6: (*PNP Transistor*)

Determine V_{CE} for the voltage-divider bias configuration of Fig. 9-12.

Solution:

Testing: $\beta R_E \geq 10R_2$

$$(120)(1.1k) \geq 10(10k)$$

$$132k\Omega \geq 100k\Omega (satisfied)$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(10k)(-18)}{47k + 10k} = -3.16V$$

$$V_E = V_B - V_{BE} = -3.16 - (-0.7) = -2.46V$$

$$I_C = I_E = \frac{V_E}{R_E} = \frac{2.46}{1.1k} = 2.24mA$$

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0 \quad \text{(KVL)}$$

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

$$= -18 + (2.24m)(2.4k + 1.1k) = -10.16V$$

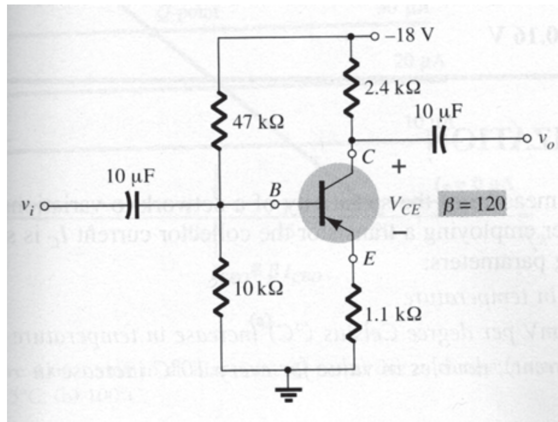
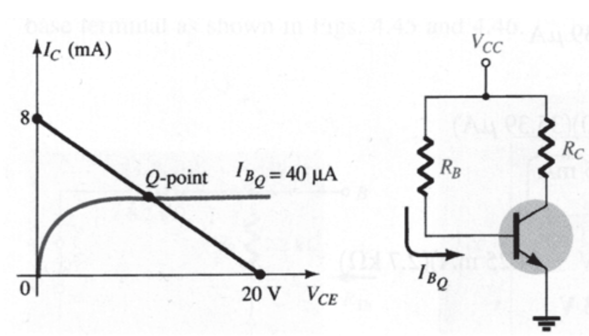


Fig. 9-12

Exercises:

1. For the fixed-biased configuration of Fig. 9-2a with the following parameters: V_{CC} = +12 V, β = 50, R_B = 240 kΩ, and R_C = 2.2 kΩ, determine: I_{BQ}, I_{CQ}, V_{CEQ}, V_B, V_C, and V_{BC}.

2. Given the device characteristics of Fig. 9-13a, determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 9-13b.



(a) (b)

Fig. 9-13

3. For the emitter bias circuit of Fig. 9-4a with the following parameters: V_{CC} = +20 V, β = 50, R_B = 430 kΩ, R_C = 2 kΩ, and R_E = 1 kΩ, determine: I_B, I_C, V_{CE}, V_C, V_E, V_B and V_{BC}.

4. Design an emitter-stabilized circuit (Fig. 9-4a) at I_{CQ} = 2 mA. Use V_{CC} = +20 V and an npn transistor with β =150.

5. Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig. 9-6a with the following parameters: V_{CC} = +18 V, β = 50, R_1 = 82 kΩ, R_2 = 22 kΩ, R_C = 5.6 kΩ, and R_E = 1.2 kΩ.

6. Design a beta-independent (voltage-divider) circuit to operate at V_{CEQ} = 8 V and I_{CQ} = 10 mA. Use a supply of V_{CC} = +20 V and an npn transistor with β = 80.

7. Determine the quiescent levels of I_{CQ} and V_{CEQ} for the voltage-feedback circuit of Fig. 9-7a with the following parameters: V_{CC} = +10 V, β = 90, R_B = 250 kΩ, R_C = 4.7 kΩ, and R_E = 1.2 kΩ.

8. Prove that $R_B \le \beta(R_C + R_E)$ is the required condition for an optimum design of the voltage-feedback circuit.

9. Prove mathematically that I_{CQ} for the voltage-feedback bias circuit is approximately independent of the value of beta.

10. Fig. 9-14 shows a three-stage circuit with a V_{CC} supply of +20 V. GND stands for ground. If all transistors have a β of 100, what are the I_C and V_{CE} of each stage?

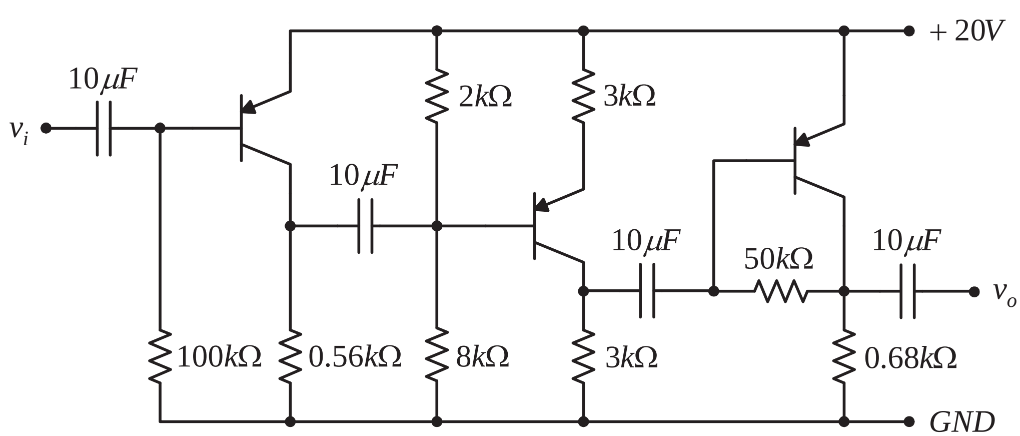


Fig. 9-14

Bias Stabilization

Basic Definitions:

The stability of system is a measure of sensitivity of a circuit to variations in its parameters. In any amplifier employing a transistor the ***collector current I_C*** is sensitive to each of the following parameters:

- ***I_{CO}* (*reverse saturation current*): *doubles in value for every 10°C increase in temperature.***
- ***$|V_{BE}|$* (*base-to-emitter voltage*): *decrease about 7.5 mV per 1°C increase in temperature.***
- ***β* (*forward current gain*): *increase with increase in temperature.***

Any or all of these factors can cause the bias point to drift from the design point of operation.

Stability Factors, $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$:

A stability factor, S, is defined for each of the parameters affecting bias stability as listed below:

$$\boxed{S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}} = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\beta=const.}} \qquad [10.1a]$$

$$\boxed{S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta=const.}} \qquad [10.1b]$$

$$\boxed{S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},V_{BE}=const.}} \qquad [10.1c]$$

Generally, networks that are quite stable and relatively insensitive to temperature variations have low stability factors. In some ways it would seem more appropriate to consider the quantities defined by Eqs. [10.1a - 10.1c] to be sensitivity factors because: the higher the stability factor, the more sensitive the network to variations in that parameter.

The total effect on the collector current can be determined using the following equation:

$$\boxed{\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta} \qquad [10.2]$$