Al-Mustaqbal University
Department of Medical Instrumentation Techniques Engineering
Class 2^{nd}
Subject: Electronic Circuits
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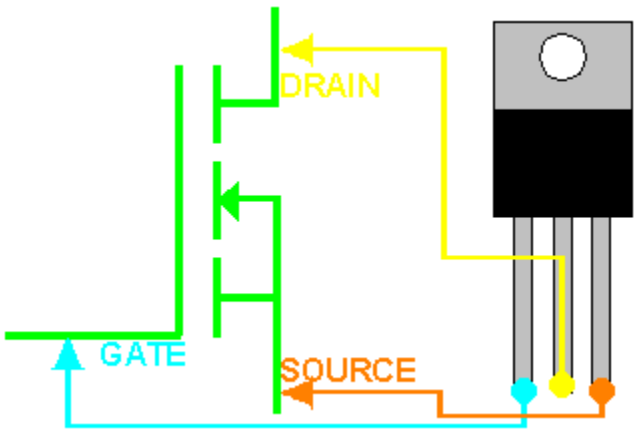
1st term – Lect. FET and MOSFET Biasing

Electronic Circuits

Lecture 8 (12^{th} Week)

FET And MOSFET Biasing



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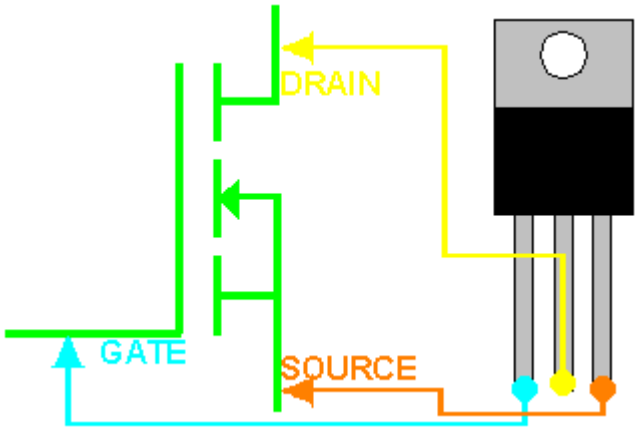
7.1. Introduction

Field-Effect Transistor (FET) Biasing is crucial to set the proper operating point in the active region for amplifier circuits. This ensures stable and predictable performance despite variations in transistor parameters or environmental changes. FET biasing methods differ slightly between JFETs and MOSFETs but share similar principles.



The Equation applicable of biasing is:

1. FET Biasing

$$I_G \cong 0\ A \qquad I_D = I_S$$

2. JFET and depletion-type MOSFETs

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

3. Enhancement-type MOSFET:

$$I_D = k(V_{GS} - V_T)^2$$

7.2. Common FET Biasing Techniques

7.2.1. Fixed Bias Configuration

The simplest biasing arrangement for the n-channel JFET, known as the fixed-bias configuration, is shown in Fig. (1). This configuration can be solved using either a mathematical or graphical approach. Both methods are presented in this section to highlight the differences and demonstrate that the same solution can be achieved with either method.

In Fig. (1), the configuration includes the AC levels V_i and V_o, along with the coupling capacitors (C_1 and C_2). These capacitors act as **open circuits** during DC

analysis and as **short circuits** during AC analysis. The resistor R_G ensures that the input voltage is applied to the FET amplifier during AC analysis.

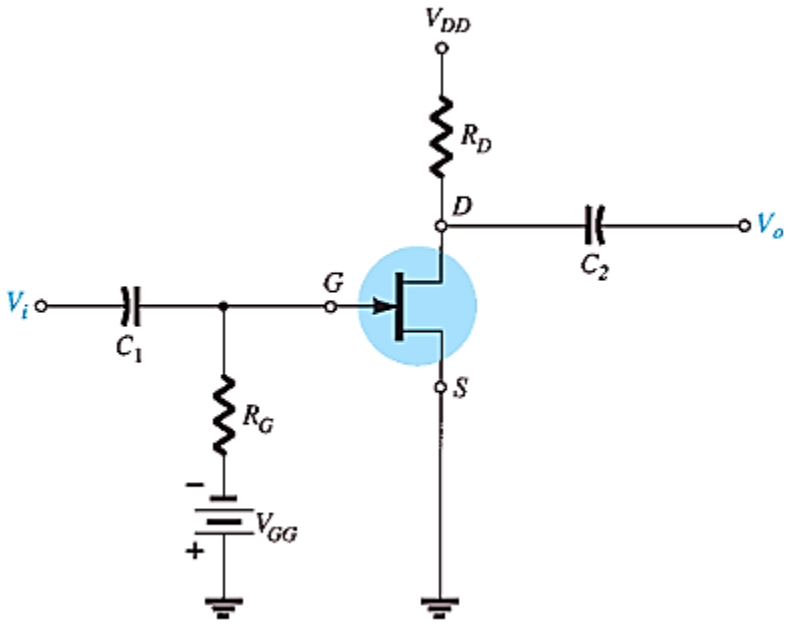


Fig. (1). Fixed-bias configuration.

$$I_G \cong 0\ A$$

$$V_G = I_G R_G = 0 \times R_G = 0\ volt$$

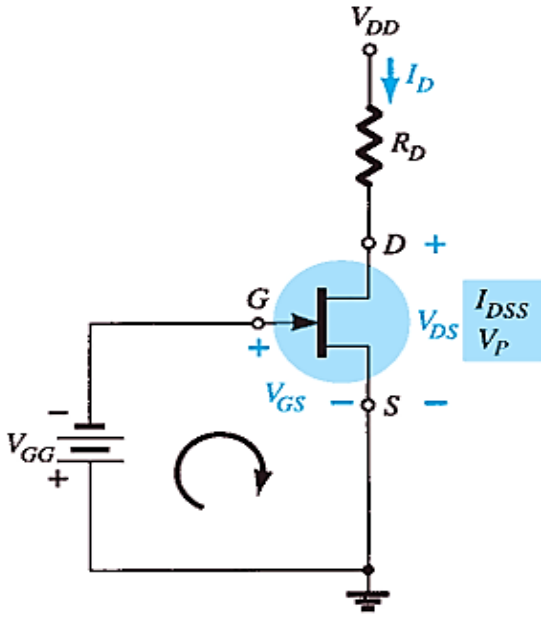
$$V_{GS} = -V_{GG}$$

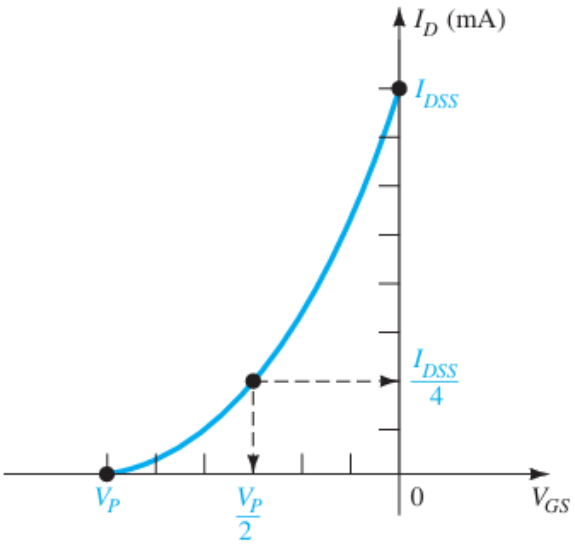
$$V_{DS} = V_{DD} - I_D R_D$$

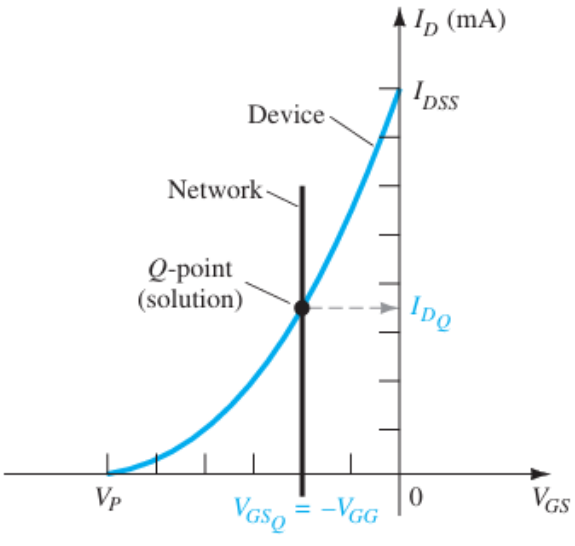
$$V_S = 0$$

$$V_D = V_{DS}$$

$$V_{GS} = V_G$$

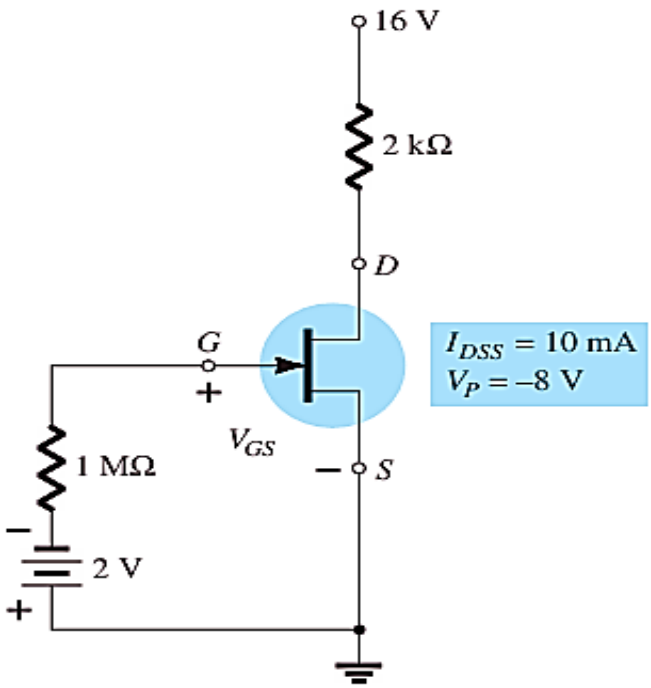






Example 1: Determine the following for the network of fig below:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.



SOL:

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

c. $$V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$$
$$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

7.2.2. Voltage-Divider Bias

The voltage-divider bias is a widely used biasing configuration for both BJT and FET amplifiers, as it provides good stability of the operating point against variations in temperature and transistor parameters. While the circuit arrangement for BJT and FET amplifiers is structurally similar, their operating principles and corresponding DC analysis differ significantly. As shown in Fig. (2).

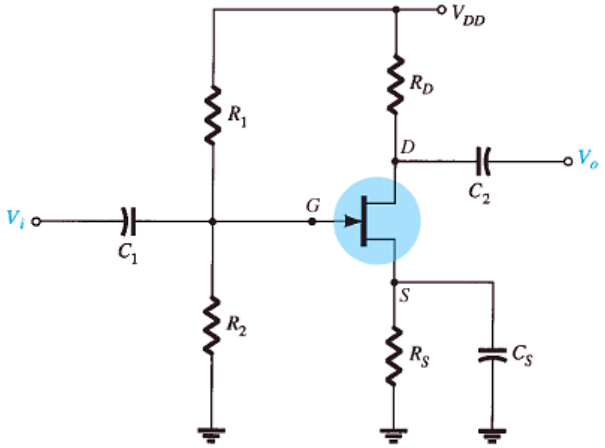


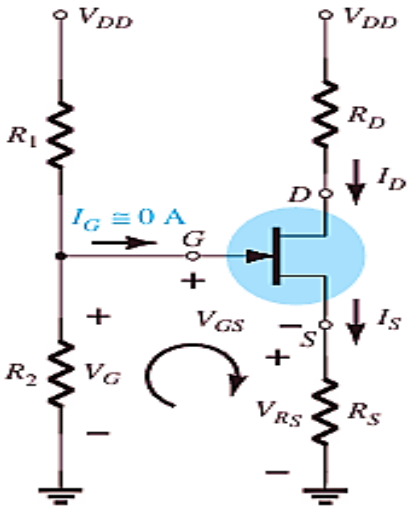
Fig. (2). Voltage-divider bias arrangement

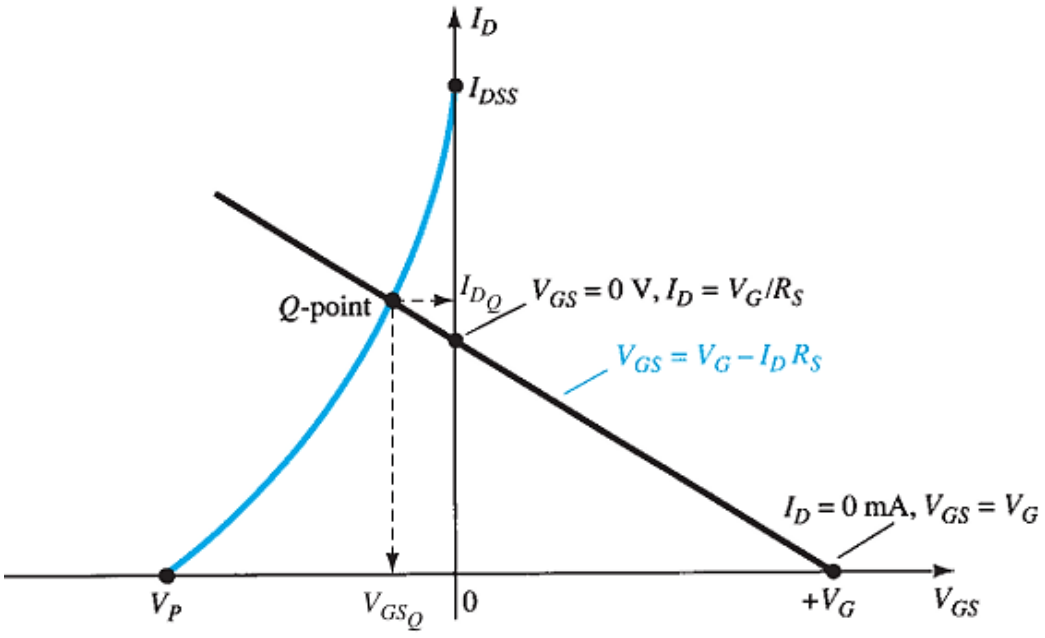
$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{GS} = V_G | I_D = 0$$

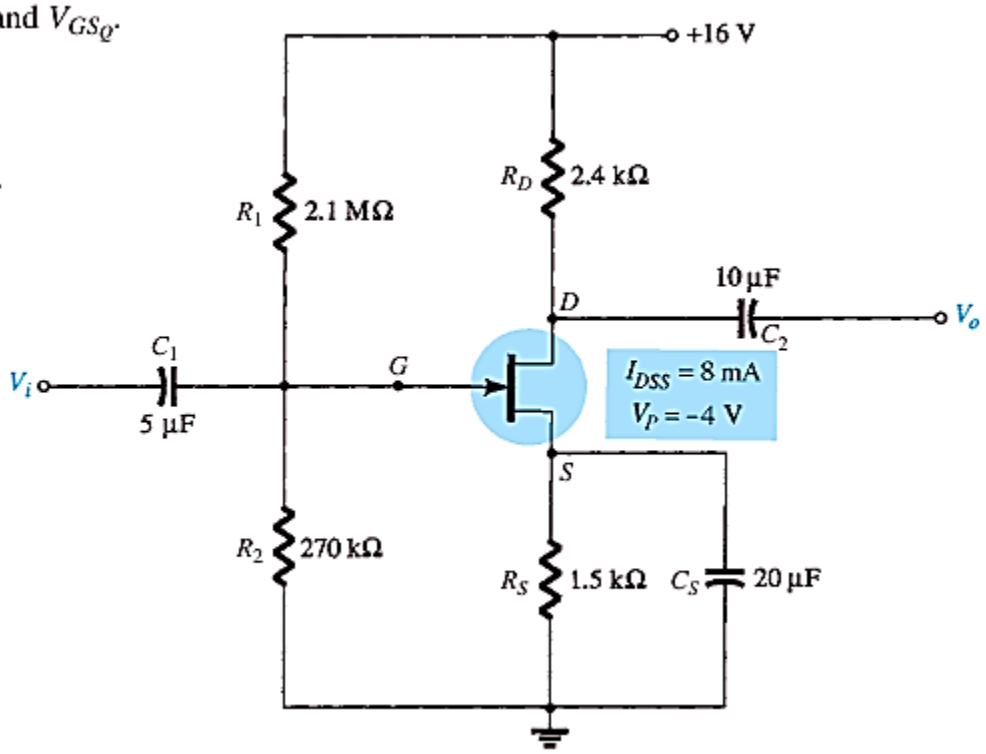
$$I_D = \frac{V_G}{R_S} | V_{GS} = 0$$





Example (2): Determine the following for the network of Fig below:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.
c. V_S.
d. V_{DS}.
e. V_{DG}.



SOL/

a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\,\text{mA}/4 = 2\,\text{mA}$, then $V_{GS} = V_P/2 = -4\,\text{V}/2 = -2\,\text{V}$. The resulting curve representing Shockley's equation appears in Fig. 7.22. The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

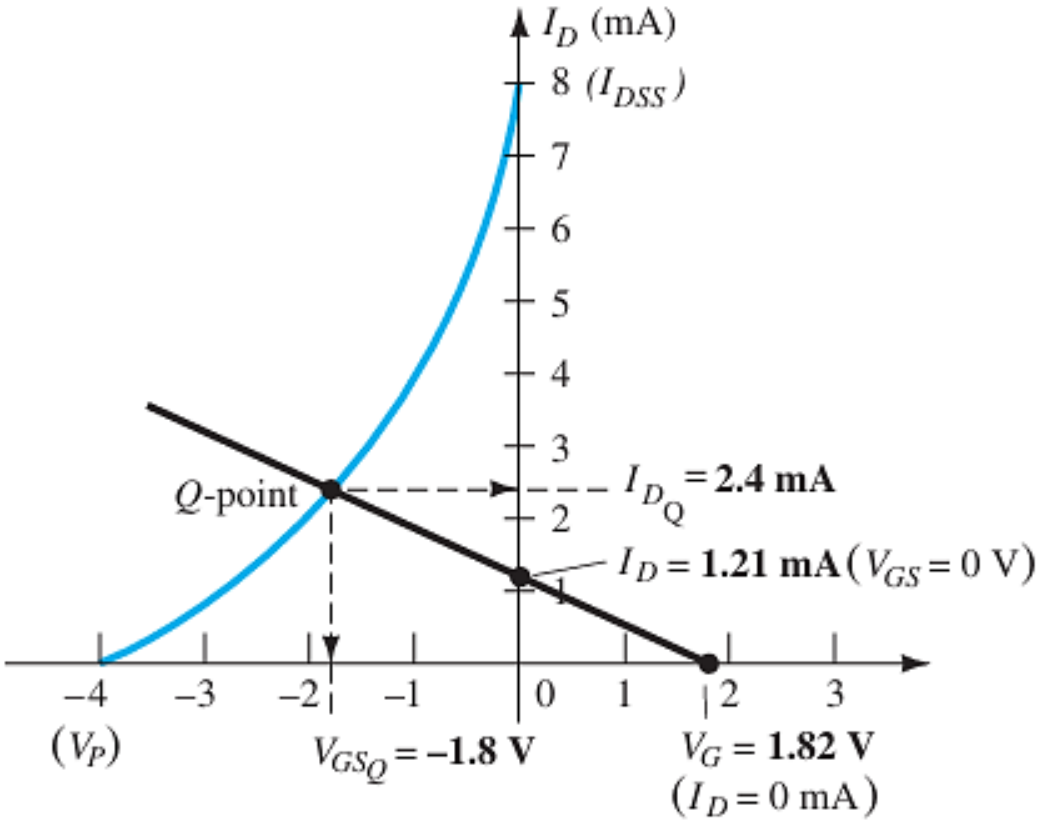
$$= \frac{(270\,\text{k}\Omega)(16\,\text{V})}{2.1\,\text{M}\Omega + 0.27\,\text{M}\Omega}$$

$$= 1.82\,\text{V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\,\text{V} - I_D(1.5\,\text{k}\Omega)$$



When $I_D = 0$ mA,

$$V_{GS} = +1.82 \text{ V}$$

When $V_{GS} = 0$ V,

$$I_D = \frac{1.82 \text{ V}}{1.5 \text{ k}\Omega} = 1.21 \text{ mA}$$

The resulting bias line appears on Fig. 7.22 with quiescent values of

$$I_{D_Q} = \mathbf{2.4 \text{ mA}}$$

and

$$V_{GS_Q} = \mathbf{-1.8 \text{ V}}$$

b. $V_D = V_{DD} - I_D R_D$
$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega)$
$= \mathbf{10.24 \text{ V}}$

c. $V_S = I_D R_S = (2.4 \text{ mA})(1.5 \text{ k}\Omega)$
$= \mathbf{3.6 \text{ V}}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$
$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega + 1.5 \text{ k}\Omega)$
$= \mathbf{6.64 \text{ V}}$
or $V_{DS} = V_D - V_S = 10.24 \text{ V} - 3.6 \text{ V}$
$= \mathbf{6.64 \text{ V}}$

e. Although seldom requested, the voltage V_{DG} can easily be determined using

$$V_{DG} = V_D - V_G$$
$$= 10.24 \text{ V} - 1.82 \text{ V}$$
$$= \mathbf{8.42 \text{ V}}$$

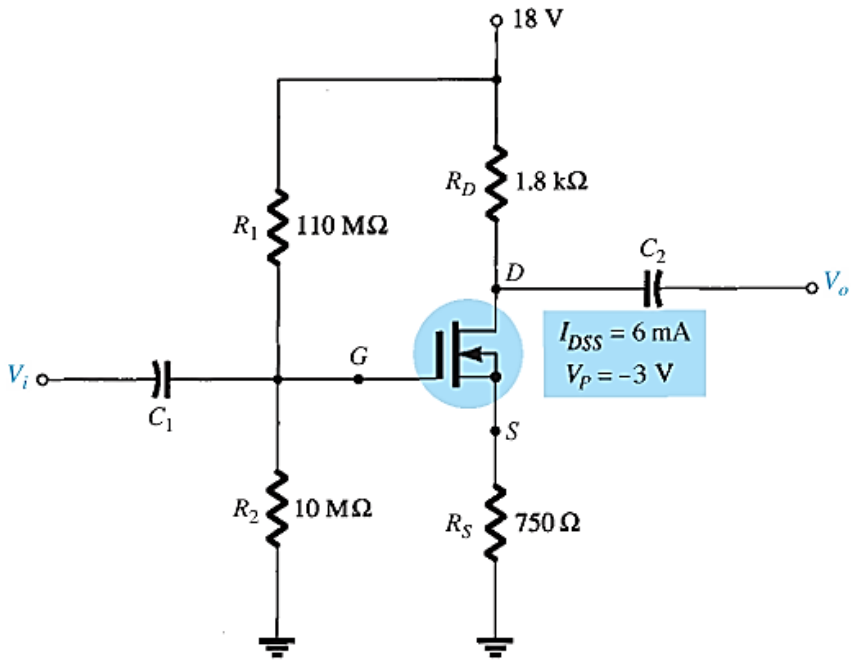
7.3. Biasing for Specific FET Types:

7.3.1. Depletion-type MOSFET

The transfer curves of JFETs and depletion-type MOSFETs are similar in appearance, allowing for comparable DC domain analysis. The main difference is that depletion-type MOSFETs can operate at positive V_{GS} values and I_D levels exceeding I_{DSS}. In all configurations, replacing a JFET with a depletion-type MOSFET results in the same analysis, except for defining how Shockley's equation extends for positive V_{GS}. The required range for the transfer curve is generally determined by the MOSFET parameters and the network's bias line. Simple examples can illustrate the impact of this change on the analysis.

Example (3): For the n-channel depletion-type MOSFET of Fig below, determine:

a. I_{D_Q} and V_{GS_Q}.
b. V_{DS}.



SOL/

a. For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}\,(1.778)$$
$$= 10.67\text{ mA}$$

The resulting transfer curve appears in Fig. (3). Proceeding as described for JFETs, we have:

$$V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$
$$\therefore V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$

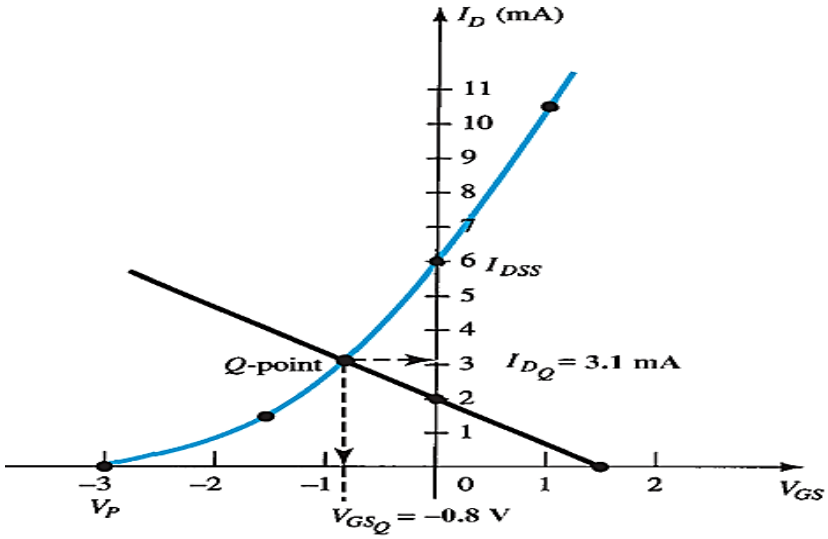


Fig. (3). Determining the Q-point for the network

Setting $I_D = 0$ mA results in

$$V_{GS} = V_G = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{750\ \Omega} = 2\text{ mA}$$

The resulting operating point is given by:

$$I_{D_Q} = \mathbf{3.1\ mA}$$
$$V_{GS_Q} = \mathbf{-0.8\ V}$$

b.

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18\text{ V} - (3.1\text{ mA})(1.8\text{ k}\Omega + 750\ \Omega)$$
$$\cong \mathbf{10.1\ V}$$

7.3.2. Enhancement-type MOSFET

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from those of the preceding sections. First and foremost, recall that for the n -channel enhancement-type MOSFET, the drain current is zero for levels of gate to-source voltage less than the threshold level $V_{GS_{TH}}$ as shown in Fig. (4). For levels of V_{GS} greater than $V_{GS_{TH}}$, the drain current is defined by:

$$I_D = k(V_{GS} - V_{GS_{TH}})^2$$

$$k = \frac{I_{D(on)}}{(V_{GS} - V_{GS_{TH}})^2}$$

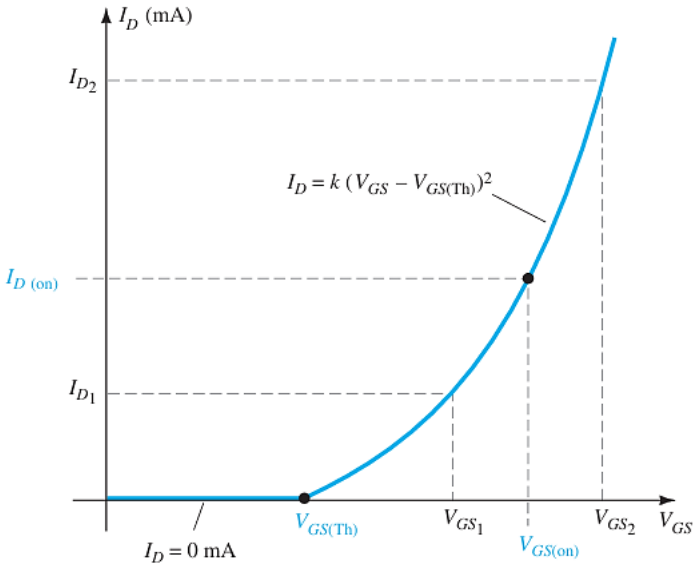


Fig. (4). Transfer characteristics of an n-channel enhancement-type MOSFET.

Feedback Biasing Arrangement A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. (5). The resistor R G brings a suitably large voltage to the gate to drive the MOSFET "on." Since $I_G = 0$ mA, $V_{RG} = 0$ V and the dc equivalent network appears as shown in Fig. (5).

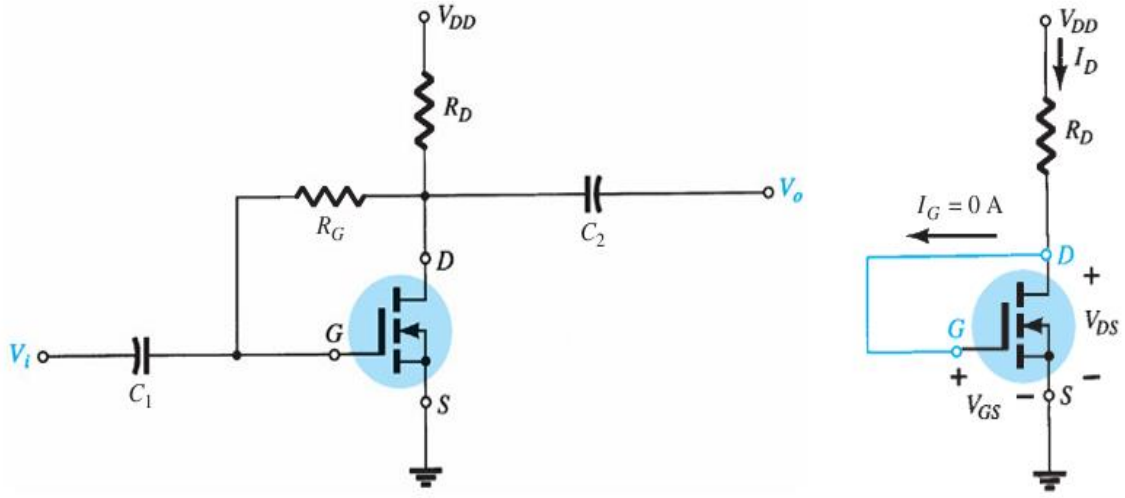


Fig. (5). DC equivalent of the network

$$V_{DS} = V_{GS}$$

$$V_{GS} = V_{DD} - I_D R_D$$

$$V_{GS} = V_{DD} | I_D = 0\ mA$$

$$I_D = \frac{V_{DD}}{R_D} | V_{GS} = 0\ V$$

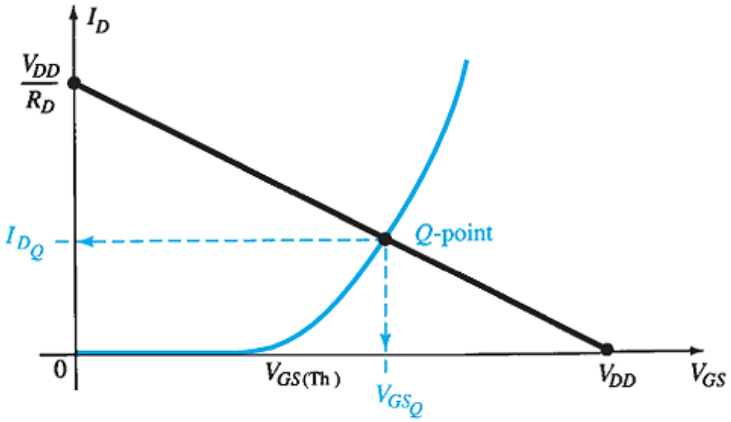
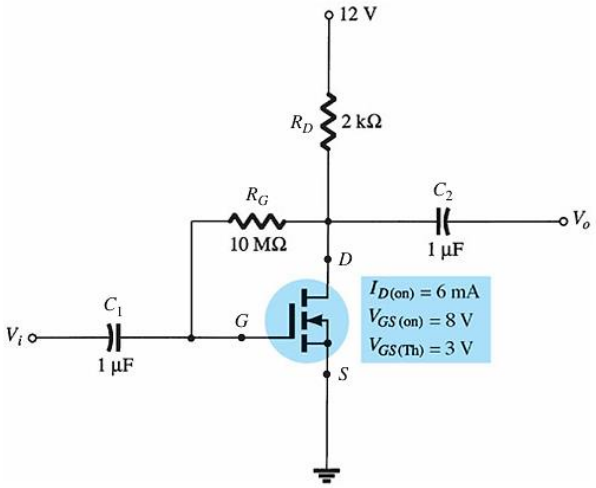


Fig. (6). Determining the Q-point for the network

Example (5): **Determine I_{DQ} and V_{DSQ} for the enhancement-type MOSFET**



Plotting the Transfer Curve Two points are defined immediately as shown in Fig above. Solving for k , we obtain

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$
$$= \frac{6\text{ mA}}{(8\text{ V} - 3\text{ V})^2} = \frac{6 \times 10^{-3}}{25}\text{A/V}^2$$
$$= \mathbf{0.24 \times 10^{-3}\,A/V^2}$$

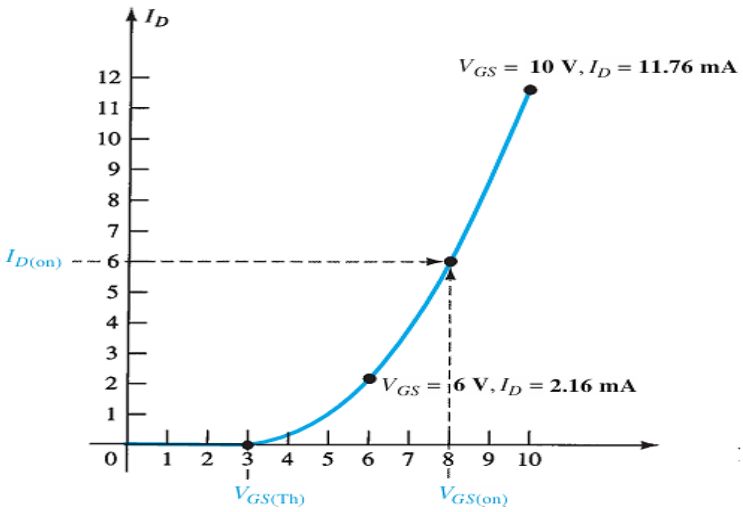


Fig. (7). Plotting the transfer curve for the MOSFET

For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$
$$= 2.16\text{ mA}$$

as shown on Fig. 7.41. For $V_{GS} = 10$ V (slightly greater than $V_{GS(\text{Th})}$),

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$
$$= 11.76\text{ mA}$$

For the Network Bias Line

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$
$$V_{GS} = V_{DD} = 12\text{ V}\big|_{I_D=0\text{ mA}}$$
$$I_D = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}\big|_{V_{GS}=0\text{ V}}$$

$$I_{D_Q} = \mathbf{2.75\text{ mA}}$$
$$V_{GS_Q} = 6.4\text{ V}$$
$$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\text{ V}}$$

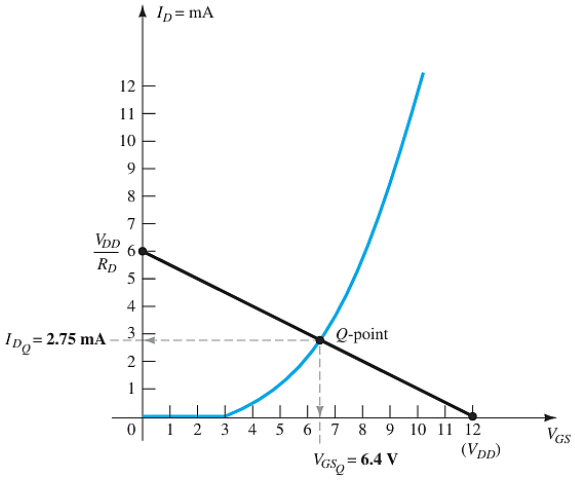


Fig. (8). Determining the Q-point for the network

Voltage-Divider Biasing Arrangement

$$\boldsymbol{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}}$$

$$\boldsymbol{V_{GS} = V_G - I_D R_S}$$

$$\boldsymbol{V_{DS} = V_{DD} - I_D(R_S + R_D)}$$

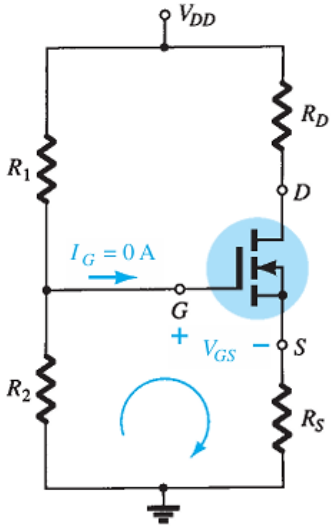
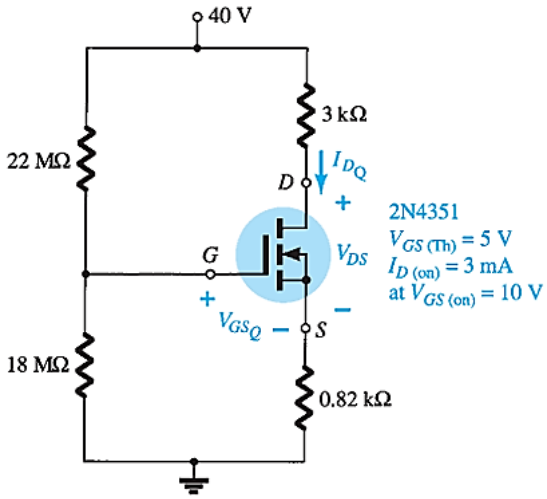


Fig. (9). Voltage-divider biasing arrangement for an n-channel enhancement MOSFET

Example (6): **Determine I_{DQ} , V_{GS} , and V_{DS} for the network of fig below:**



SOL/

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\,\text{M}\Omega)(40\,\text{V})}{22\,\text{M}\Omega + 18\,\text{M}\Omega} = 18\,\text{V}$$

$$V_{GS} = V_G - I_D R_S = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

When $I_D = 0\,\text{mA}$,

$$V_{GS} = 18\,\text{V} - (0\,\text{mA})(0.82\,\text{k}\Omega) = 18\,\text{V}$$

as appearing on Fig. 7.45. When $V_{GS} = 0\,\text{V}$,

$$V_{GS} = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

$$0 = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

$$I_D = \frac{18\,\text{V}}{0.82\,\text{k}\Omega} = 21.95\,\text{mA}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40\,\text{V} - (6.7\,\text{mA})(0.82\,\text{k}\Omega + 3.0\,\text{k}\Omega)$$

$$= 40\,\text{V} - 25.6\,\text{V}$$

$$= \mathbf{14.4\,V}$$

Summary:

1) Biasing refers to the process of setting voltage and current levels to establish a suitable operating point for stable and efficient transistor operation.
2) Stabilize the operating point regardless of temperature variations or transistor parameter changes.
3) Ensure the FET or MOSFET operates in the desired region (linear or saturation) depending on the application.
4) A resistor is placed in the source terminal (Rs) to stabilize the operating point.
5) The gate voltage (Vg) is often zero, with the gate connected to ground.
6) A fixed voltage is applied to the gate using a voltage source and a resistor.
7) A voltage-divider network using resistors provides a stable gate voltage.
8) Offers better stability compared to fixed biasing.

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