Real Time System

Third Level

I/O Interfacing and
Programmable Devices

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Goals
Up-on completing this lecture, the student should be able to:

1- Identify the concepts behind interfacing using octal buffers
2- Comprehend the c/c of 74LS373, 74LS374.
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Tri-state Buffers are available in integrated circuits form as octal buffer/drivers in both unidirectional and bi-directional forms, with the more common being the TTL 74240, the TTL 74244 and the TTL 74245.
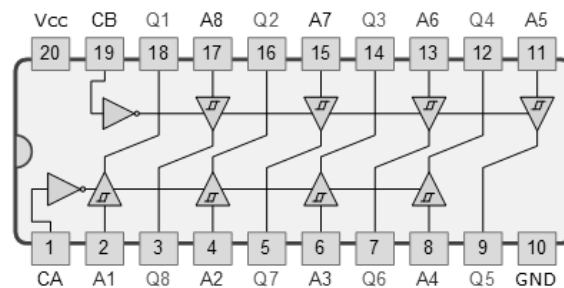
The most commonly available Digital Buffer and Tri-state Buffer IC's include:

- 74LS07 Hex Non-inverting Buffer.
- 74LS17 Hex Buffer/Driver.
- 74LS244 Octal Buffer/Line Driver.
- 74LS245 Octal Bi-directional Buffer.

74LS07 Digital Buffer
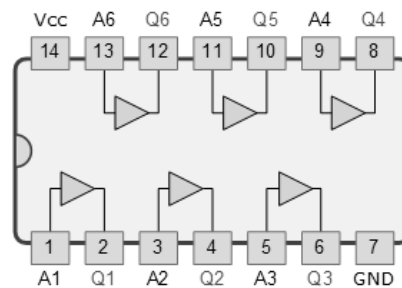
74LS244 Octal Tri-state Buffer

74LS244 Octal 3-State Buffer/Line Driver/Line Receiver

The 74LS244 buffer/line driver is designed to improve the performance of 3-State buffers/ drivers plus to provide improved noise rejection.

In electronics, a driver is an electrical circuit or other electronic component used to control another circuit or component, such as a high-power transistor, liquid crystal display (LCD), and numerous others. They are usually used to regulate current flowing through a circuit or is used to control the other factors such as other components, some devices in the circuit.

Features:-

- 3-State outputs drive bus lines.

- PNP inputs reduce DC loading on bus lines.

- Improves noise rejection.

- Typical I_{OL} (sink current) 24 mA.

- Typical I_{OH} (source current) -15 mA.

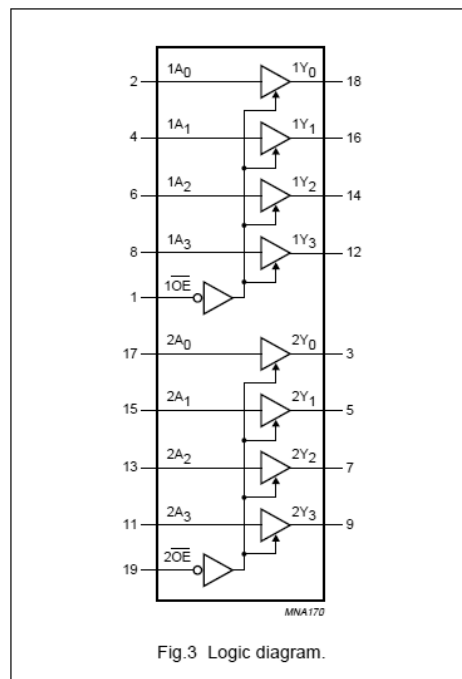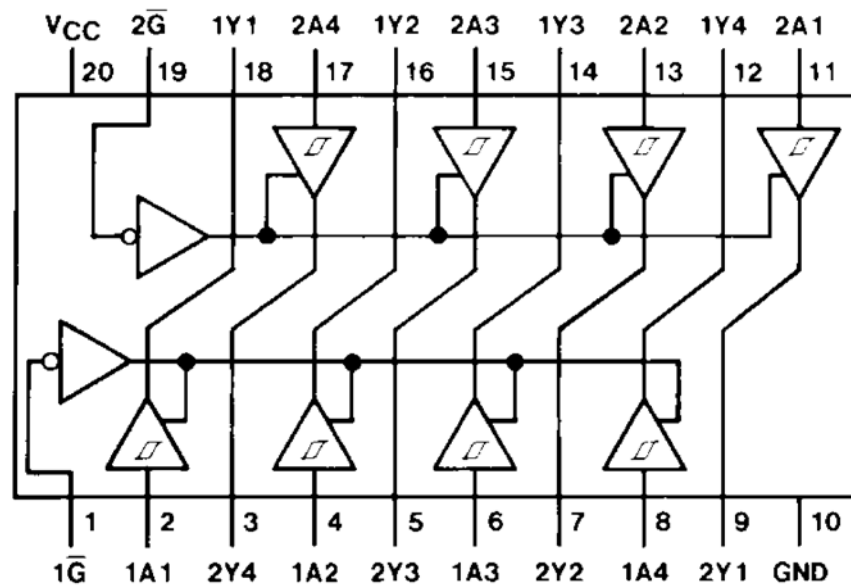- Typical enable/disable time 18 ns.

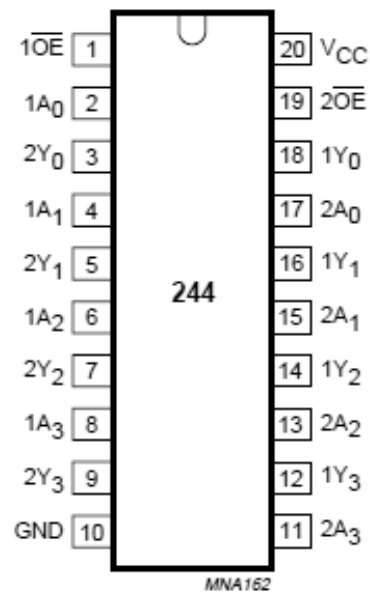**Connection Diagram**

Fig.3 Logic diagram.

Fig.1 Pin configuration.

Function Table

Inputs		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = LOW Logic Level
H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
Z = High Impedance

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

- Supply Voltage 7V.
- Operating Free Air Temperature Range 0°C to +70°C.
- Storage Temperature Range -65°C to +150°C.

Recommended Operating Conditions

| Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
I_{OH}	HIGH Level Output Current			−15	mA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

74LS245 Octal Bus Transceiver

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can disable the device so that the buses are effectively isolated.

Features:-

- 3-State Outputs Drive Bus Lines.

- PNP Inputs Reduce DC Loading on Bus Lines.

- Improves Noise rejection.

- 2-Way Asynchronous Data Bus Communication.

- Typical I_{OL} (sink current) 24 mA.

- Typical I_{OH} (source current) -15 mA.

Logic and Connection Diagrams
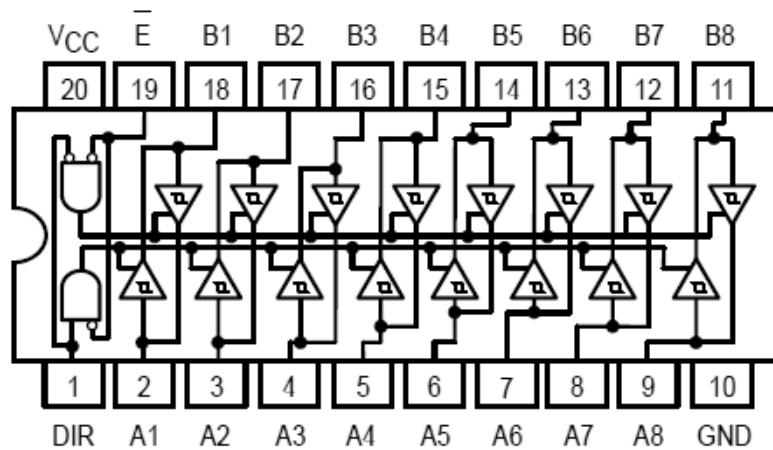
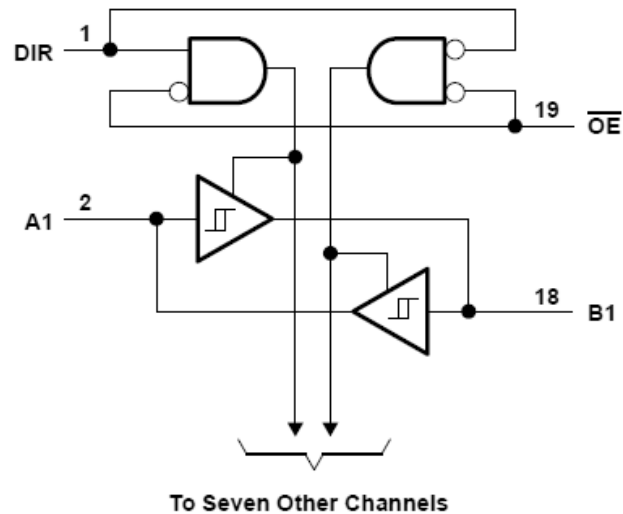

TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

logic diagram (positive logic)

To Seven Other Channels

recommended operating conditions

| | | SN74LS245 | | | UNIT |
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

74LS373 / 74LS374 3-State Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

The 74LS37X (3, 4) consists of eight registers (latches, flip flop) with 3-state outputs. The eight latches of the 74LS373 are D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up. The eight flip-flops of the 74LS374 are edge-triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs. The 74LS37X (3, 4) is a high-speed, low-power Octal D-type (latch or Flip-Flop) featuring separate D-type inputs for each latch or flip-flop and 3-state outputs. A buffered Clock and Output Enable is common to all latches and flip-flops. The 74LS37X (3, 4) is manufactured using advanced Low Power technology and is compatible with all TTL families. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state.

Connection Diagrams

Dual-In-Line Packages

'LS373

'LS374
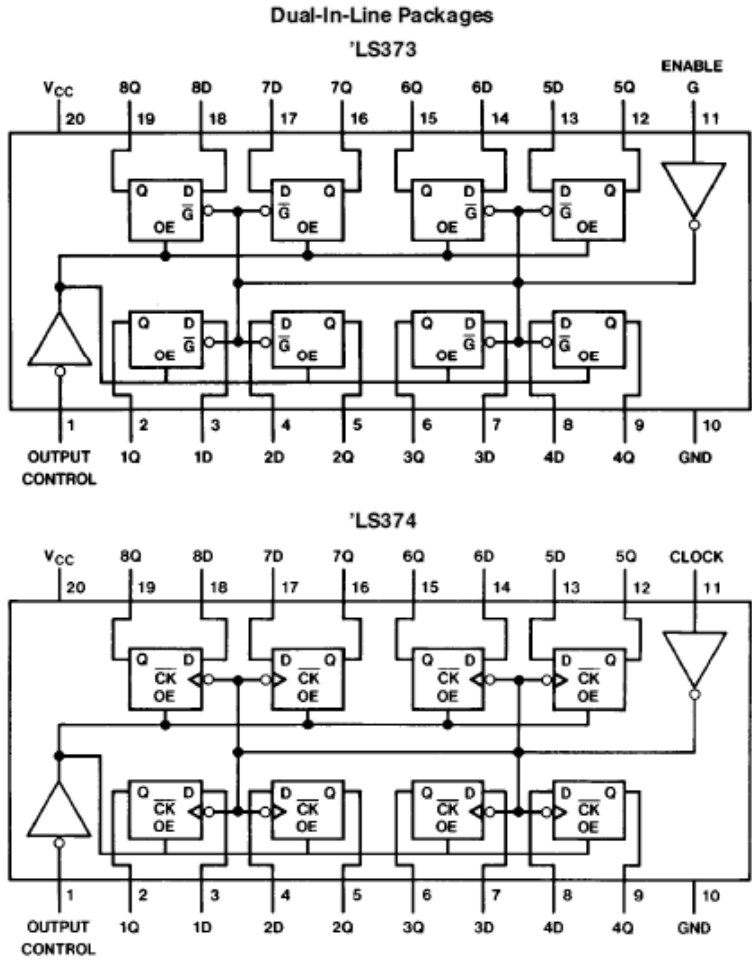
Function Tables
DM54/74LS373

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care
↑ = Transition from low-to-high level, Z = High Impedance State
Q_0 = The level of the output before steady-state input conditions were established.

DM54/74LS374

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

DM54/74LS334
Transparent Latches

OUTPUT CONTROL (1)

1D (3) — D / Ḡ / Q̄ — (2) 1Q
2D (4) — D / Ḡ / Q̄ — (5) 2Q
3D (7) — D / Ḡ / Q̄ — (6) 3Q
4D (8) — D / Ḡ / Q̄ — (9) 4Q
5D (13) — D / Ḡ / Q̄ — (12) 5Q
6D (14) — D / Ḡ / Q̄ — (15) 6Q
7D (17) — D / Ḡ / Q̄ — (16) 7Q
8D (18) — D / Ḡ / Q̄ — (19) 8Q

ENABLE (11) G

DS006431-3

DM54/74LS374
Positive-Edge-Triggered Flip-Flops

OUTPUT CONTROL (1)

1D (3) — D / CK / Q̄ — (2) 1Q
2D (4) — D / CK / Q̄ — (5) 2Q
3D (7) — D / CK / Q̄ — (6) 3Q
4D (8) — D / CK / Q̄ — (9) 4Q
5D (13) — D / CK / Q̄ — (12) 5Q
6D (14) — D / CK / Q̄ — (15) 6Q
7D (17) — D / CK / Q̄ — (16) 7Q
8D (18) — D / CK / Q̄ — (19) 8Q

CLOCK (11)

DS006431-4
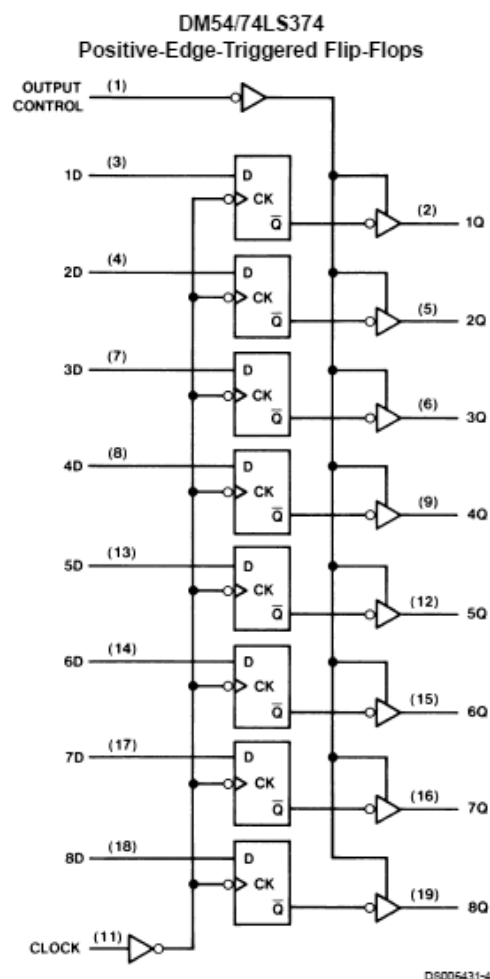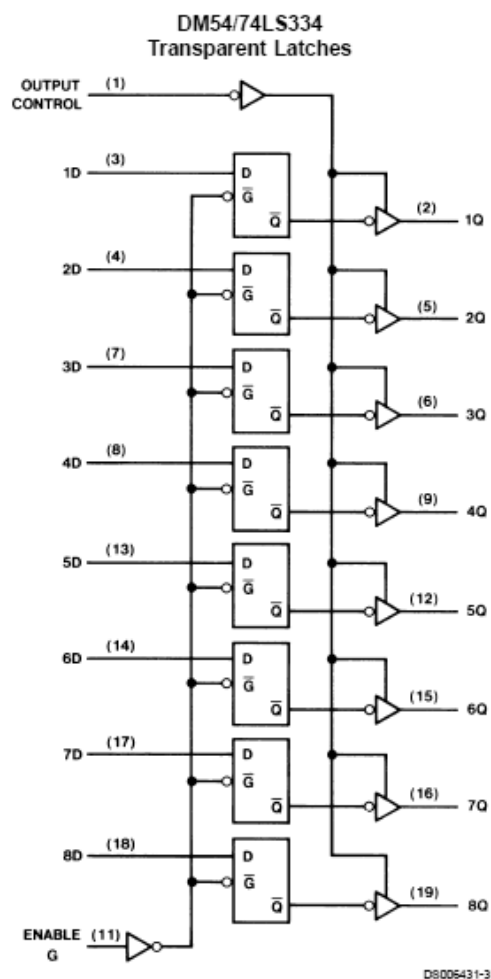
Absolute Maximum Ratings

- Supply Voltage 7V.

- Operating Free Air Temperature Range 0°C to +70°C.

- Storage Temperature Range -65°C to +150°C.

Recommended Operating Conditions

Symbol	Parameter	DM74LS373			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
I_{OH}	High Level Output Current			−2.6	mA
I_{OL}	Low Level Output Current			24	mA

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3.5.1 Interfacing to 8-bit Bus

In a simple system, a tri-state buffer such as 74LS244 can be used as an input port and a latch such as 74LS374 can be used as an output port.

Programmable Devices:-

The CPU needs to check whether a peripheral is ready before reads from or write into a device because the execution speed of the processor is much faster than the response of the peripheral such as printer. For example, when CPU sends data byte (characters) to a printer, the processor can execute the instructions to transfer a byte in (ns or µs), on the other hand, the printer can take 10 to 25 ms to print a character. After transferring a character to the printer, the CPU should wait until the printer is ready for the next character, otherwise the data will be lost. To prevent the loss of data, signals are exchanged between the CPU and peripheral before to data transfer; these signals are called handshake signals.

So we can summarize the requirements for a programmable interfacing device as follow:

The device should include:
- Input and output registers (latches and flip flops).
- Tri-state buffers.
- Bidirectional data flow.
- Handshake and interrupt signals.
- Control logic.
- Chip select logic.
- Interrupt control logic.

Is the 74LS245 programmable or not?

Can we make it programmable? How?

Recommended Operating Conditions

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		Min	Nom	Max	
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Is the 74LS245 programmable or not?

Can we make it programmable? How?

- The direction of data flow is determined by DIR.

- When E = 0 the 47ls245 is Bidirectional, DIR = 0 the data flow from B to A, DIR = 1 the data flow from A to B. when E = 1 it's became isolation.

- We can program the 74LS245 by CPU when we connect to register called control register and connect the DIR on the any bits of register.

- The CPU controls the 74LS245 by sending appropriate control word register to activate the proper value of DIR. this word called control word of programmable device.

Now the question is: How would the MPU write into the control register? It does so the same way it would with any other I/O port, through a port address. Figure 13.2 shows that the address lines A_7–A_1 are used to select the chip through a NAND gate and A_0 is used to differentiate between the control register and the transreceiver. When A_0 is high, the control register is enabled, and when A_0 is low, the transreceiver is enabled. Thus, the MPU could access the control register through the port address FF_H; and the transreceiver through FE_H. To set up the transreceiver as an output device, the control word would be 01_H, and to set it up as an input device the control word would be 00_H.
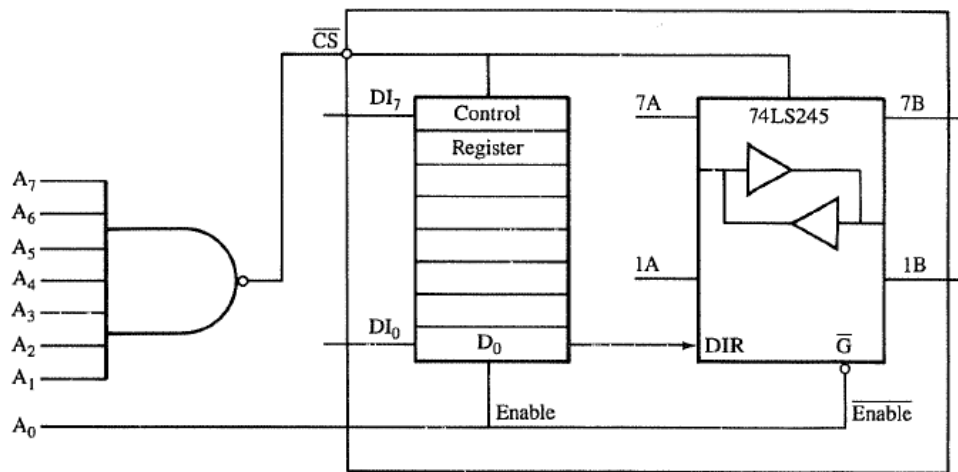

FIGURE 13.2
Making 74LS245 Programmable

Example 13.1	Write instructions to initialize the hypothetical chip (Figure 13.2) as an output buffer and send a byte.

Solution

Instructions

```
LD A, 01H        ;Set D0 = 1, D1 through D7 are "don't care" lines
OUT (FFH), A     ;Write in the control register
LD A, BYTE1      ;Load data byte
OUT (FEH), A     ;Send data out
```

In the last example, we used the 74LS245 as a tri-state buffer. However, in microprocessor applications, we often need registers that can be used as I/O ports. We can build a latch with a buffer, and by controlling the enable signal of the latch, we can program it to function as an input port or an output port. Figure 13.3 shows two latches (representing eight latches in each direction); the enable signals of these latches are controlled by bit D_0 in the control register. If bit D_0 is 0, it enables the output latch, and if D_0 is 1, it enables the input latch. Thus, by programming bit D_0, we can make the device function as an input port or an output port. When the device is programmed as an output device, the MPU can write to the port by using the $\overline{WR}$ control signal to enable the tri-state buffer and to send out a byte. When bit $D_0 = 1$, the input latch is enabled and the output latch is disabled, and the MPU can read by enabling the input buffer. If we have additional registers (or I/O ports),
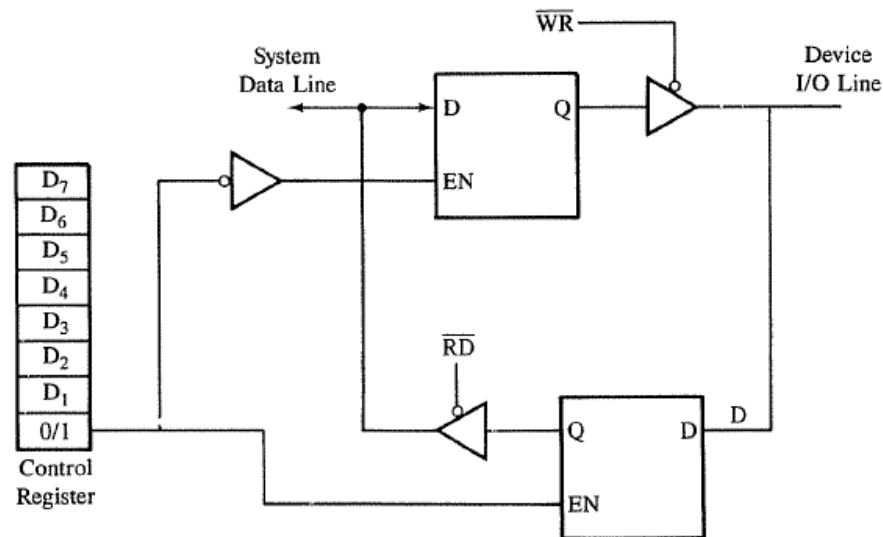

FIGURE 13.3
Programmable I/O Ports

Programmable device with Handshake Signals:-

The CPU and peripherals at different speeds, therefore signals are exchanged prior to data transfer between the fast response CPU and slow response of peripherals, such as printers and keyboard. These signal called handshake signals, these signals generally provide by programmable devices.

**The steps in data input from a peripheral such as keyboard**

1. A peripheral send data byte in the port and informs the interfacing device by sending handshake signal STB (strobe).

2. The interfacing device informs the peripheral that the input port is full - do not send the next byte until this has been read by sending handshake signal IBF (input buffer full).

3. The interfacing device informs the CPU that there is a byte available to read by sending interrupt signal (INTR).

4. The CPU reads the byte by sending control signal RD.

The steps in data output to a peripheral such as printer

1. The CPU writes a data byte into the port of programmable interfacing device by sending control signal WR.

2. Programmable interfacing device interrupt the CPU until the peripheral receive the byte by sending interrupt signal (INTR).

3. The interfacing device informs the peripheral that the byte is on the way by sending handshake signal OBF (output buffer full).

4. When the peripheral receive the byte it acknowledge the interfacing device by sending acknowledge signal ACK to interfacing device.

5. The interfacing device interrupts the CPU to ask for the next byte by sending interrupt signal (INTR).

The figure below explains the two processes (input and output).
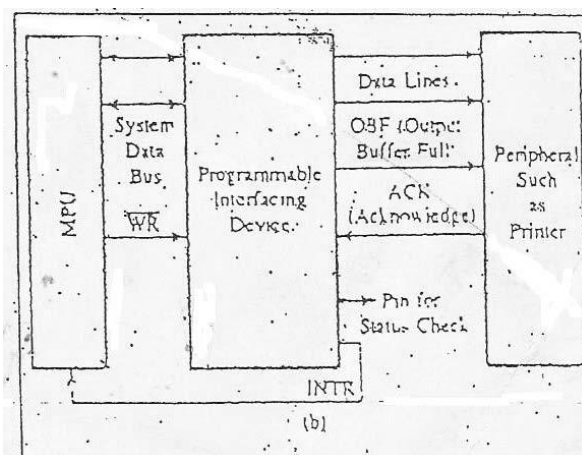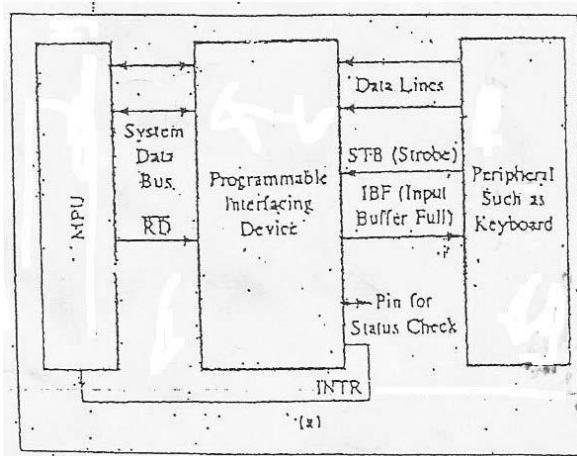
Summary:
1- octal buffers allow for easy interfacing of 8-bit devices.
2- 74LS37x family comes with different pin configurations to provide high design flexibility.

Questions:
1- How does the 74LS373 fit into input interfacing designs ?
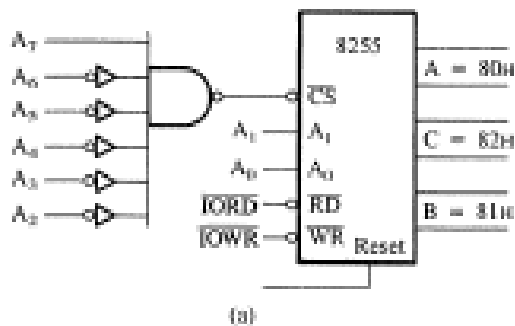2- Draw the internal cct of the 74LS373.

Ex. 1: Configure Port A as i/p in Mode 0, Port B as o/p in mode 0, Port C (Lower) as o/p and Port C (Upper) as i/p ports.

Ex. 2: Configure Port A as i/p in Mode 1, Port B as o/p in mode 1, Port C7-8 as i/p ports. (PC5-0 are handshake lines, some i/p lines and others o/p. So they are shown as X)

Ex. 3: Configure Port A in Mode 2, Port B as o/p in mode 1. (PC5-0 are handshake lines for Port A and PC2-0 are handshake signals for port B)

Ex. 4: what is the control word for the following:

- Port A: simple input, Port B: simple output, Port CL: output, Port CU: input
- Port A: output with handshake, Port B: input with handshake, Port CL: output, Port CU: input
- Port A: Output, Port B: Output, Port CU: Output, Port CL: Output all mode 0.
- Port A: Input, Port B: Input, Port CU: Input, Port CL: Input all mode 0.
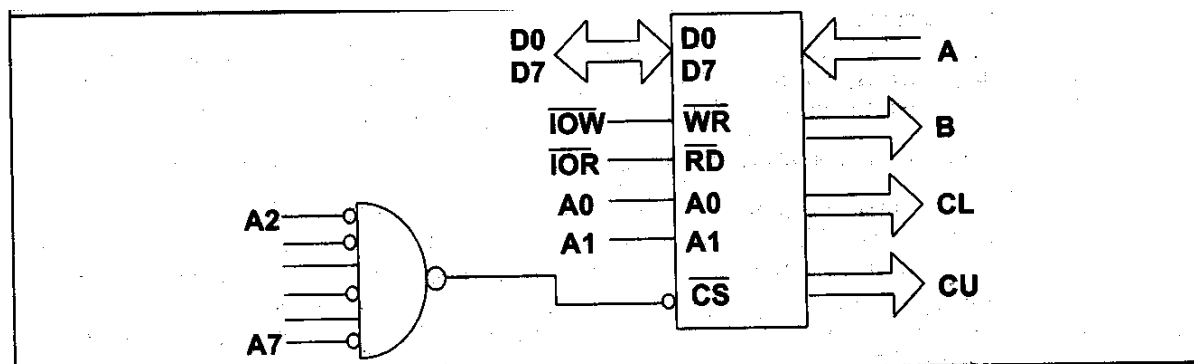

$\overline{CS}$								Hex Address	Port
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	0	0	0	0	0	0	0	= 80H	A
						0	1	= 81H	B
						1	0	= 82H	C
						1	1	= 83H	Control Register

(a)   (b)

Example 4-5

The 8255 shown in Figure 4-6 is configured as follows: port A as input, B as output, and all the bits of port C as output.
(a) Find the port addresses assigned to A, B, C, and the control register.
(b) Find the control byte (word) for this configuration.

Example 4-6

(a) Find the port address for Figure 4-7.
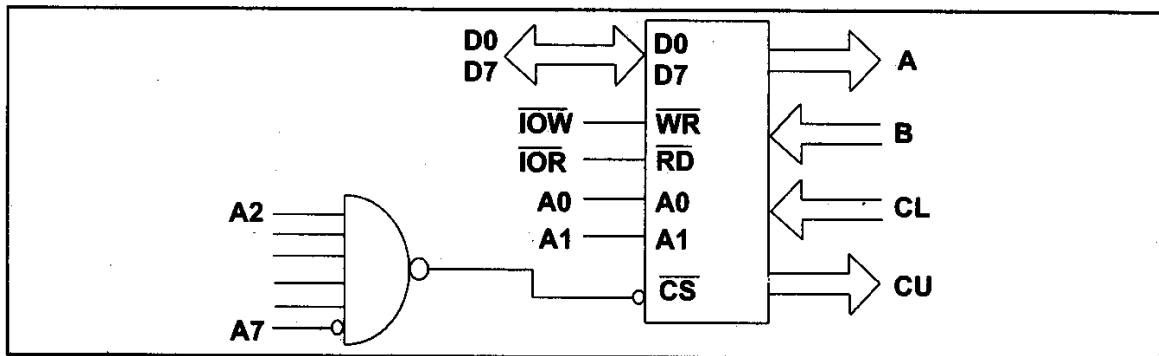(b) Find the control word if PA =out, PB=in, PC0 - PC3 =in, and PC4 - PC7=out.

Figure 4-7. Configuration for Example 4-6

Ex. 5:- Design (draw and explain) an interfacing circuit using the 8255 to read data from an A/D converter and then display the data to meet the following requirement:-

- Setup port A to read data.
- Setup PC0 to start of conversion and PC7 to read the ready status of the converter.
- Display current data on 7 segment connected to port B
- Write the CW and BSR for port C.

Summary:
1- 8255 is similar to 8155 but with richer feature set.
2- 8255 Modes can over-come scenarios where 8155 can't perform.

Questions:
1- What are 8255A modes ?
2- What is BSR mode ?

Real Time System

Third Level

Lecture Thirteen

Programmable Interval Timer
PIT 8253 and 8254

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Goals
Up-on completing this lecture, the student should be able to:

1- Identify the concepts PIT
2- Utilize PIT capabilities in RT designs.