Al-Mustaqbal University
Department of Medical Instrumentation Techniques Engineering
Class 2^{nd}
Subject: Electronic Circuits
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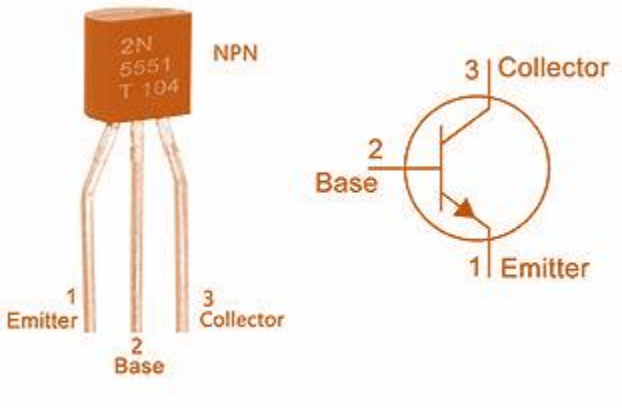
1st term – LEC5-DC biasing BJTs

Electronic Circuit

Lecture 5 (8^{th} Week)

DC biasing (BJT)



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4.1 INTRODUCTION

The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality,

any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.

The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion.

The following important basic relationships for a transistor:

$$V_{BE} \cong 0.7\,\text{V} \qquad (4.1)$$

$$I_E = (\beta + 1)I_B \cong I_C \qquad (4.2)$$

$$I_C = \beta I_B \qquad (4.3)$$

في هذا الفصل سنتعلم وضع الترانزستور في وضع التشغيل عن طريق تحديد قيم الجهد والتيار المستمر في هذا الترانزستور حتى يكون جاهز لتكبير الاشارة. هنالك اكثر من طريقة لعمل ذلك سنتعرف عليها لاحقا.

4.2 OPERATING POINT

The term biasing appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.

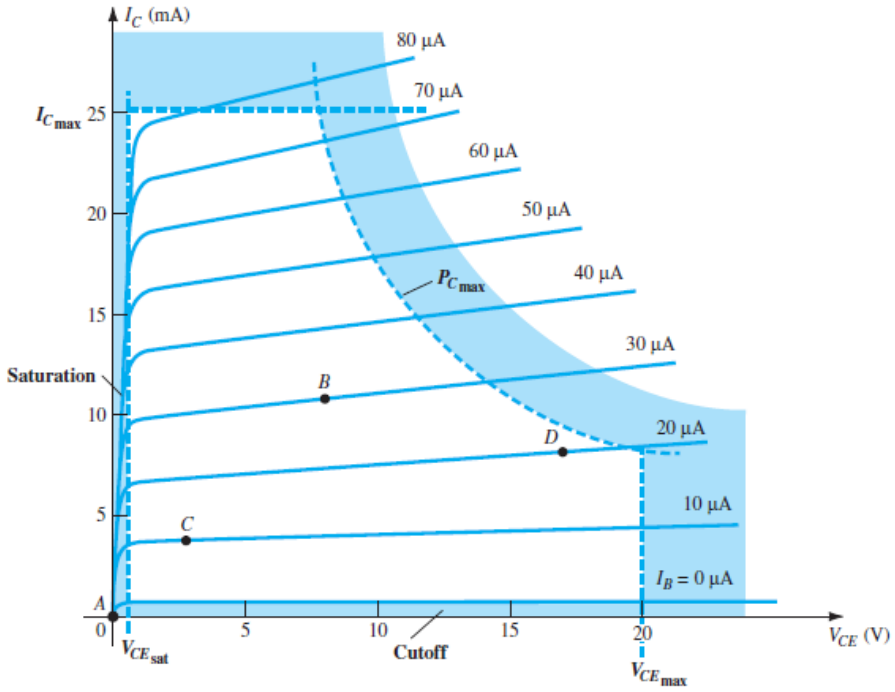

FIG.1: Various operating points within the limits of operation of a transistor

يمكن تمييز عدة مناطق في منحنى خصائص الترانستور ولكي يعمل الترانستور كمكبر يجب ان يكون في المنطقة الفعالة وعلية يجب مراعاة اختيار مصدر الجهد والمقاومات والربط بطريقة تضمن بقاء انحياز الترانستور في المنطقة الفعالة.

For the BJT to be biased in its linear or active operating region the following must be true:

1. The base emitter junction must be forward-biased (P-region voltage more positive), with a resulting forward-bias voltage of about 0.6 V to 0.7 V.

2. The base collector junction must be reverse-biased (N-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.

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[Note that for forward bias the voltage across the p n junction is p - positive, whereas for reverse bias it is opposite (reverse) with n -positive.]

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. Linear-region operation:

Base emitter junction forward-biased

Base collector junction reverse-biased

2. Cutoff-region operation:

Base emitter junction reverse-biased

Base collector junction reverse-biased

3. Saturation-region operation:

Base emitter junction forward-biased

Base collector junction forward-biased

4.3 FIXED-BIAS CONFIGURATION

The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration.

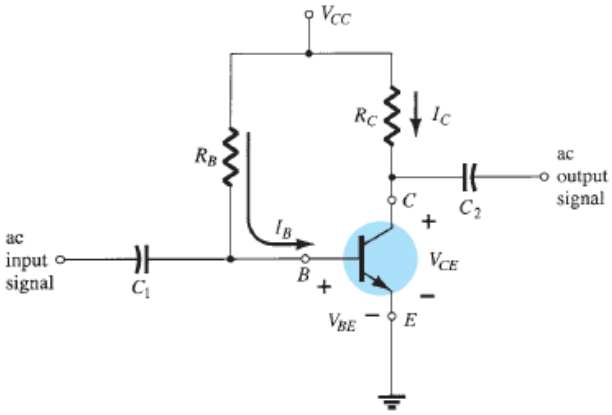

FIG. 2: Fixed-bias circuit.

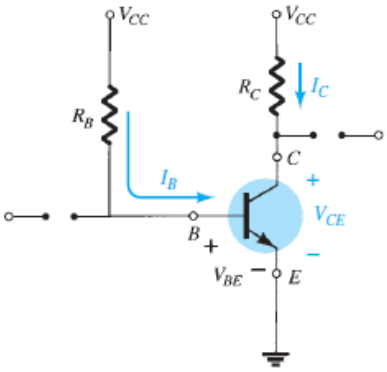

FIG. 3: DC equivalent of Fig.2

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في هذه الدائرة يتم اولا تحليل دائرة الدخل لحاسب تيار القاعدة ومن ثم تحليل دائرة الخرج لحساب تيار الجامع وفولتية الخرج

Forward Bias of Base Emitter:

Consider first the base emitter circuit loop of Fig. 4.4 . Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$+V_{CC} - I_B R_B - V_{BE} = 0$

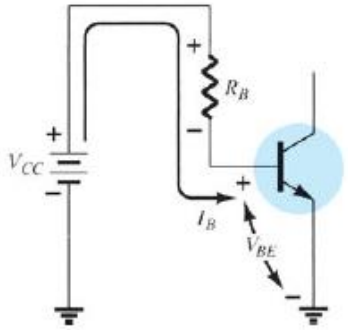

FIG. 4.4
Base–emitter loop.

Note the polarity of the voltage drop across R_B as established by the indicated direction of I_B . Solving the equation for the current I_B results in the following

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad (4.4)$$

نلاحظ ان قيمة تيار القاعدة يعتمد على قيمة المقاومة وكذلك على قيمة فولتية المصدر منقوص منها ال0.7 فولت

Collector Emitter Loop:

The collector emitter section of the network appears in Fig. 4.5 with the indicated direction of current I_C and the resulting polarity across R_C . The magnitude of the collector current is related directly to I_B through

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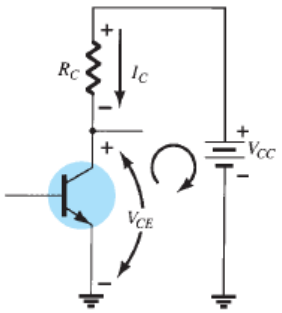

FIG. 4.5
Collector–emitter loop.

$$I_C = \beta I_B \qquad (4.5)$$

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 results in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

and

$$V_{CE} = V_{CC} - I_C R_C \qquad (4.6)$$

which states that the voltage across the collector–emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across R_C.

As a brief review of single- and double-subscript notation recall that

$$V_{CE} = V_C - V_E \qquad (4.7)$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground, respectively. *In this case,* since $V_E = 0$ V, we have

$$V_{CE} = V_C \qquad (4.8)$$

In addition, because

$$V_{BE} = V_B - V_E \qquad (4.9)$$

and $V_E = 0$ V, then

$$V_{BE} = V_B \qquad (4.10)$$

EXAMPLE 4.1

Determine the following for the fixed-bias configuration of Fig. 4.7 .

a. I_{BQ} and I_{CQ}. b. V_{CEQ}. c. V_B and V_C . d. V_{BC} .

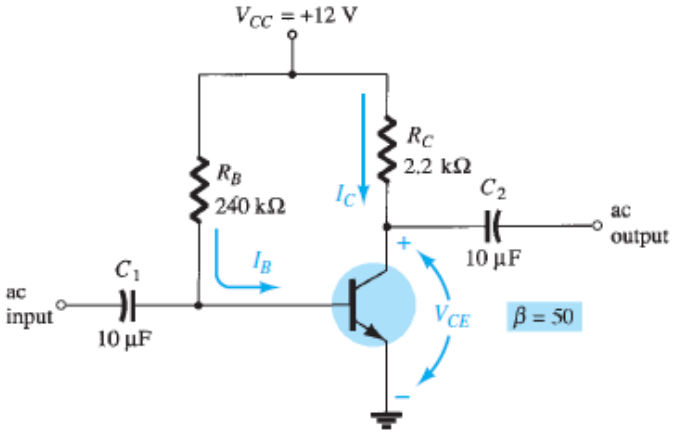

FIG. 4.7
DC fixed-bias circuit for Example 4.1.

Solution:

a. Eq. (4.4): $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

Eq. (4.5): $$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

b. Eq. (4.6): $$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

c. $V_B = V_{BE} = \mathbf{0.7\ V}$
$V_C = V_{CE} = \mathbf{6.83\ V}$

d. Using double-subscript notation yields
$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$

Transistor Saturation

the collector current is relatively high

the collector-to-emitter voltage is at or below

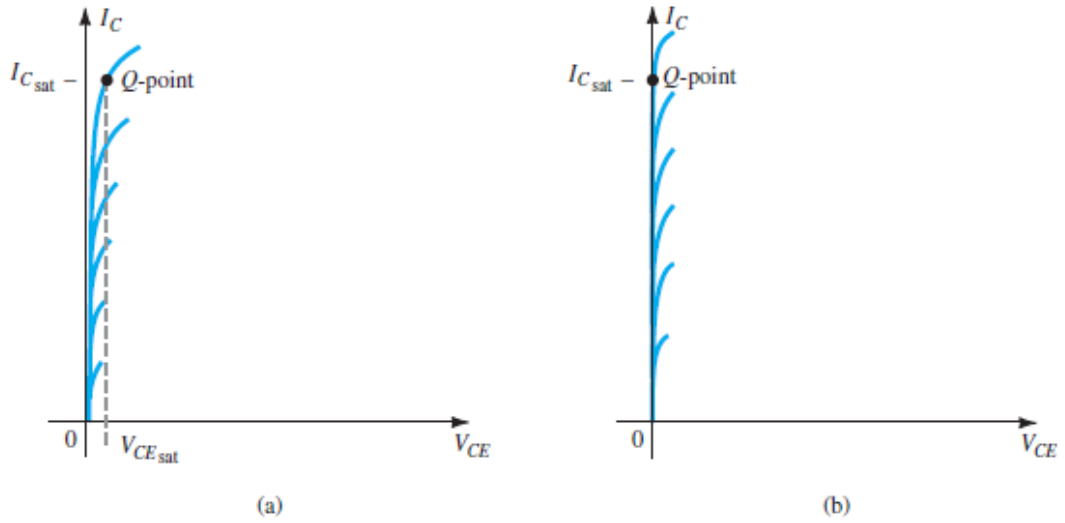

FIG. 4.8
Saturation regions: (a) actual; (b) approximate.

Therefore

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\,\text{V}}{I_{C_{sat}}} = 0\,\Omega$$

the base–collector junction is no longer reverse-biased

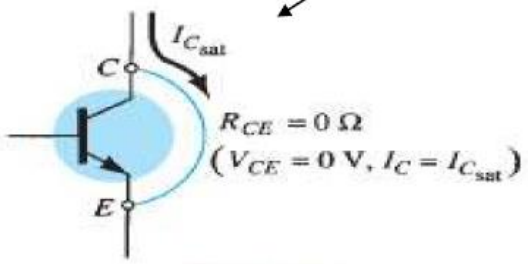

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FIG. 4.9 Determining I_{Csat}

The resulting saturation current for the fixed-bias configuration is

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \qquad (4.11)$$

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Load-Line Analysis:

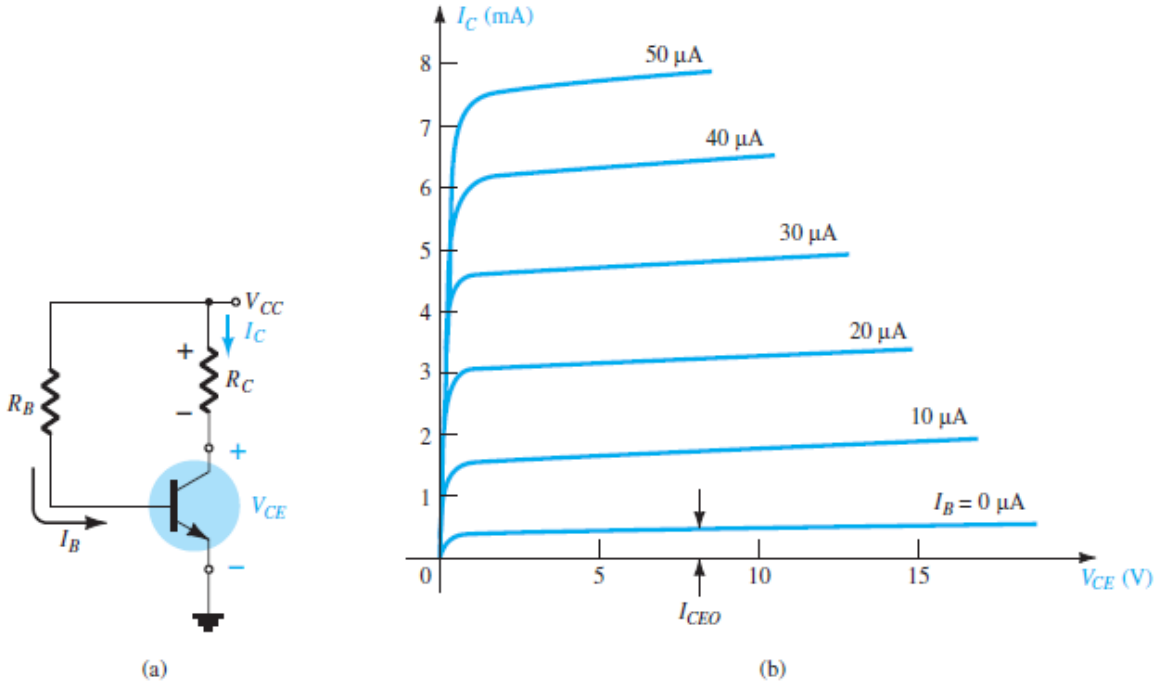


FIG. 4.11
Load-line analysis: (a) the network; (b) the device characteristics.

steeper the slope of the network load line. The network of Fig. 4.11a establishes an output equation that relates the variables I_C and V_{CE} in the following manner:

$$V_{CE} = V_{CC} - I_C R_C \tag{4.12}$$

The output characteristics of the transistor also relate the same two variables I_C and V_{CE} as shown in Fig. 4.11b.

The device characteristics of I_C versus V_{CE} are provided in Fig. 4.11b. We must now superimpose the straight line defined by Eq. (4.12) on the characteristics. The most direct method of plotting Eq. (4.12) on the output characteristics is to use the fact that a straight line is defined by two points. If we *choose* I_C to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. By substituting $I_C = 0$ mA into Eq. (4.12), we find that

$$V_{CE} = V_{CC} - (0)R_C$$

and

$$V_{CE} = V_{CC}|_{I_C = 0\text{ mA}} \tag{4.13}$$

defining one point for the straight line as shown in Fig. 4.12.

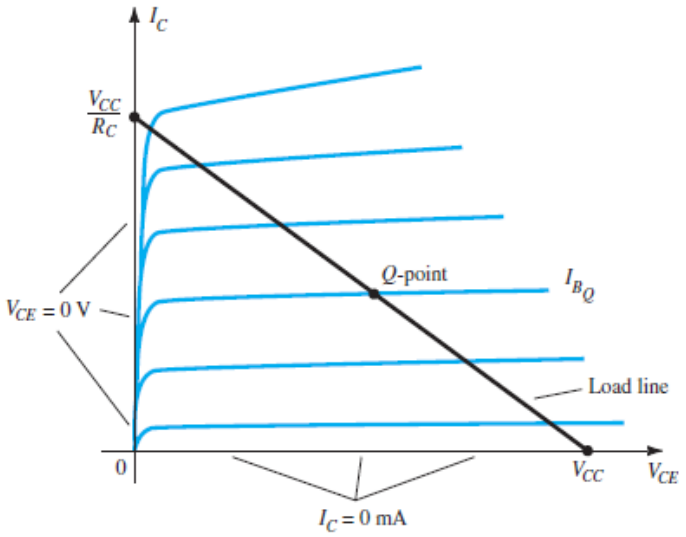


FIG. 4.12
Fixed-bias load line.

If we now *choose* V_{CE} to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that I_C is determined by the following equation:

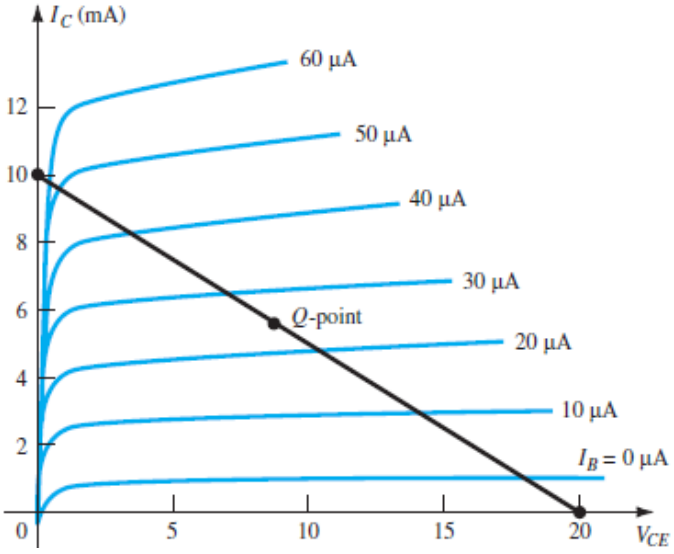
$$0 = V_{CC} - I_C R_C$$

and

$$I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE}=0\text{ V}} \qquad (4.14)$$

EXAMPLE 4.2:

Given the load line of Fig. 4.16 and the defined Q -point, determine the required values of V_{CC} , R_C , and R_B for a fixed-bias configuration.



Solution: From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\text{ V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\text{ V}}{10\text{ mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\text{ V} - 0.7\text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

4.4 EMITTER-BIAS CONFIGURATION:

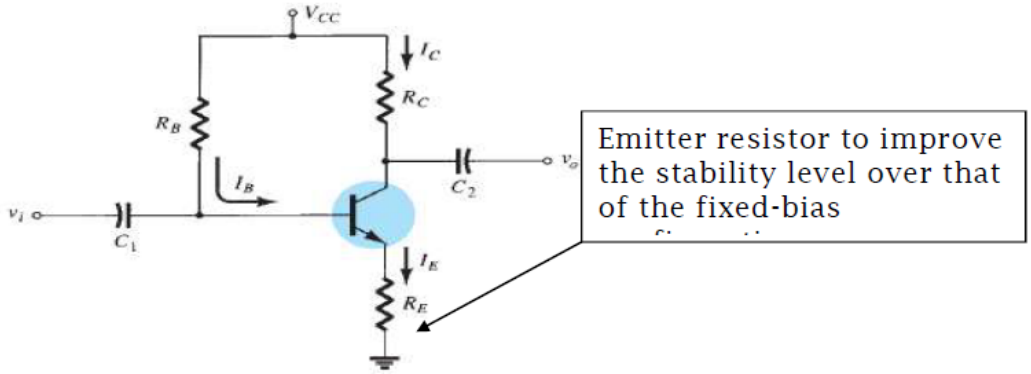


FIG. 4.17 BJT bias circuit with emitter resistor.

Base–Emitter Loop

The base–emitter loop of the network of Fig. 4.18 can be redrawn as shown in Fig. 4.19. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \qquad \textbf{(4.15)}$$

Recall from Chapter 3 that

$$I_E = (\beta + 1) I_B \qquad \textbf{(4.16)}$$

Substituting for I_E in Eq. (4.15) results in

$$V_{CC} - I_B R_B - V_{BE} - (\beta + I) I_B R_E = 0$$

Grouping terms then provides the following:

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (-1), we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

with

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

and solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \qquad \textbf{(4.17)}$$

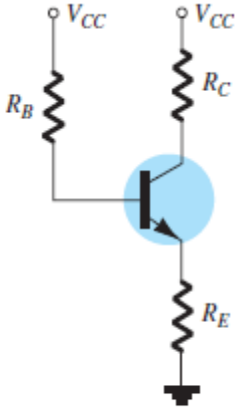


FIG. 4.18
DC equivalent of Fig. 4.17.

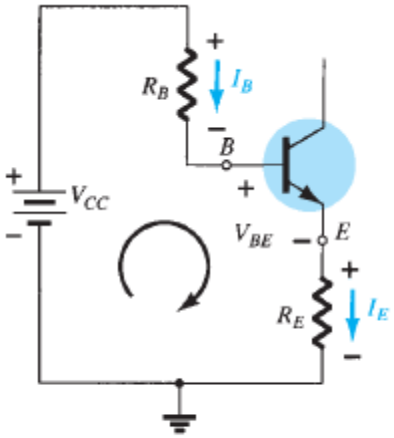


FIG. 4.19
Base–emitter loop.

Collector–Emitter Loop

The collector–emitter loop appears in Fig. 4.22. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \qquad (4.19)$$

whereas the voltage from **collector to ground** can be determined from
VCE = VC – VE

And VC = VCE + VE or **VC = VCC - ICRC**

The single-subscript voltage **VE** is the **voltage from emitter to ground** and is determined by **VE = IERE**

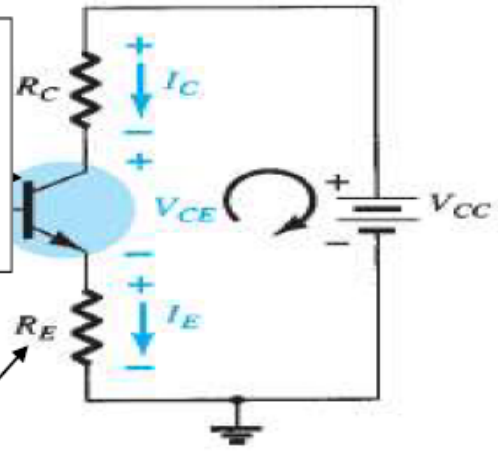


FIG. 4.22
Collector–emitter loop.

The voltage at the base with respect to ground can be determined using Fig. 4.18 **$V_B = V_{CC} - I_B R_B$** or **$V_B = V_{BE} + V_E$**

EXAMPLE 4.3 :

For the emitter-bias network of Fig. 4.23 , determine:

a. I_B . b. I_C . c. V_{CE} . d. V_C . e. V_E . f. V_B . g.V_{BC}

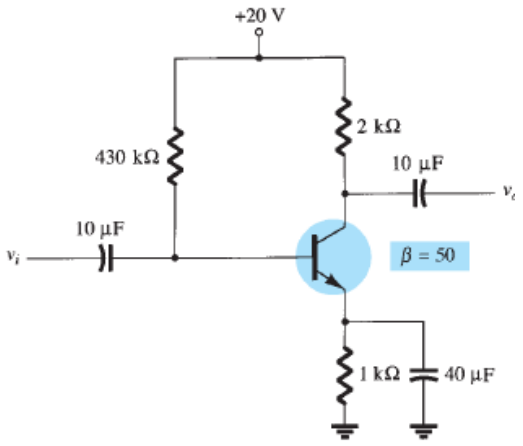


FIG. 4.23
Emitter-stabilized bias circuit for Example 4.4.

Solution:

a. Eq. (4.17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b. $$I_C = \beta I_B$$
$$= (50)(40.1\ \mu\text{A})$$
$$\cong \mathbf{2.01\ mA}$$

c. Eq. (4.19): $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$$
$$= \mathbf{13.97\ V}$$

d. $$V_C = V_{CC} - I_C R_C$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$$
$$= \mathbf{15.98\ V}$$

e. $$V_E = V_C - V_{CE}$$
$$= 15.98\text{ V} - 13.97\text{ V}$$
$$= \mathbf{2.01\ V}$$

or $$V_E = I_E R_E \cong I_C R_E$$
$$= (2.01\text{ mA})(1\text{ k}\Omega)$$
$$= \mathbf{2.01\ V}$$

f. $$V_B = V_{BE} + V_E$$
$$= 0.7\text{ V} + 2.01\text{ V}$$
$$= \mathbf{2.71\ V}$$

g. $$V_{BC} = V_B - V_C$$
$$= 2.71\text{ V} - 15.98\text{ V}$$
$$= \mathbf{-13.27\ V}\text{ (reverse-biased as required)}$$

Saturation Level:

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.24 and calculate the resulting collector current. For Fig. 4.24

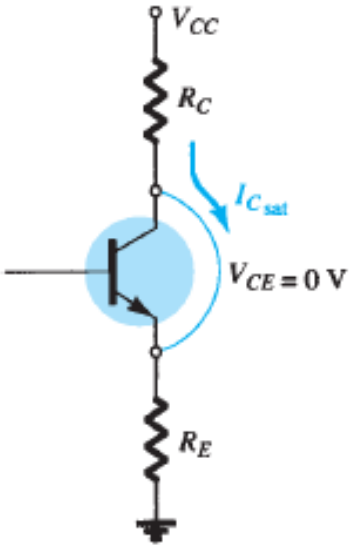


FIG. 4.24
Determining $I_{C_{sat}}$ for the emitter-stabilized bias circuit.

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} \qquad (4.25)$$

EXAMPLE 4.6 Determine the saturation current for the network of Example 4.4.

Solution:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$
$$= \frac{20\text{ V}}{2\text{ k}\Omega + 1\text{ k}\Omega} = \frac{20\text{ V}}{3\text{ k}\Omega}$$
$$= \mathbf{6.67\text{ mA}}$$

which is about three times the level of I_{C_Q} for Example 4.4.

Load-Line Analysis:

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of I B as determined by Eq. (4.17) defines the level of I B on the characteristics of Fig. 4.25 (denoted IBQ). The collector–emitter loop equation that defines the load line is

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

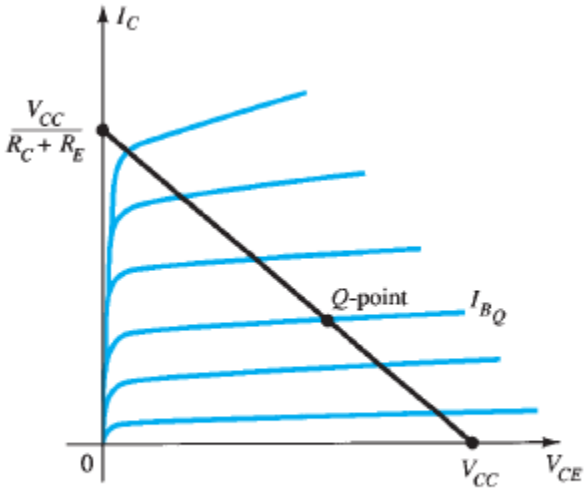


FIG. 4.25
Load line for the emitter-bias configuration.

Choosing $I_C = 0$ mA gives

$$\boxed{V_{CE} = V_{CC}\big|_{I_C=0\,\text{mA}}} \tag{4.26}$$

as obtained for the fixed-bias configuration. Choosing $V_{CE} = 0$ V gives

$$\boxed{I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE}=0\,\text{V}}} \tag{4.27}$$

as shown in Fig. 4.25. Different levels of I_{B_Q} will, of course, move the Q-point up or down the load line.