Al-Mustaqbal University

College of Engineering and Technology

Department of Computer Techniques Engineering

Class: Second Class

Subject: Computer Architecture

Lecturer: Assistant Lecturer Zainab Kadhum Jaber

Lecture Address: Overview of instruction execution cycle

2024 - 2025

E-mail: Zainab.kadum.jaber@uomus.edu.iq

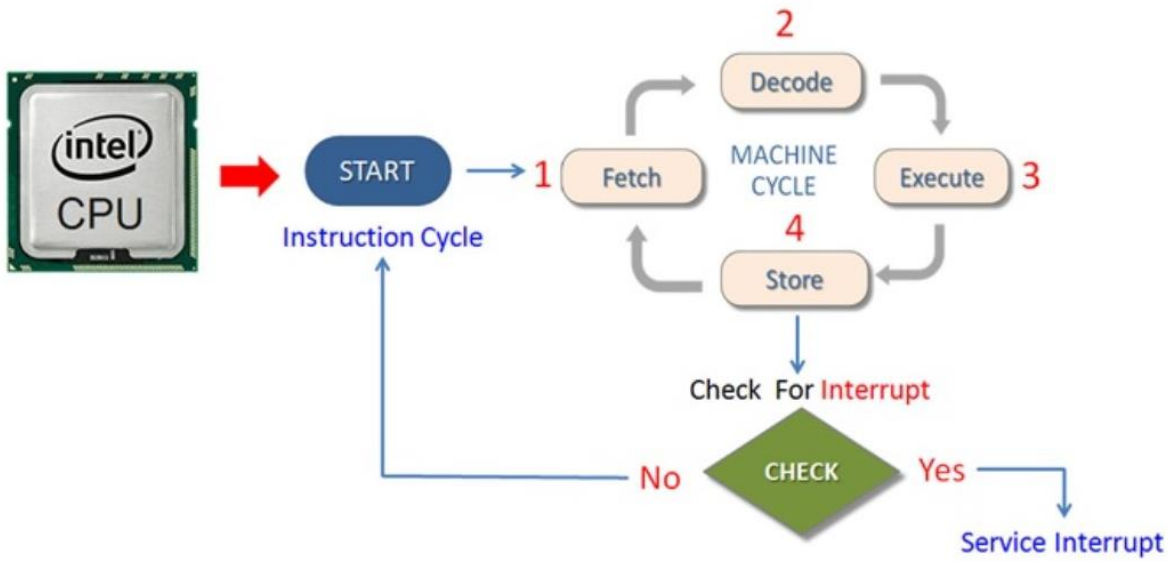
Instruction Cycle

Computer Organization And Architecture

The instruction cycle is the time required by the CPU to execute one single instruction. The instruction cycle is the basic operation of the CPU which consist of three steps.

The CPU repetitively performs fetch , decode , execute cycle to execute one program instruction. The machine cycle is part of the instruction cycle.

The computer system's main function is to execute the program. The computer program consist of set of instructions . The central processing unit (CPU) is responsible to execute these program instructions.



E-mail: Zainab.kadum.jaber@uomus.edu.iq

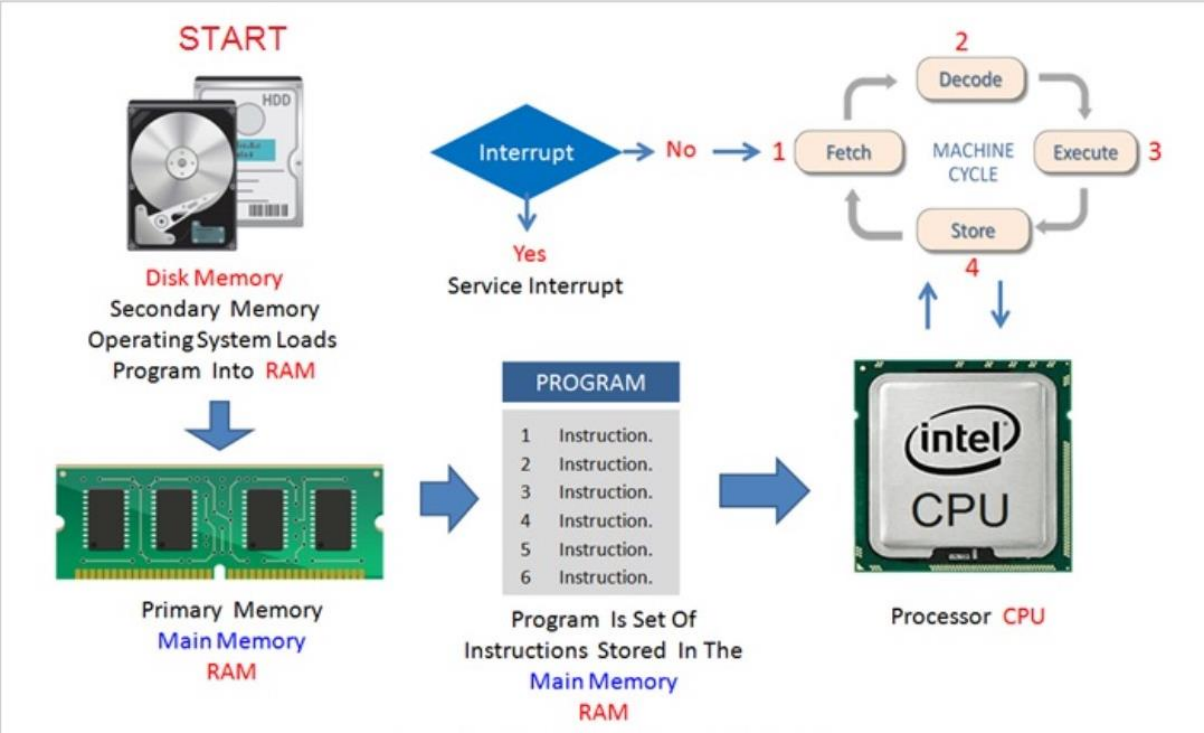
The program instructions are stored into the main memory RAM. The computer memory is organized into number of cells. Each cell (location) has a specific memory address.

The processor initiates the program execution by fetching the machine instructions one by one from the main memory RAM.

The CPU executes these instructions by repetitively performing sequence of four steps called instruction cycle. Each part of the instruction cycle requires number of machine cycles to complete that part.

In order to understand the instruction cycle , It is important to first understand some related topics before we start the discussion on the concept of instruction cycle.

How Computer Executes Program ?



E-mail: Zainab.kadum.jaber@uomus.edu.iq

Instruction Cycle

Computer Organization And Architecture

Table Of Contents

What Is Computer Program ?

The computer system needs a set of instructions which directs the computer to perform the desired operations. This set of instruction which computer can interpret and execute is called a computer program.

The computer program is an essential component of every computer system. The choice of the programming language depends upon the type of the software being developed.

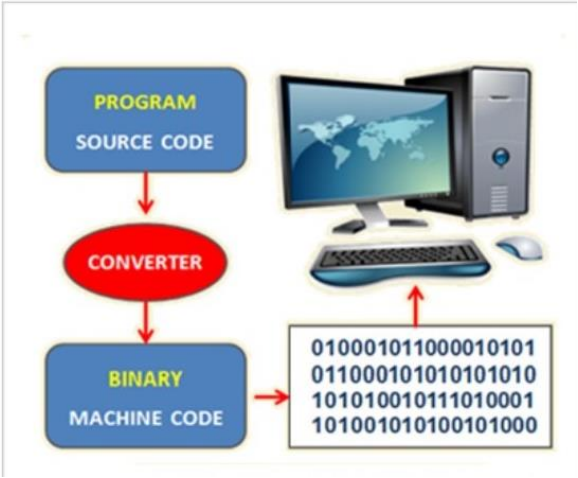
The application software are written using a high level programming languages. Some commonly used programming languages include C language , C ++ , Java , JavaScript and Python.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

Computer Program

```
int main()
{
// Variable declaration
int a, b, sum;
// Take two numbers as input from the
user
scanf("%d %d", &a, &b);
// Add the numbers and assign the value
// to  some variable
sum = a + b;
// Use the calculated value
printf("%d\n", sum);
return 0;
// End of program
}
```

Program Compilation



The computer program written in any high level programming language needs to be converted into machine readable format in binary.

The machine code instructions in binary is low level set of program instructions that can be directly executed by the computer system.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

Instruction Cycle

What Is Program Instruction ?

The computer program consist of a set of program statements also called as program instructions. Each program instruction performs a specific task.

The program instructions are machine instructions in binary format that CPU can directly execute. The operating system loads the machine instructions into the main memory RAM to initiate the program execution.

The CPU starts the program execution by fetching them one by one. The control unit decodes the machine instructions as per the instruction format.

The computer program use different types of program instructions as per the program logic and algorithm.

For example, the program instruction can either perform input and output operations or arithmetic calculations or some logical decision making operation.

Program Instructions

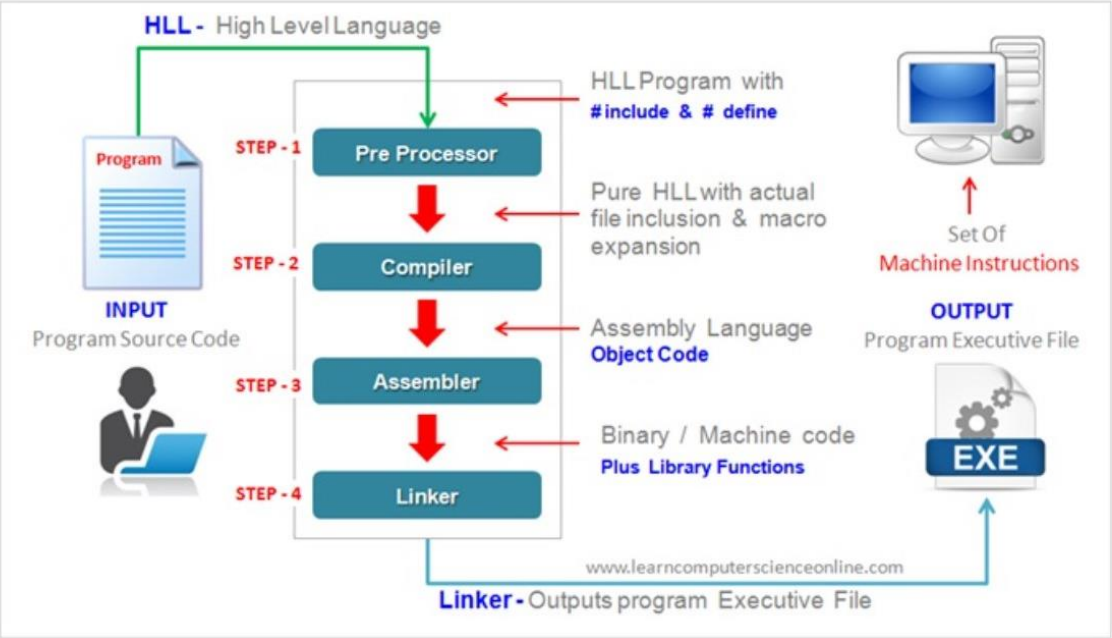
E-mail: Zainab.kadum.jaber@uomus.edu.iq

During the program compilation process , each program instruction is converted into machine instruction in binary.

Depending upon the type of the programming language , the program compiler converts the entire program into an executable code (set of machine instructions). In case of interpreted language , this conversion takes place line by line.

The executable code consist of set of machine instructions in binary that can be directly decoded and executed by the CPU.

Program Compilation



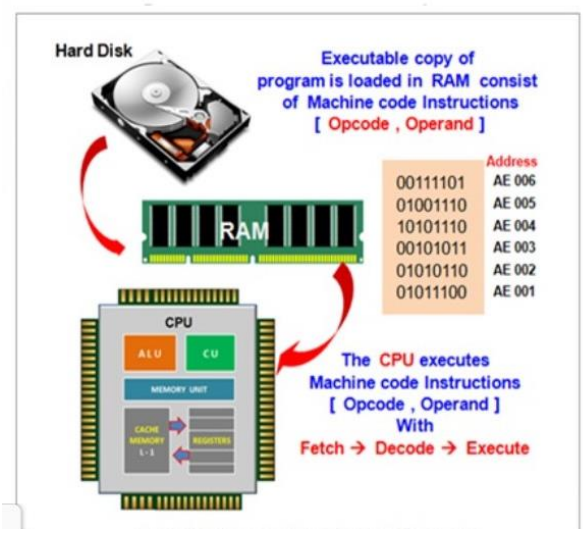
What Is Central Processing Unit ?

E-mail: Zainab.kadum.jaber@uomus.edu.iq

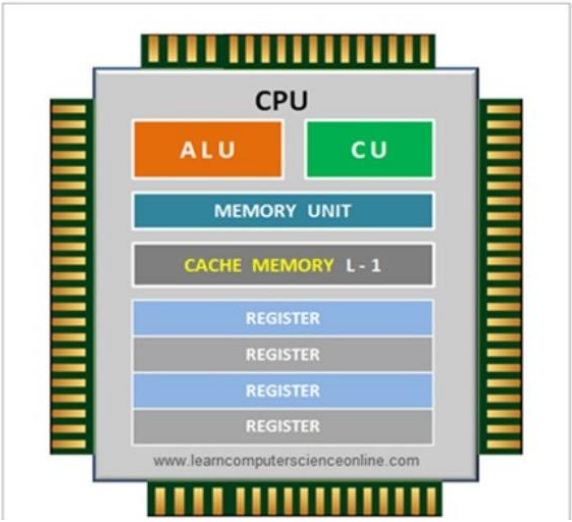
The central processing unit (CPU) is the brain and the processing engine of the computer system. The CPU provides the real processing power to the system.

The main function of the CPU is to execute the computer program and control all the operations performed by the computer system.

Program Execution



Microprocessor (CPU)



E-mail: Zainab.kadum.jaber@uomus.edu.iq

The CPU internally consist of number of units and each unit perform a specific task. The CPU internal units include Memory Unit (MU) , Arithmetic Logic Unit (ALU), and Control Unit (CU).

The CPU executes the computer program instructions by repetitively performing a process called machine cycle.

Read More

What Is Central Processing Unit (CPU) ?

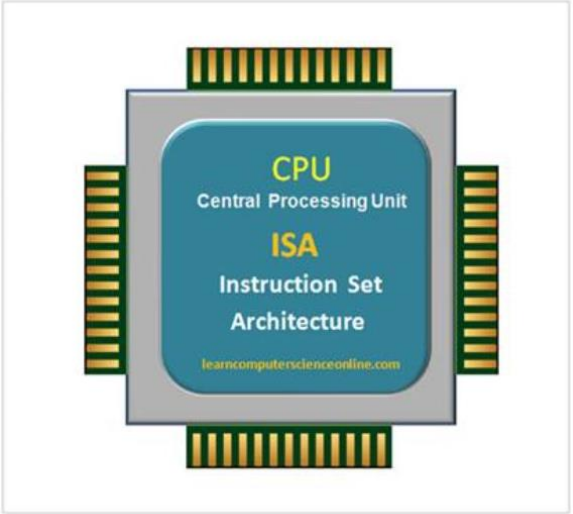
CPU Micro Architecture

CPU Instruction Set Architecture (ISA)

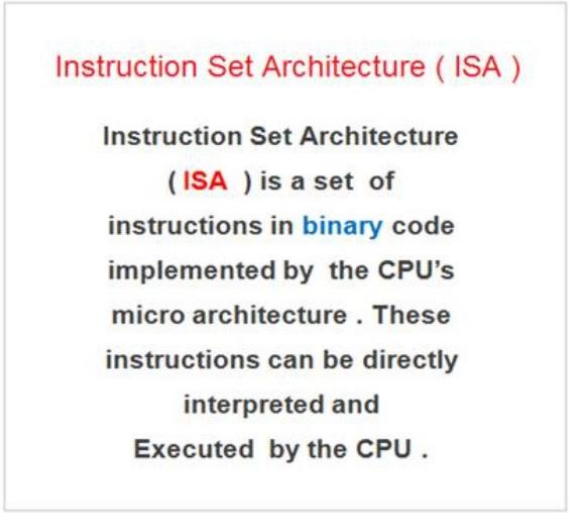
Each micro processor chip implements and supports a set of binary commands that the CPU can decode and execute .

This set of commands is hardwired into the microprocessor's circuitry during processor chip manufacturing process. This set of commands implemented by the CPU is called instruction set architecture (ISA).

Instruction Set Architecture



Instruction Set Architecture



E-mail: Zainab.kadum.jaber@uomus.edu.iq

And for this reason , the compiler compiles the program for a specific platform. The program compiler generates an executable code that can be executed on a specific platform.

Instruction Cycle

Instruction Format

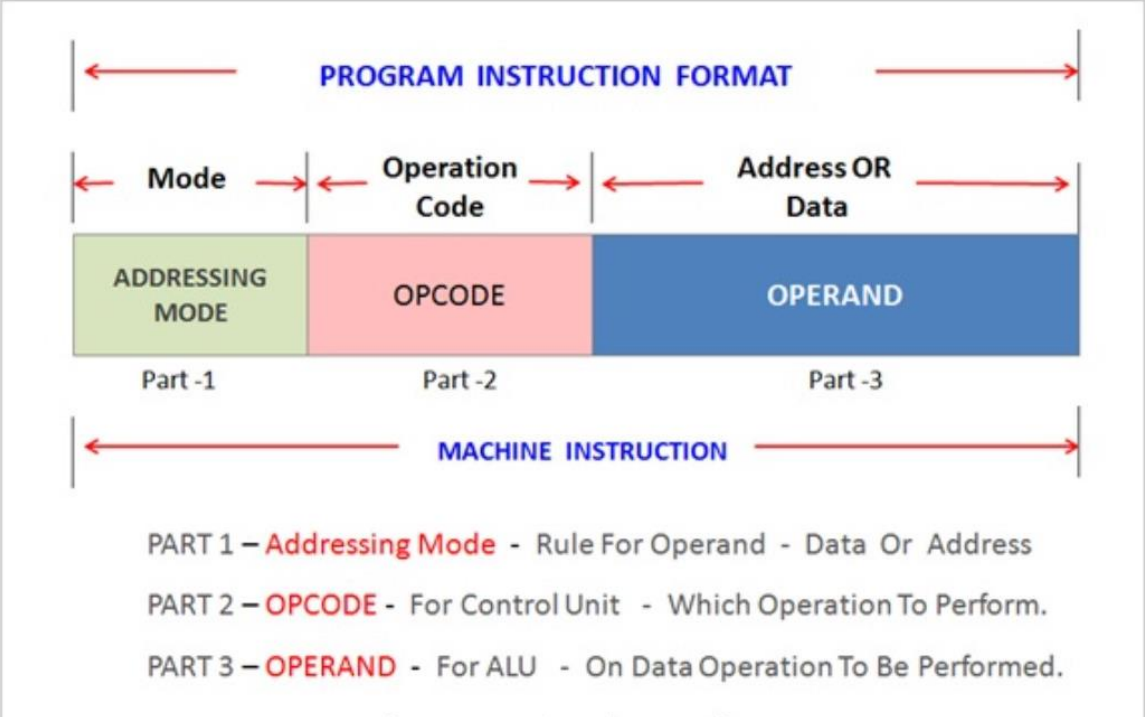
What Is Instruction Format ?

The computer program consist of number of instructions which directs the CPU to perform specific operation.

However , the CPU needs to know the details such as which operation is to be performed , on which data and the location of the data. This information is provided by the instruction format.

The CPU starts the program execution by fetching the program instructions one by one from the main memory RAM. The control unit of the CPU decodes the program instruction.

Program Instruction Format



E-mail: Zainab.kadum.jaber@uomus.edu.iq

The control unit of the CPU decodes the instruction based on the instruction format .

It is the instruction format which provides the details of the operation to be performed (opcode) , effective address of the operand and the data (operand) on which the operation is to be performed.

The instruction format defines the layout and structure of the program instruction that can be decoded by the CPU and then perform the desired operation on the data.

The instruction format essentially consist of three parts which includes OPCODE , OPERAND and the addressing MODE.

Machine Instruction Format

Addressing MODE | OPCODE | OPERAND

Instruction Format

What Is Operation Code ?

OPCODE

In microprocessor architecture the OPCODE is part of the machine instruction that specifies which operation is to be performed by the CPU while executing the instruction.

The OPCODE directs the control unit of the CPU to operate on the data (OPERAND) as supported by the instruction set architecture (ISA) of the processor chip.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

Instruction Format

What Is OPERAND ?

OPERAND

In microprocessor architecture the OPERAND simply means the data on which the CPU performs the desired operation.

The OPERAND is part of the machine instruction that specifies either the data itself or a reference to the data such as memory address which contains the actual data.

The CPU decodes the OPERAND part of the machine instruction as specified in the addressing mode. There are different types of addressing modes used in the instruction format.

Instruction Format

What Is Addressing Mode ?

ADDRESSING MODE

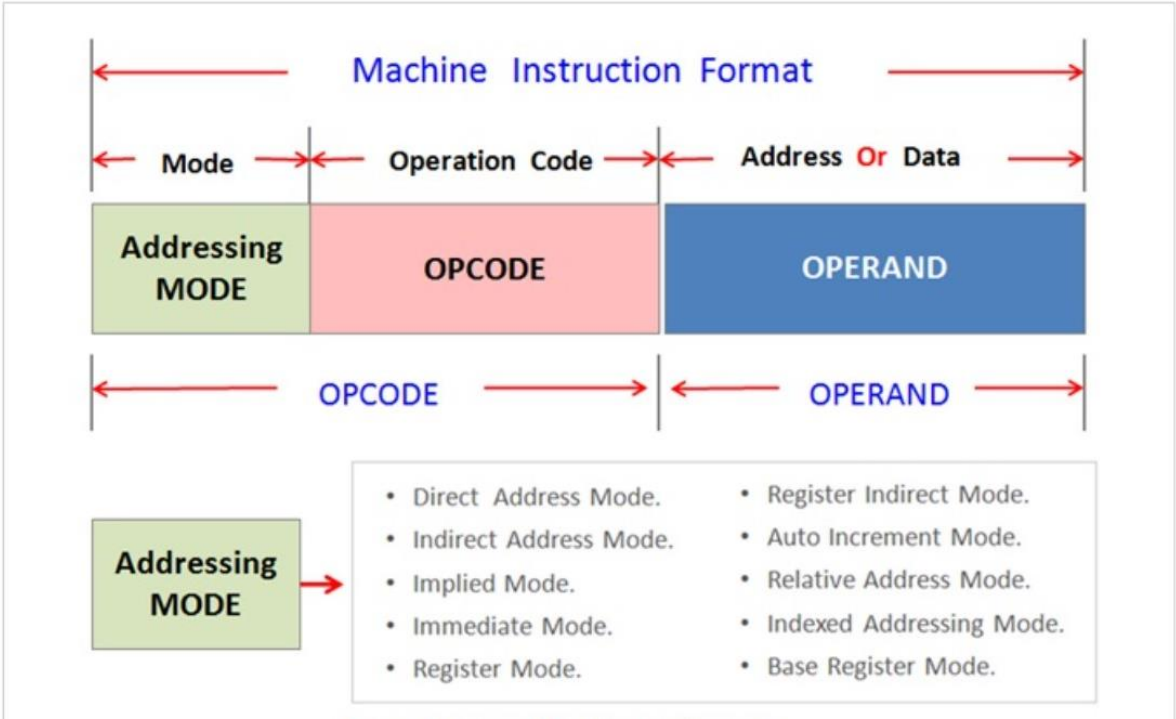
In microprocessor architecture, the addressing mode is part of the machine instruction that specifies the rules for the CPU while operating on the OPERAND part of the machine instruction.

The addressing mode part of the machine instruction format allows to specify whether the OPERAND value is a direct data Or It is an indirect referencing.

The OPERAND bits can either represent a direct value , or main memory address or CPU register number. It is the addressing mode that indicates the type of the OPERAND value.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

Instruction Format - Addressing Mode



E-mail: Zainab.kadum.jaber@uomus.edu.iq

If the addressing mode is specified as indirect then the OPERAND contains a memory address that points to the actual data.

The machine code instruction format can use ten different types of addressing modes depending upon the type of the instruction.

Machine Cycle

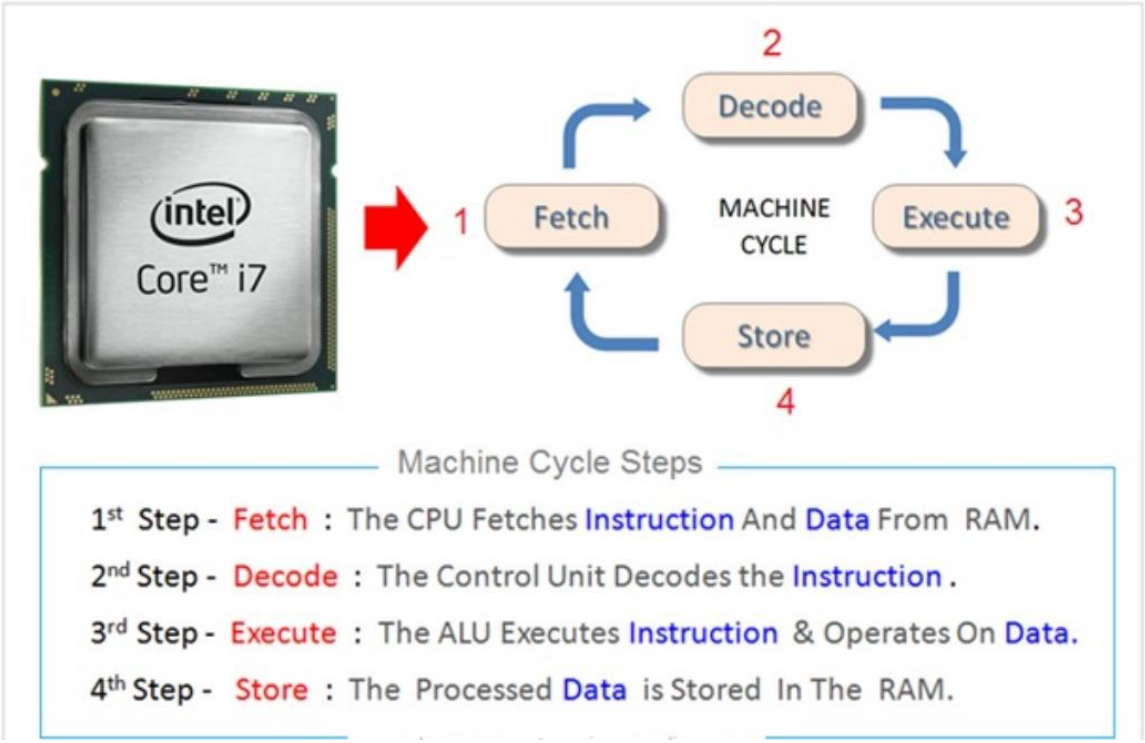
What Is Machine Cycle ?

The operating system loads the executable copy of the program code and the data that needs to be processed into the main memory RAM. The main memory contains the set of program instructions in the form of machine instructions .

The CPU is responsible to execute these machine instructions. In order to perform any task , the CPU has to repetitively perform a sequence of steps. These sequence of steps is called a machine cycle.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

Machine Cycle



The machine cycle is the basic operation of the microprocessor to perform any activity. For each part of the instruction cycle to complete specific number of machine cycles are required.

The CPU continuously performs the machine cycle in order to execute the program instructions one by one.

The instruction cycle consist of sequence of four steps. These four CPU operations includes Fetch , Decode , Execute and Store.

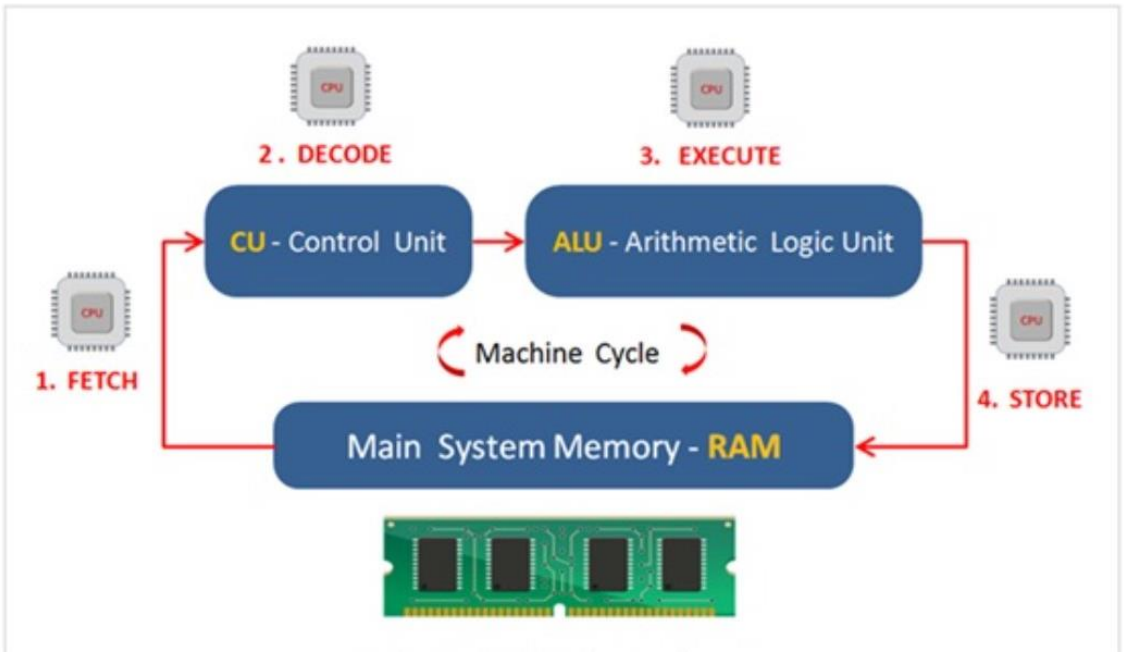
The CPU performs number of machine cycle rounds to complete fetch , decode, execute and store operations.

And therefore , In order to execute one single program instruction , the CPU might need one or more machine cycles . The number of machine cycles required depends upon the type and the CPU architecture.

For example, the both 8085 and 8086 will need different number of machine cycles to execute the same instruction.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

Machine Cycle Steps



Instruction Cycle

What Is Instruction Cycle ?

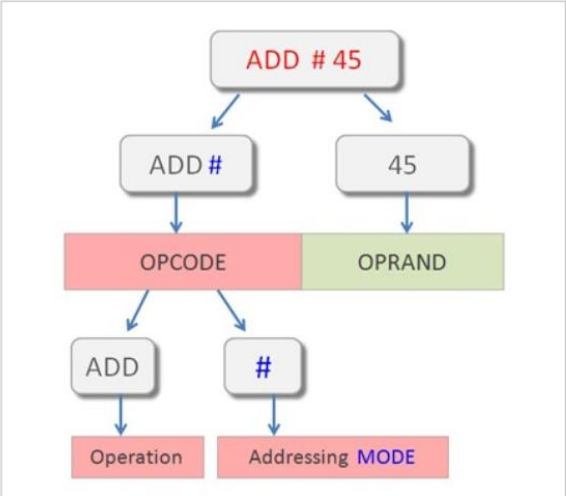
In simple words , the instruction cycle is the time taken by the CPU to fetch and execute one single machine instruction .

The computer program contains different types of instructions. Depending up on the complexity of the program instruction , the CPU might need one or more machine cycles to execute one single instruction.

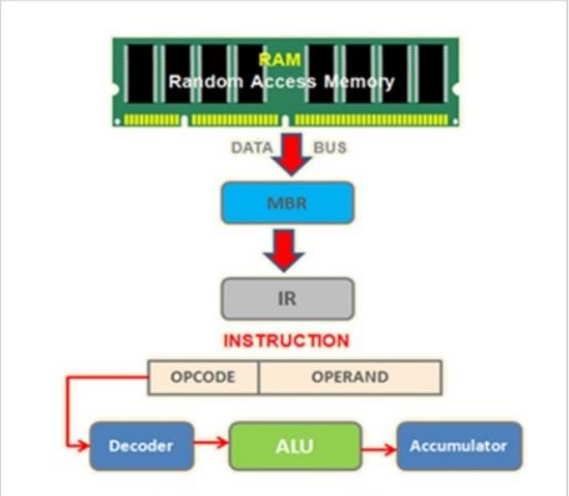
And therefore , the machine cycle is a part of the instruction cycle . However , in computing world , the machine cycle and instruction are used to indicate the instruction execution mechanism of the CPU.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

Instruction Format



Instruction Execution



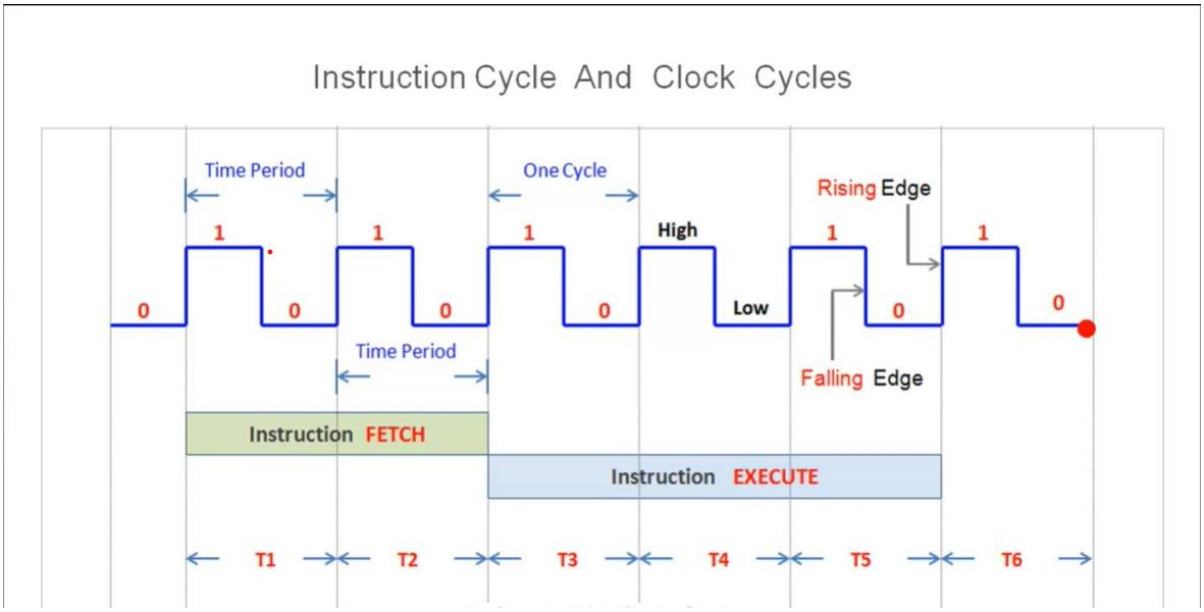
The processor is driven by an internal clock . This clock generates a steady stream of clock pulses. These analog clock signals are converted to the digital clock pulse (square wave).

The frequency of the clock that drives CPU is called the processor frequency. So , higher the frequency , faster will be the instruction execution speed of the processor (CPU).

For each clock cycle , the CPU completes a part of the execution process. This part instruction execution can either be a fetch , decode , execute or store operation.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

CPU Is Driven By Stream Of Clock Pulses



Each program instruction go through different execution phases. The CPU usually completes one instruction cycle in four clock cycles.

However ,depending upon the complexity , type of the instruction and addressing mode some instructions might take more clock ticks.

Instruction Cycle

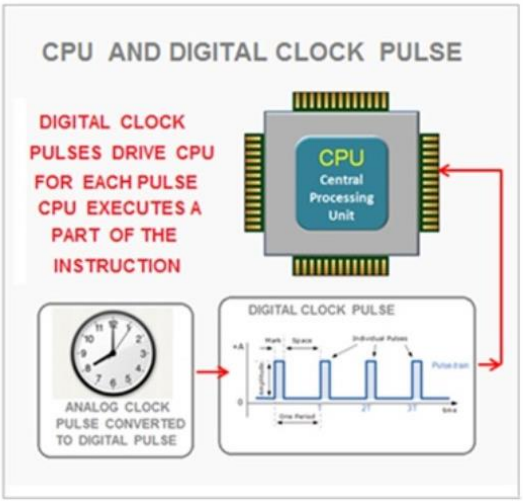
CPU Clock Speed And Instruction Cycle

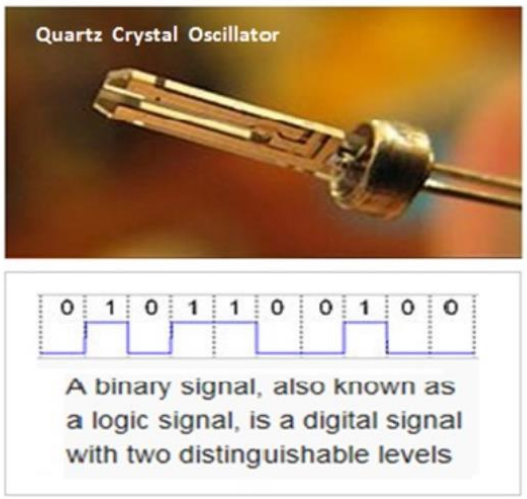
The processor is driven by an internal clock which generates the steady stream of clock pulses . For each clock pulse , the CPU performs part of the execution.

And therefore , faster the clock speed , faster will be the execution speed of the CPU. The clock speed is measured Hertz . The CPU speed is measured in Gigahertz (GHz).

E-mail: Zainab.kadum.jaber@uomus.edu.iq

CPU Clock Cycle





The microprocessor (CPU) speed depends upon the number of clock cycle needed to execute the instruction. A clock cycle is the time taken between the two pulses of an oscillator.

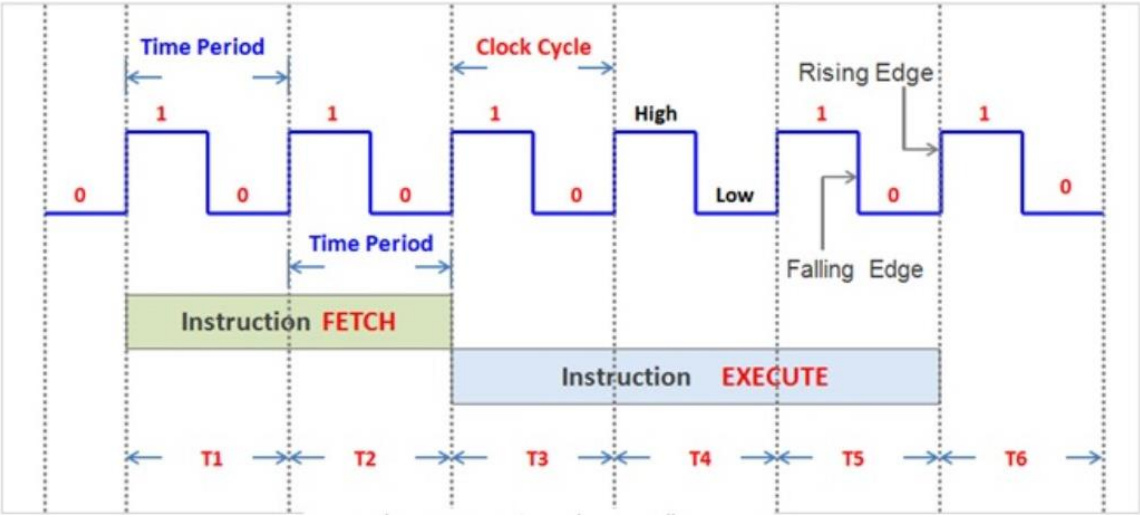
The processor will be able to work faster for higher number of clock pulses per second. The clock speed is measured hertz (Hz). The most commonly unit of clock speed in Megahertz (MHz) or Gigahertz (GHz).

For example , the processor with 3 GHz clock speed will perform 3,000,000,000 clock cycles per second. The processor speed also significantly depends upon other factors such as processor types and its micro architecture.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

CPU Clock Cycle

Instruction Cycle Steps



Pipelined Architecture

What Is Instruction Pipelining ?

The hardware industry is inventing new technologies to improve the processor speed. The processor speed has significantly improved since its inception.

The pipelined architecture or instruction pipelining has significantly improved the CPU speed. The instruction pipelining helps the CPU to process more number of instructions for the same number of clock cycles.

The CPU can execute the instructions in two modes. These two modes are pipelined and non-pipelined processing mode that depending upon the CPU architecture.

Instruction Cycle

- Instruction Pipelined Architecture.
- Instruction Non-Pipelined Architecture.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

What Is Instruction Pipelining ?

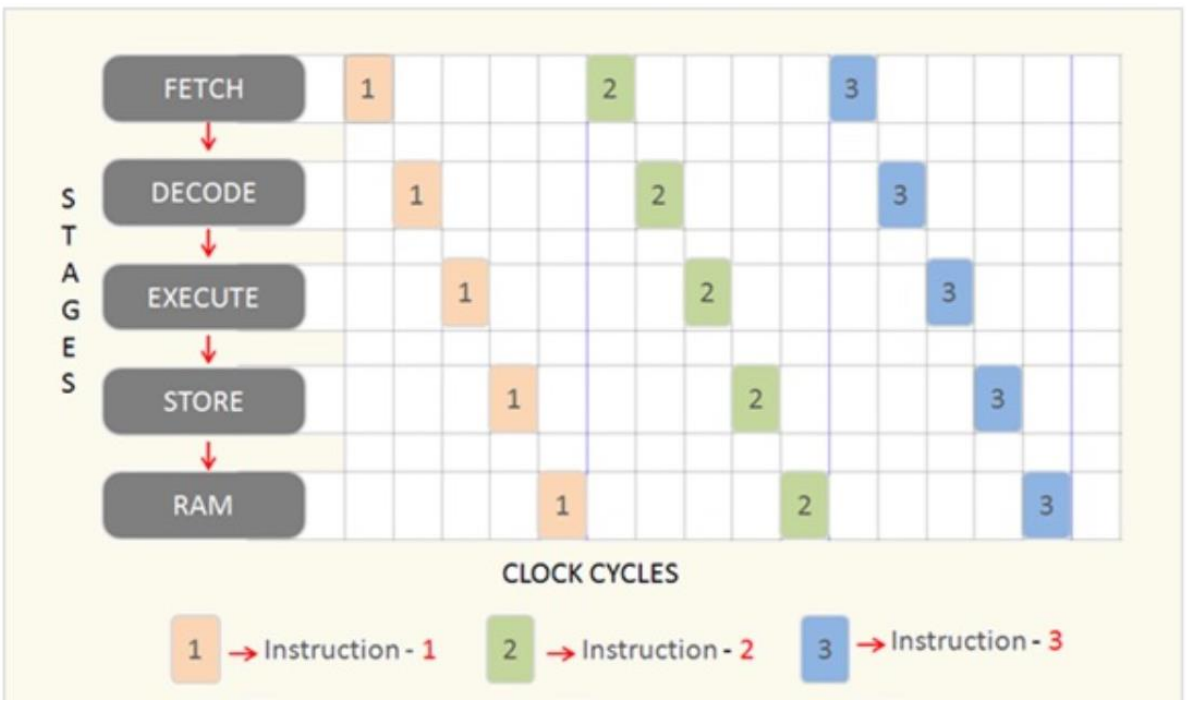
We can compare the concept of instruction pipelining that is similar to the technique used in production on the assembly line.

In assembly line, the production process is divided into suitable number of jobs for simultaneous production . This production methodology allows the faster production rate.

Similarly , in pipelined architecture , each instruction is divided into fixed number of stages such as fetch , decode and execute. For each clock cycle , the CPU completes one stage of the instruction.

The pipeline processing allows the CPU to simultaneously process number of instruction. And therefore , the CPU can execute the program instructions in less number of clock cycles.

Non-Pipeline Instruction Execution



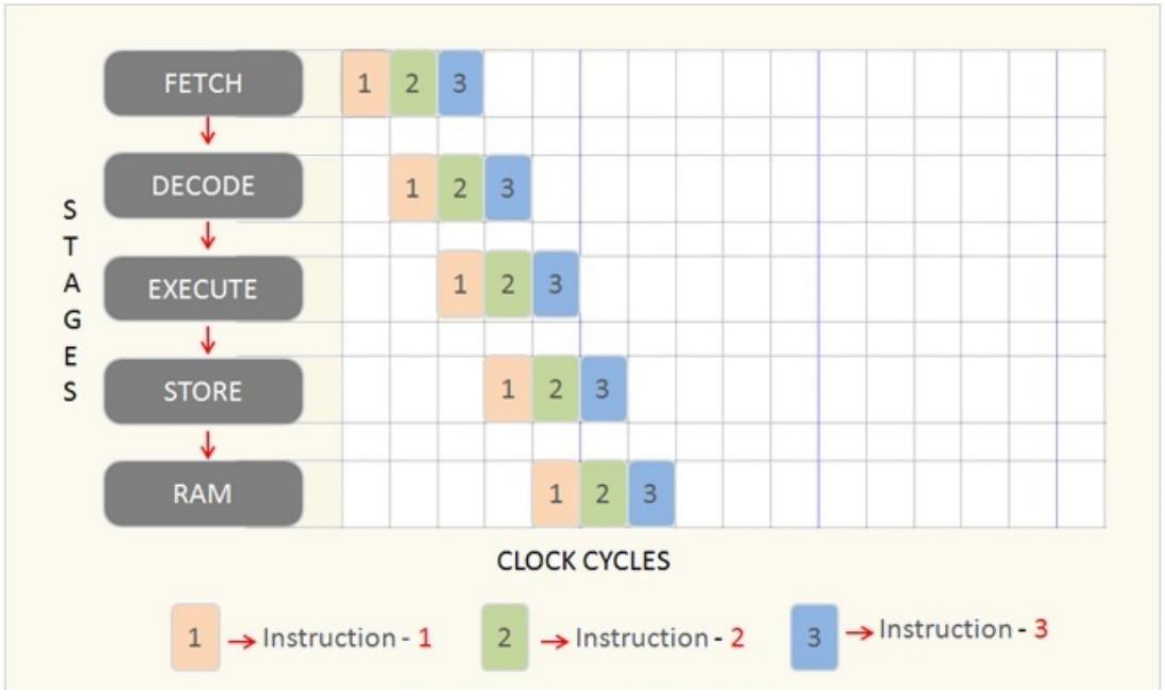
E-mail: Zainab.kadum.jaber@uomus.edu.iq

The CPU can process more number of instructions in parallel. Whereas, in non-pipelined architecture, the CPU executes only one instruction at a time. However , most modern processor supports the instruction pipelining.

In instruction pipelining , for each clock cycle , the CPU completes one part of the instruction. This could be either fetch operation , decode operation or execute operation.

One round of machine cycle needs twelve clock cycles. And one instruction cycle needs anywhere between one to four machine cycles depending upon the complexity of the instruction.

Pipeline Instruction Execution



E-mail: Zainab.kadum.jaber@uomus.edu.iq

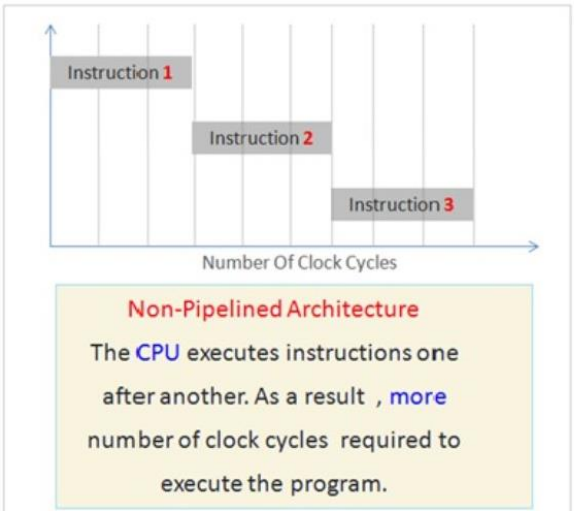
Instruction Cycle

What is Pipelined Architecture ?

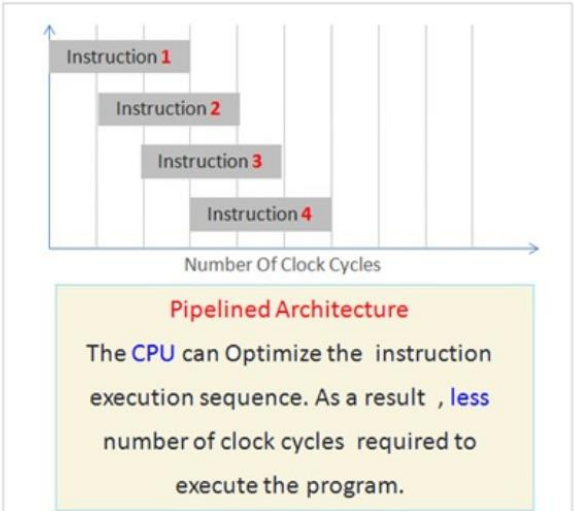
In pipelined architecture , the CPU can simultaneously process some part of the number of instructions in parallel.

And as a result , the CPU can optimize on the sequence of instruction execution. Therefore , in pipelined architecture , less number of clock cycles required to execute the same number of instructions.

Non-Pipelined Architecture



Pipelined Architecture



Instruction Cycle

What is Non-Pipelined Architecture ?

In non-pipelined architecture , the CPU can execute program instruction only one after another . The CPU lacks the ability to process number of instructions in parallel.

And as a result , the CPU cannot optimize on the sequence of instruction execution . For this reason in non-pipelined architecture , more number of clock cycles required to execute the same number of instructions as compared to pipelined instructions.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

Instruction Cycle

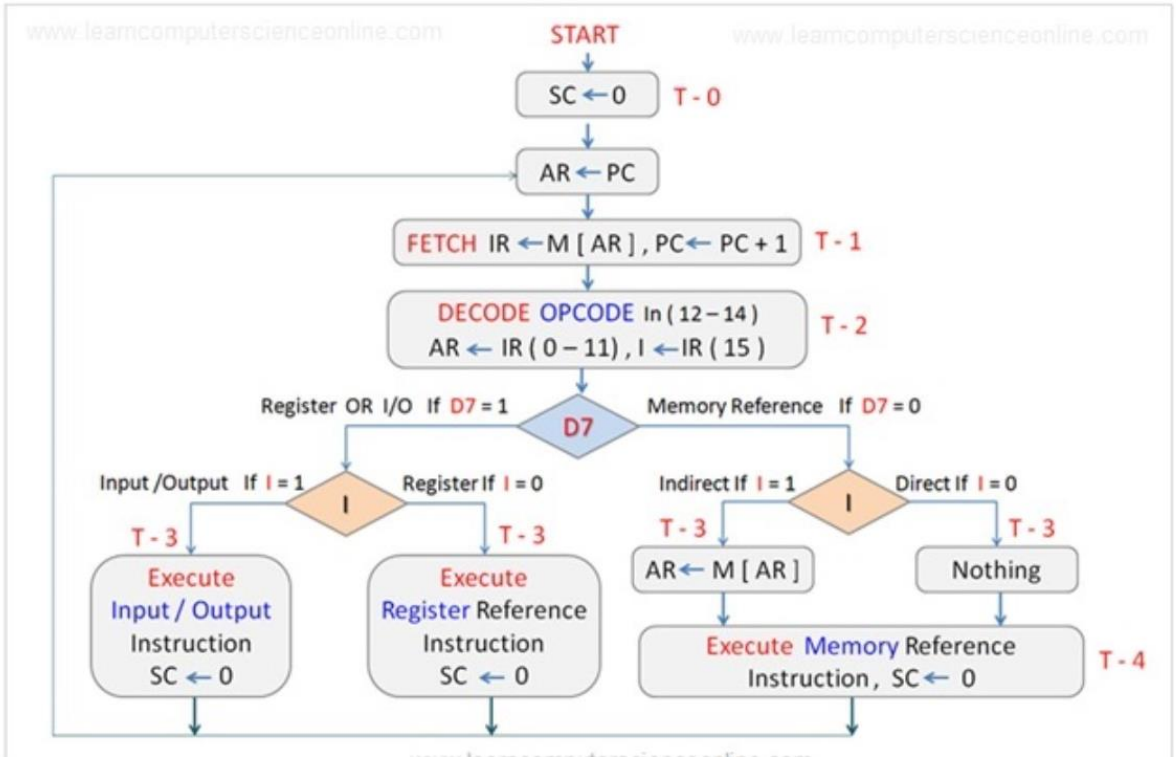
Fetch Decode Execute Cycle

Step-By-Step

Each instruction executed by the CPU goes through different phases at each clock cycle. Let us now take a closer look at the different phases of execution of the instruction cycle.

In order to understand the step by step execution of the instruction cycle, let us break the cycle into series of steps initiated by the CPU to execute one instruction.

Instruction Cycle Execution



E-mail: Zainab.kadum.jaber@uomus.edu.iq

Step - 1

Instruction Cycle Starts

The **first** phase of the instruction cycle is called a FETCH phase .The instruction cycle starts with the sequence counter (SC) initialized to zero.

SC <— 0

Step - 2

Fetch Phase - At Clock Pulse (T - 0)

The program counter (PC) register contains the address of the next instruction. In the first clock cycle (T- 0) the content (address) of the PC will be assigned to the address register (AR).

AR <— PC

Step - 3

Fetch Phase - At Clock Pulse (T - 1)

In the next clock cycle (T-1) , the instruction is fetched from the memory and brought to the instruction register (IR) and at the same time the program counter (PC) is also incremented by one.

The program counter (PC) now points to the memory location of the next instruction to be fetched.

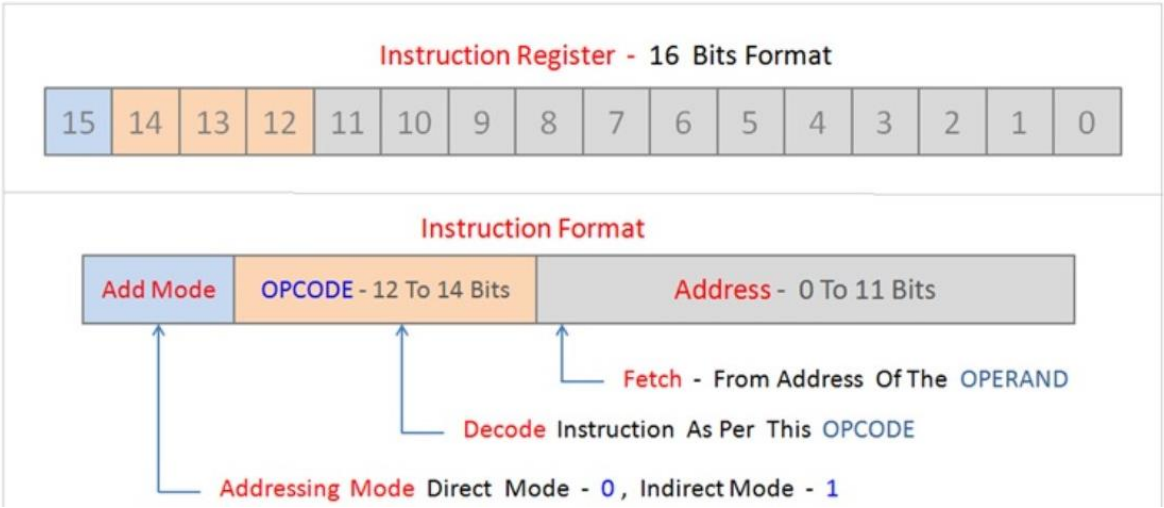
IR <– M [AR] AND PC <— PC + 1

The Instruction Register (IR) is a 16 Bit register that supports 16 bit format instruction.

The 16 bit instruction format has three parts that includes Addressing Mode (15th Bit) , OPCODE (12, 13, 14 Bit) And Operand Address (0 To 11 Bit).

Instruction Format (16 Bits)

E-mail: Zainab.kadum.jaber@uomus.edu.iq



Step - 4

Decode Phase - At Clock Pulse (T - 2)

The second phase of the instruction cycle is called a Decode Phase .The control unit of the CPU decodes the program instruction once it is fetched into the instruction register (IR) .

The instruction is decoded by the control unit of the CPU as per the operation code (OPCODE) specified by three bits (Bit 12 , 13, 14).

Step - 5

Decode Instruction Type - At Clock Pulse (T - 2)

The control unit of the CPU has to first decode the type of the instruction. The three types of instruction includes memory reference instruction , register reference instruction or input / output instruction.

The type of the instruction is decoded by the 3 X 8 decoder. The instruction type is decided by the value of the D7.

The three bit OPCODE can have 8 values starting from (D0, D1, D2, ..., D6 , D7) . In other words , the OPCODE can have values D0 – 000 To D7 – 111.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

Step - 6

Decode Addressing Mode - At Clock Pulse (T - 3)

If the value of D7 is 0 then type of instruction is memory reference type. If the value of D7 is 1 then the instruction type can either be register reference type or input / output instruction.

If the D7 = 1 and **I = 0** then the instruction type is register reference type. Else If the D7 = 1 and **I = 1** then the instruction type is Input / Output instruction type.

The decode phase ends after deciding the type of instruction and subsequent decision based on the value of **I** present in the 15^{th} bit.

For memory reference instructions , the decode operation decides the addressing mode of the instruction .

The addressing mode depends upon the value of I present in the 15^{th} bit of the instruction format. If this value **I = 0** then addressing mode is direct else the mode is indirect if **I = 1**.

The decode phase ends here and now the execution phase starts.

Step - 7

Execution Phase - At Clock Pulse (T - 4)

After completing the decode phase , the execution phase starts. In the execution phase of the instruction cycle , the processor performs the desired operation on the data (operand) placed in the accumulator register.

For both register reference and for input / output instruction the execution is straight forward . The processor performs the desired operation and the sequence counter (SC) is again initialized to zero .

Execute – **Register Reference** Instruction And SC <– 0

Execute – **Input And Output** Instruction And SC <– 0

For Memory reference instruction , the 15^{th} bit decides the direct or indirect execution depends upon the addressing mode.

For direct referencing **I = 0** and the processor executes the desired operation on the data fetched from the address (Bits 0 to 11) And the sequence counter (SC) is again initialized to zero.

E-mail: Zainab.kadum.jaber@uomus.edu.iq

However , for indirect referencing **I = 1** and effective address is first located . The processor then executes the desired operation on the data fetched from the effective address (Bits 0 to 11 points to effective address). And the sequence counter (SC) is again initialized to zero.

Execute – **Direct Memory Reference** Instruction And SC <– 0

Execute – **Indirect Memory Reference** Instruction And SC <– 0

Instruction Cycle

Halt Phase And Interrupt

After completing the execution phase of the instruction cycle the control again goes back to the Fetch phase where instruction cycle again starts.

The instruction cycle can go to halt phase after execution phase if it encounters a halt signal sent by the interrupt.

The processor attends the interrupt and then again resumes the instruction cycle execution.

E-mail: Zainab.kadum.jaber@uomus.edu.iq