Al-Mustaqbal University
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جامعة المستقبل
AL MUSTAQBAL UNIVERSITY

كلية العلوم
قسم الانظمة الطبية الذكية

Lecture: (6)

Subject: Arithmetic circuits
Level: First
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1. Arithmetic circuits

A combinational circuit is one where the output at any time depends only on the present combination. More complex combinational circuits such as adders and subtractors, multiplexers and demultiplexers, magnitude comparators, etc., can be implemented using a combination of logic gates.

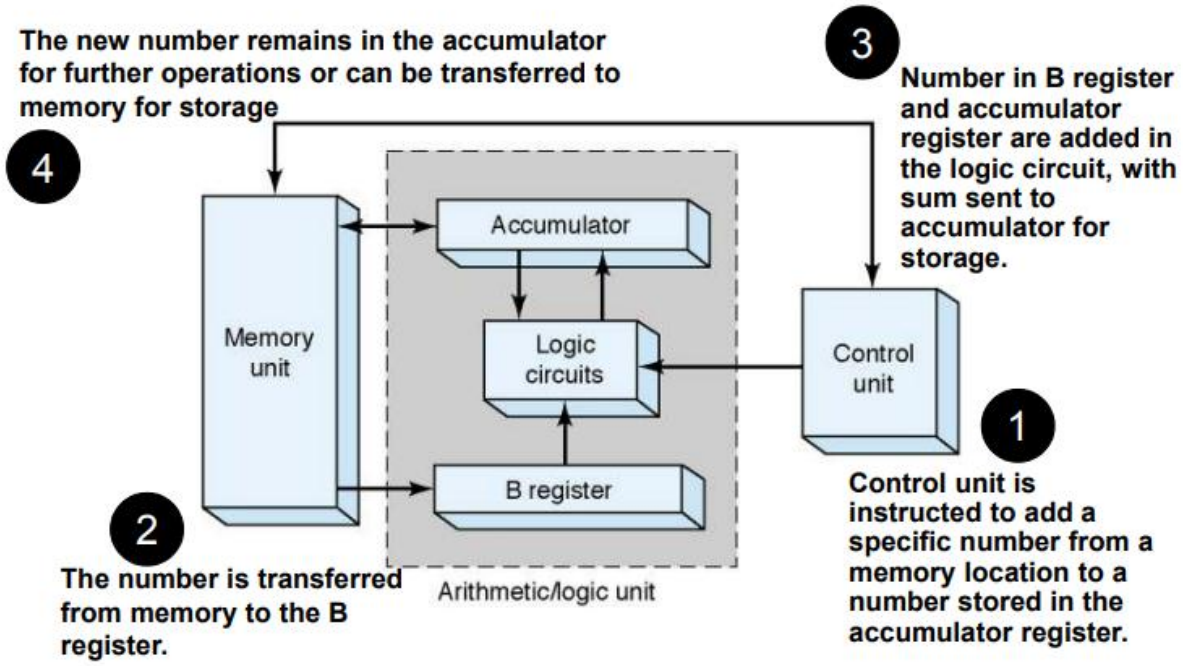


Fig. 1 Arithmetic Circuits Elements

2. Logic Circuits for Addition

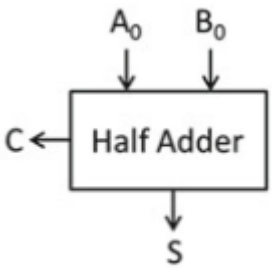
The most basic arithmetic operation is addition. The circuit, which performs the addition of two binary numbers is known as **Binary adder**. First, let us implement an adder, which performs the addition of two bits.

2.1 Half adder

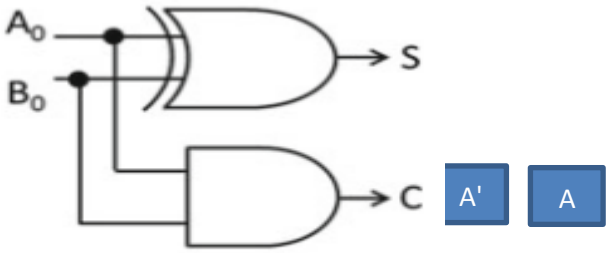
The logic circuit that adds two bits (A_0 and B_0) is **called half adder**. The rules of ***adding two 1-bit binary numbers are shown in the form of truth table*** in Fig. 2a. The simplified logic function for the truth table is obtained using K-map. The combinational logic circuit diagram for implementing the logic function is shown in Fig. 2b. The block diagram of half adder is shown in Fig. 2c, K-maps for sum and carry along with the logic diagram are shown in figure 2.

Inputs		**Outputs**	
A_0	B_0	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(a)Truth Table



(c) Block diagram



(b) Logic diagram

A' A B'

B \ A	0	1
0	0	0
1	0	(1)

(d) K-map for Carry

B \ A	0	1
0	0	1
1	1	0

(e) K-map for Sum

Fig. 2 Half adder

Boolean expression for Sum

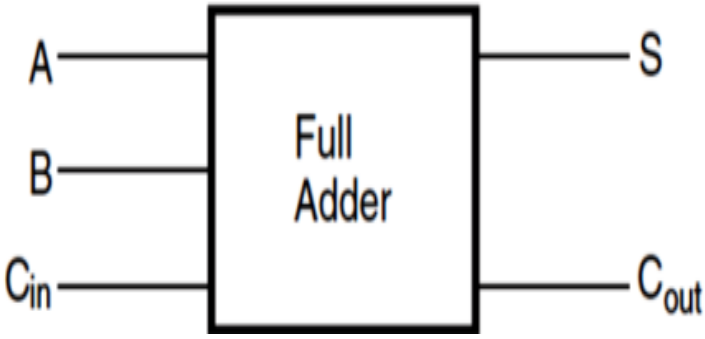
$$Sum = A\overline{B} + \overline{A}B = A \oplus B$$

Boolean expression for Carry

$$Carry = A.B$$

2.2 Full adder

Full adder is a combinational circuit, which performs the **addition of three bits** A, B and C_{in}. Where, A & B are the two parallel significant bits and C_{in} is the carry bit, which is generated from previous stage. This Full adder also produces two outputs sum, S & carry, C_{out}, which are similar to Half adder.



The **Truth table** of Full adder is shown below figure 3.

Input			Output	
A	**B**	**C_{in}**	**C_{out}**	**S**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(c) Block Diagram for Full adder

(a) Truth table

Fig. 3 Full Adder

C_{in} \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

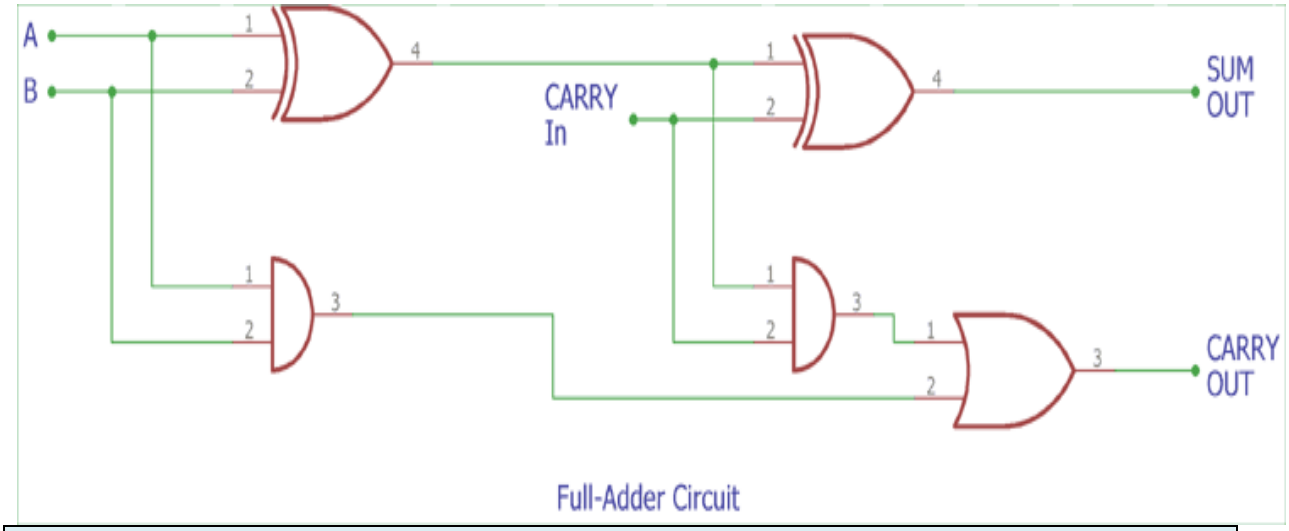
k-map for S output

C_{in} \ AB	00	01	11	10
0	0	0	1	0
1	0	1	1	1

k-map for C_{out} output

(b) Logic circuit for Full adder.

The Boolean algebra of Full adder is:



Full-Adder Circuit

$$C_{out} = AB + C_{in}A\bar{B} + C_{in}\bar{A}B$$

$$= AB + C_{in}(A \oplus B)$$

$$S = \overline{AB}C_{in} + A\,B\,C_{in} + \bar{A}\,B\,\overline{C_{in}} + A\,\overline{BC_{in}}$$

$$= C_{in}(\overline{AB} + A\,B) + \overline{C_{in}}(\bar{A}\,B + A\,\bar{B})$$

$$= C_{in}(\overline{A \oplus B}) + C_{in}(A \oplus B)$$

$$= C_{in} \oplus A \oplus B$$

2.3 Binary Adder

The registers play an important role in performing the micro-operations. The registers hold the digital component and the data which performs the arithmetic operation. The Binary Adder is a logical circuit which is used to perform the addition operation of two binary number of any length.

The Binary Adder is formed with the help of the Full-Adder circuit. The Full-Adders are connected in series, and the output carry of the first Adder will be treated as the input carry of the next Full-Adder.

2.3.1 N-Bit Parallel Adder

The Full Adder is used to sum two single-bit binary numbers with carry input. In digital calculation, we need to add two n-bit binary numbers rather than only single-bit binary numbers. For this purpose, we need to use n-bit parallel Adder. In order to get N-bit parallel adder, we cascade the n number of Full Adders. The carry output of the first Adder is treated as the carry input of the second Adder.

4-bit Binary Adder

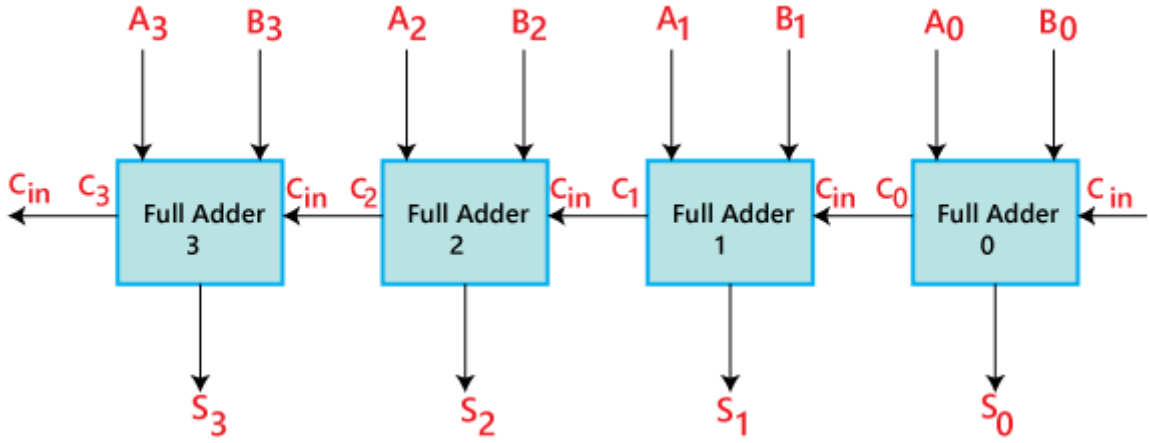


Fig.(4) 4-bit binary Parallel adder

- The 'A' and 'B' are the augend, and addend bits are defined by the subscript numbers. The subscripts start from right to left, and the lower-order bit is defined by subscript '0'.
- The C0, C1, C2, and C3 are the carry inputs which are connected together as a chain using Full Adder. The C4 is the carry output produced by the last Full-Adder.
- The C_{out} of the first Adder is connected as the C_{in} of the next Full-Adder.
- The S0, S1, S2, and S3 are the sum outputs that produce the sum of augend and addend bits.
- The inputs for the input variable 'A' and 'B' are fetched from different source registers. For example, the bit for the input variable 'A' comes from register 'R1', and a bit for the input variable 'B' comes from register 'R2'.
- The outcome produced by adding both input variables is stored into either third register or to one of the source registers.

2.4 Fast Adder

Consider 4-bit fast adder circuit for adding two 4-bit binary numbers. The construction of 4-bit fast adder is similar to 4-bit parallel adder. Full adders are cascaded in fast adder also. The carry inputs that would be generated during the addition of the 4-bit numbers are made available in advance (ahead) to the full adders before loading the numbers to the full adders. Additional logic circuit is used to generate the carry inputs in advance. The additional logic circuit is called **look-ahead carry logic circuit**. The binary numbers are then loaded to the full adders. Addition is performed on the binary numbers with minimum gate delay as the full adders need not wait for carry input from previous full adders. Fast adder is also called look-ahead carry adder. The derivation of the logic function for implementing the look-ahead carry logic circuit for the addition of two 4-bit numbers is presented. The derivations are based on carry generation and carry propagation.

Bubble Sheet Questions

Q1. What is the primary function of a Full Adder in binary addition؟

a. To perform the addition of two bits
b. To generate the carry bit
c. To find the average of two bits
d. To subtract two bits

Answer: b. To generate the carry bit

Q2. Which combinational logic circuit adds two bits and produces two outputs: sum (S) and carry-out (Cout)؟

a. Half Adder
b. Full Adder
c. N-Bit Parallel Adder
d. Fast Adder

Answer: b. Full Adder

Q3. In an N-Bit Parallel Adder, how are the Full Adders connected?

a. In series
b. In parallel
c. With additional logic gates
d. Using subtraction

Answer: a. In series

Q4. What is the primary advantage of a Fast Adder (look-ahead carry adder) compared to a regular N-Bit Parallel Adder؟

a. It performs subtraction faster.
b. It generates carry inputs in advance, reducing gate delay.
c. It is more efficient for addition of large binary numbers.
d. It has a smaller number of logic gates.

Answer: b. It generates carry inputs in advance, reducing gate delay.

Q5. In binary addition, what is the role of a Combinational Circuit؟

a. To store intermediate results
b. To perform the addition of two bits
c. To generate carry inputs
d. To produce the final sum and carry-out

Answer: b. To perform the addition of two bits