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قسم الانظمة الطبية الذكية

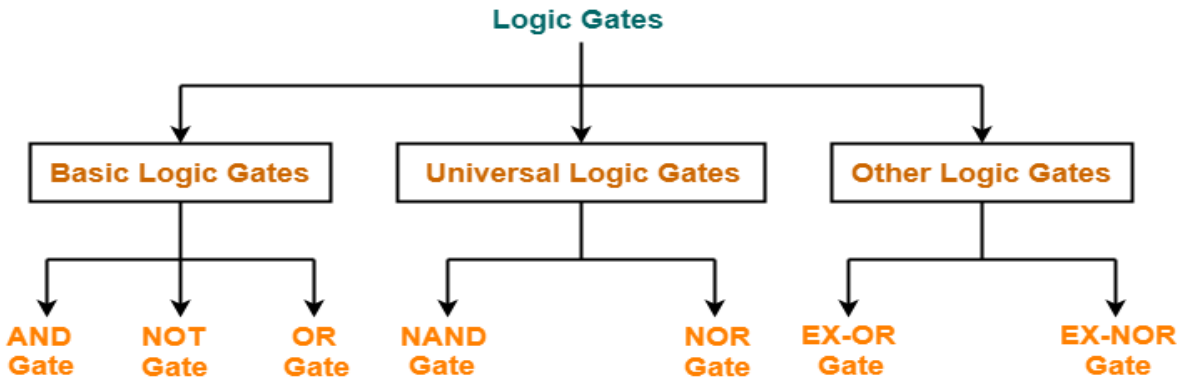
Lecture: (2)

Subject: Logic Gates
Level: First
Lecturer: Dr. Ahmad T. Jaiad

Logic Gates

Introduction

Logic gates are the basic building blocks of digital hardware. The following **categories of logic gates** are explained:



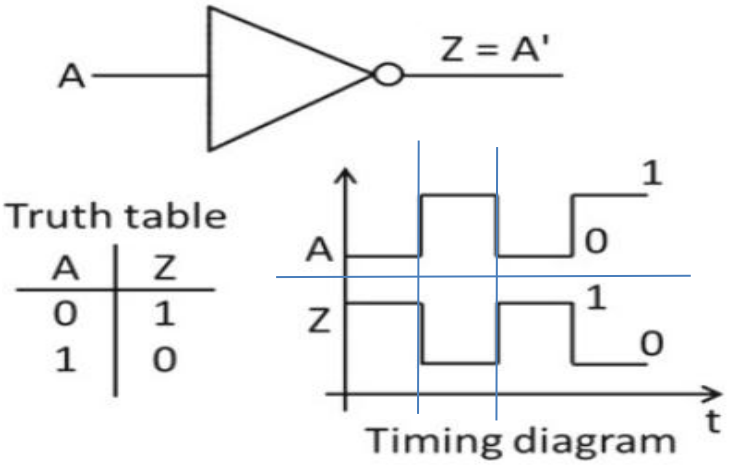
Types of Logic Gates

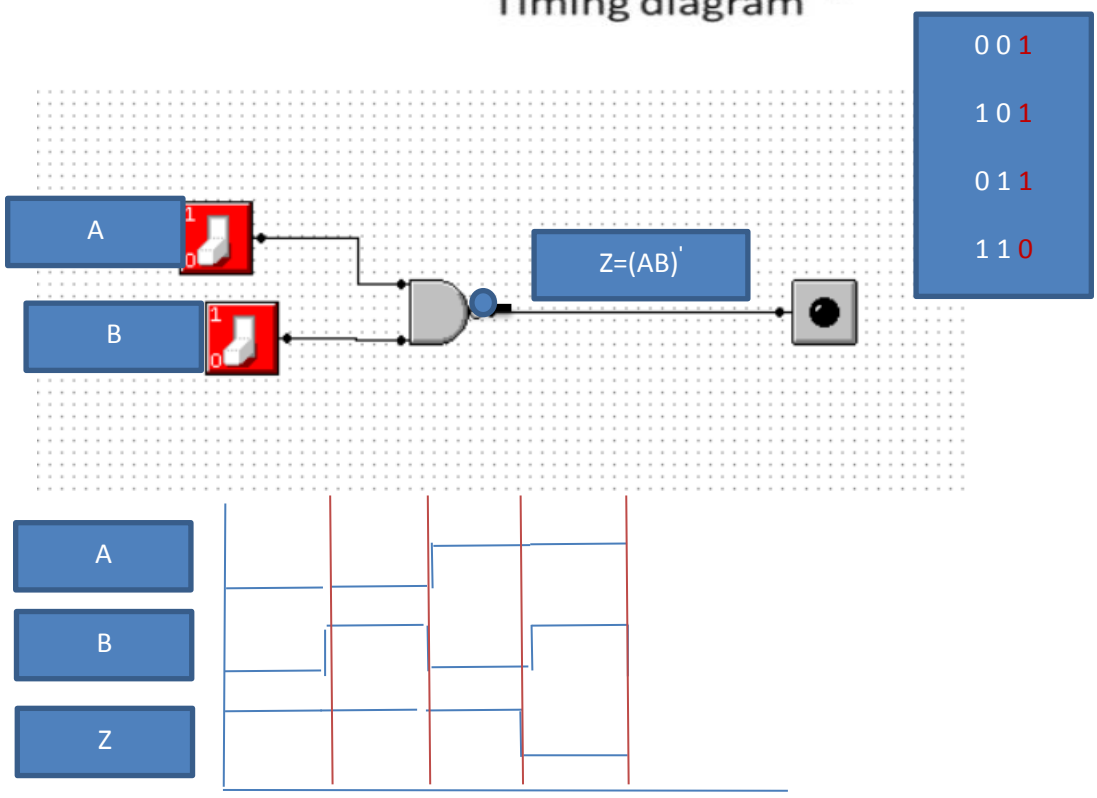
1. Basic Logic Gates

Transistor switching circuits that perform logical OR, AND and NOT operations are grouped as basic logic gates. Standard ICs are available for the basic logic gates. The datasheets of the ICs could be referred for the transistor switching circuit diagrams of OR, AND and NOT gates. The operations of the basic logic gates are presented using *Boolean algebra, truth table and timing diagram*. The standardized symbols for the gates are also indicated.

1.1 NOT Gate (Inverter)

NOT gate is generally known as inverter. It has one input and one output. The standardized symbol for inverter, the input (A), the output (Z), truth table and timing diagram of the gate are shown in Fig. 1. The output is **High** when the input is Low. The output is Low when the input is High. ICs for inverter are available with many configurations. The input and output are related by,





A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 1 Inverter with input and output signals

$$Z = A'$$

1.1.1 Active High and Active Low Input Signals

A logic gate is said to be asserted when logic 1 signal is applied to the input port of the gate. The logic 1 signal is called ***active High input*** signal to the logic gate. The application of active High input signals to 2-input AND gate is shown in Fig. 2a. The output of the AND gate is 1 when A and B are equal to 1. Active High input signal is also called positive logic input signal.

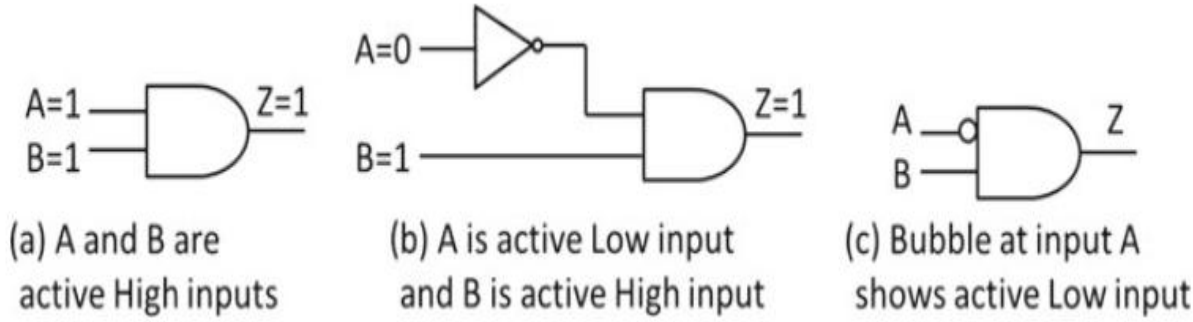


Fig.2 Active High and Active Low assertions

The AND gate in Fig. 2 could be asserted by applying logic 0 signal through inverter to the input of the gate. The schematic diagram for asserting the 2-input AND gate with logic 0 signal at A and logic 1 (active High) signal at B is shown in Fig. 2 b. The output of the AND gate is 1 with A = 0 and B = 1. The input logic 0 signal at A is called ***active Low input signal*** to the AND gate. Active Low input signal is also called ***negative logic input signal***.

The general representation of 2-input AND gate with active High and Low inputs is shown in Fig. 2c. The active Low input signal is indicated with a bubble at the input of the AND gate. The inverter is omitted in the representation.

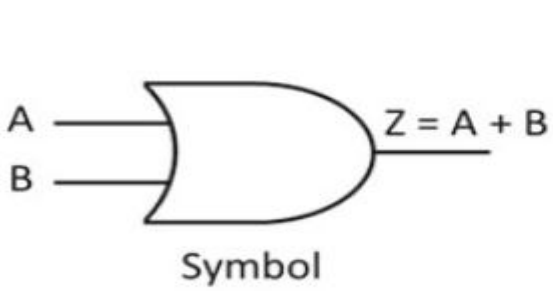
1.1.2 Bubbled Output

2-input AND gate is shown with bubble at the output of gate in Fig.3. It indicates the output of the gate is inverted i.e. ***active Low signal***. The datasheets of ICs for digital hardware use bubbles or triangles for indicating active Low signal at the inputs or outputs, as applicable. The triangle symbol is as per IEEE and IEC standards.

Fig. 3 AND gate with bubble at its output

1.2 OR Gate

OR gate has two or more input variables and the gate has one output. OR gate with two input variables (A & B), the output (Z) and the standardized symbol of the gate are shown in Fig. 4. The inputs and output are related by,



Truth table

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

Fig. 4 OR gate with two inputs

$$Z = A \; OR \; B = A + B$$

1.2.1 Truth Table

Truth table shows the relationship between the inputs and output of OR gate for all the combination of input variables. The output of OR gate is tabulated for the combinational inputs in truth table using Boolean algebra. The number of combinational inputs (c) is related to the number of input variables (n) to OR gate and it is given by:

$$c = 2^n$$

If the number of input variables (n) is **two**, the number of combinational inputs is **four**. If the number of input variables (n) is **three**, the number of combinational inputs is **eight**. The truth table for 3-input OR gate is shown in Fig.5. The truth table for 3-input OR gate is shown in Fig. 5.

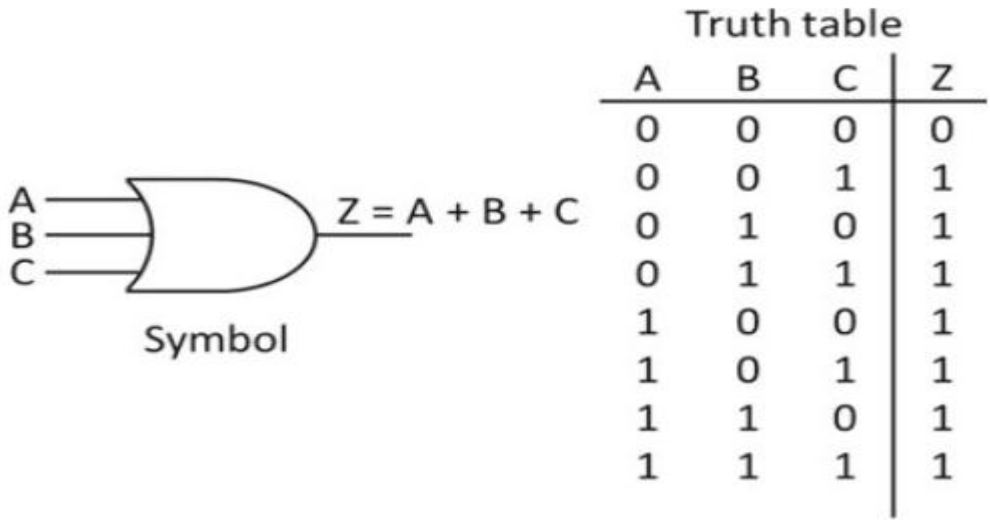


Fig. 5 OR gate with three inputs

1.2.2 Timing Diagram

Timing diagram shows the relationship between the inputs and output of OR gate graphically. The timing diagram for 2-input OR gate is shown in Fig. 6. The output is High when the input of A or B is High; otherwise it is Low.

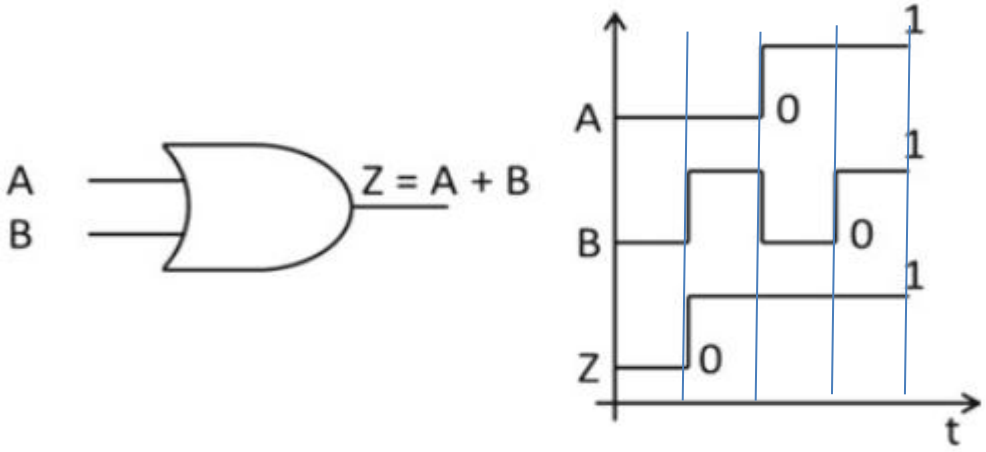


Fig. 6 Timing diagram for OR gate

1.3 AND Gate

AND gate has two or more input variables and the gate has one output. ICs for AND gate are available with many configurations. The standardized symbol for AND gate with two inputs (A & B), output (Z), truth table and timing diagram are shown in Fig. 7. A dot (**.**) is used to show the AND operation i.e. A.B. Bear in mind that ***this dot is sometimes omitted i.e. AB***. The output is High when both the inputs of A and B are High; otherwise it is Low. The inputs and output are related by,

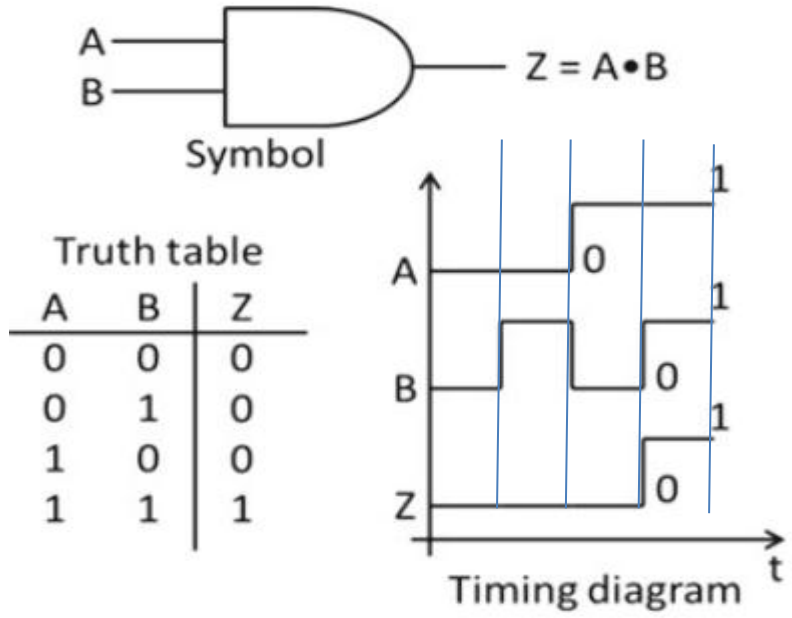


Fig. 7 AND gate with two inputs

$$Z = A \ AND \ B = A \cdot B$$

Truth table for AND gate with more than two input variables could also be prepared. The inputs and output of 3-input AND gate are related by,

$$Z = A \cdot B \cdot C$$

2. Universal Logic Gates

Universal logic gates are NOR and NAND gates. Basic logic gates OR, AND, and NOT gates could be realized from the universal gates. The operation of universal logic gates and the realization of the basic logic gates using the universal logic gates are presented.

2.1 NOR Gate

The standard NOR gate is OR gate followed by **inverter** i.e. ***OR gate with bubble at its output***. Two or more inputs are associated with NOR gate and the gate has one output. The standardized symbol for NOR gate with two inputs (A & B), the output (Z) and the truth table are shown in Fig. 8. The output of NOR gate is 1 when A= B = 0; otherwise, it is 0. ICs for standard NOR gate are available. The inputs and output of NOR gate are related by,

Truth table

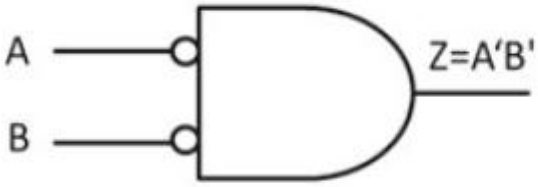
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 8 Standard NOR gate with two inputs

$$Z = (A + B)'$$

2.1.1 Bubbled AND Gate

NOR gate could also be realized by having inverters for the inputs of AND gate i.e. bubbled AND gate. The standardized symbol for bubbled AND gate with two inputs (A & B), the output (Z) and the truth table of the gate are shown in Fig. 9. The inputs and output of bubbled NOR gate are related by,



Truth table

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 9 Bubbled AND gate with two inputs

$$Z = A' \cdot B'$$

The outputs of standard NOR gate and bubbled AND gate are same for the same combination of inputs. It could be proved by applying ***De Morgan's theorem*** on the outputs.

$$Z = A' \cdot B' = (A + B)'$$

2.1.2 Basic Logic Gates from NOR Gate

The three basic logic gates, NOT, OR and AND, could be realized from NOR gate. The logic circuits for realizing the gates are shown in Fig.10. The derivations for the output expressions for the gates are also shown in the figures.

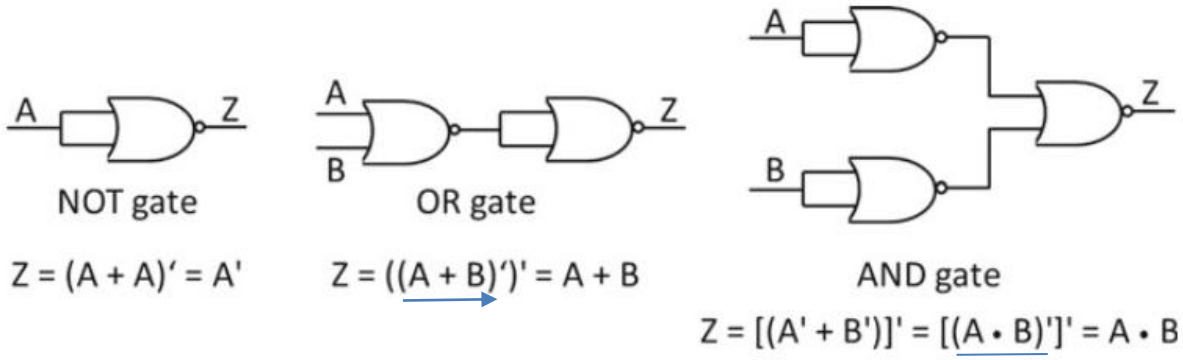


Fig. 10 Basic logic gates from NOR gate