Al-Mustaqbal University
College of Sciences
Intelligent Medical System Department

جامعة المستقبل
AL MUSTAQBAL UNIVERSITY

كلية العلوم
قسم الانظمة الطبية الذكية

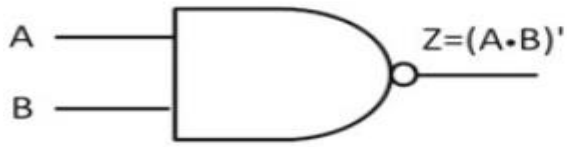
Lecture: (3)

Subject: Logic Gates (II)
Level: First
Lecturer: Dr. Ahmad T. Jaiad

1. Universal Logic Gates

1.1 NAND Gate

The standard NAND gate is AND gate followed by inverter i.e. AND gate with bubble at its output. Two or more inputs are associated with NAND gate and the gate has one output. The standardized symbol for NAND gate with two inputs (A & B), the output (Z) and the truth table are shown in Fig.1. ICs for standard NAND gate are available. The inputs and output of NAND gate are related by,



Truth table

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 1 Standard NAND gate with two inputs

$$Z = (A \cdot B)'$$

1.1.1 Bubbled OR Gate

NAND gate could also be realized by having inverters for the inputs of OR gate i.e. bubbled OR gate. The standardized symbol for bubbled OR gate with two inputs (A & B), the output (Z) and the truth table are shown in Fig.2. The inputs and output of bubbled OR gate are related by,

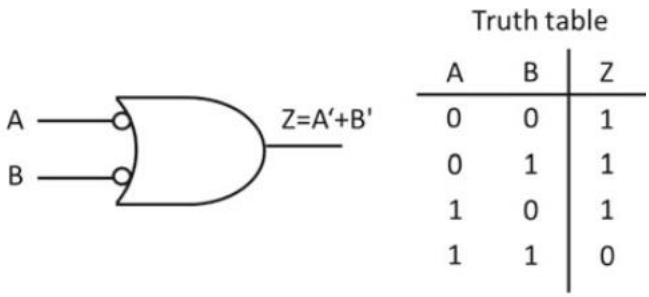


Fig. 2 Bubbled OR gate with two inputs

$$\boldsymbol{Z = A' + B'}$$

The outputs of standard NAND gate and bubbled OR gate are same for the same combination of input

s. It could be proved by applying De Morgan's theorem on the outputs.

$$\boldsymbol{Z = A' + B' = (A \cdot B)'}$$

1.1.2 Basic Logic Gates from NAND Gate

The three basic logic gates, NOT, OR and AND, could be realized from NAND gate. The logic circuits for realizing the gates are shown in Fig.3. The derivations for the output expressions for the gates are also shown in the figures.

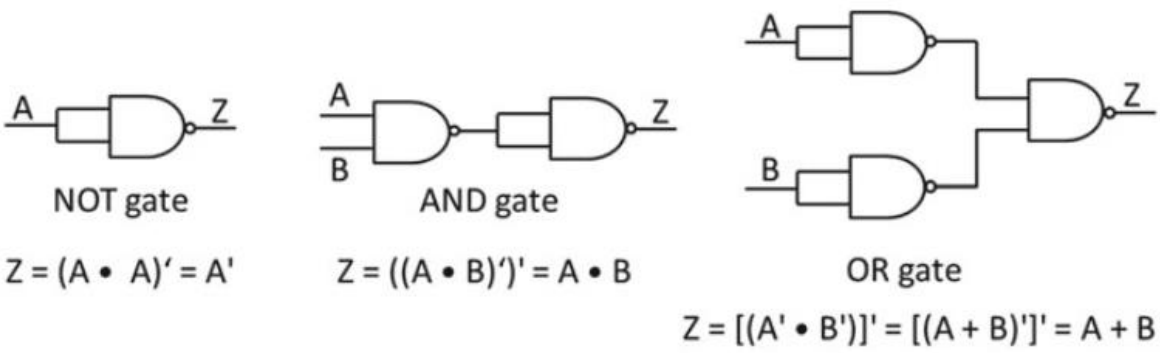
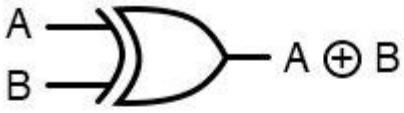


Fig.3 Basic logic gates from NAND gate

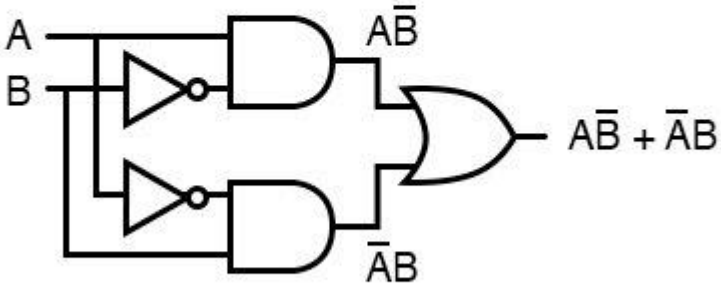
2. The Exclusive-OR Gate (XOR Gate)

The exclusive-OR gate performs modulo-2 addition. Standard symbols for an exclusive OR (X-OR) gate and Boolean expression for the output of a 2-input XOR gate can be written as:

$$Q = \bar{A}B + A\bar{B} = A \oplus B$$



. . . is equivalent to . .

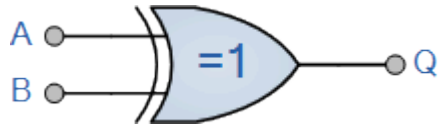


$A \oplus B = A\bar{B} + \bar{A}B$

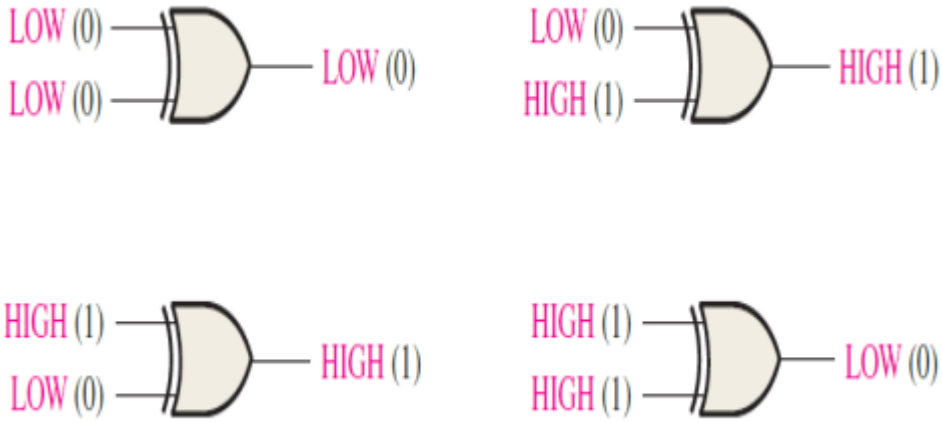
The X-OR gate has only two inputs. The four possible input combinations and the resulting outputs f

or an X-OR gate. The operation of an X-OR gate is summarized in the truth table shown

2-input XOR Gate

<table>
<tr><th>Symbol</th><th colspan="3">Truth Table</th></tr>
<tr><td></td><td colspan="3"></td></tr>
<tr><td rowspan="6"> 

2-input Ex-OR Gate</td><td>B</td><td>A</td><td>Q</td></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Boolean Expression Q = A ⊕ B</td><td colspan="3">A OR B but NOT BOTH gives Q</td></tr>
</table>



3. Exclusive NOR-Gate (XNOR-Gate)

XNOR (exclusive NOR) gate is XOR gate followed by inverter. The output of XNOR gate is the complement of the output of XOR gate. Standard ICs (Ex. 74LS266, Quad 2-input XNOR) are available for XNOR gates with two inputs. The output of 2-input

when both the inputs are either Low or High; otherwise, the output is Low.

XNOR gate could be implemented by using appropriate combination of inverter, AND, OR, NOR and NAND gates. 2-input XNOR gate could be

conveniently implemented using Quad 2-input NOR gate. The NOR gate implementation, the symbol and the truth table of XNOR gate are shown in Fig. 4. The operator,⊙ ,represents XNOR operation. The inputs and output of 2-input XNOR function are related by,

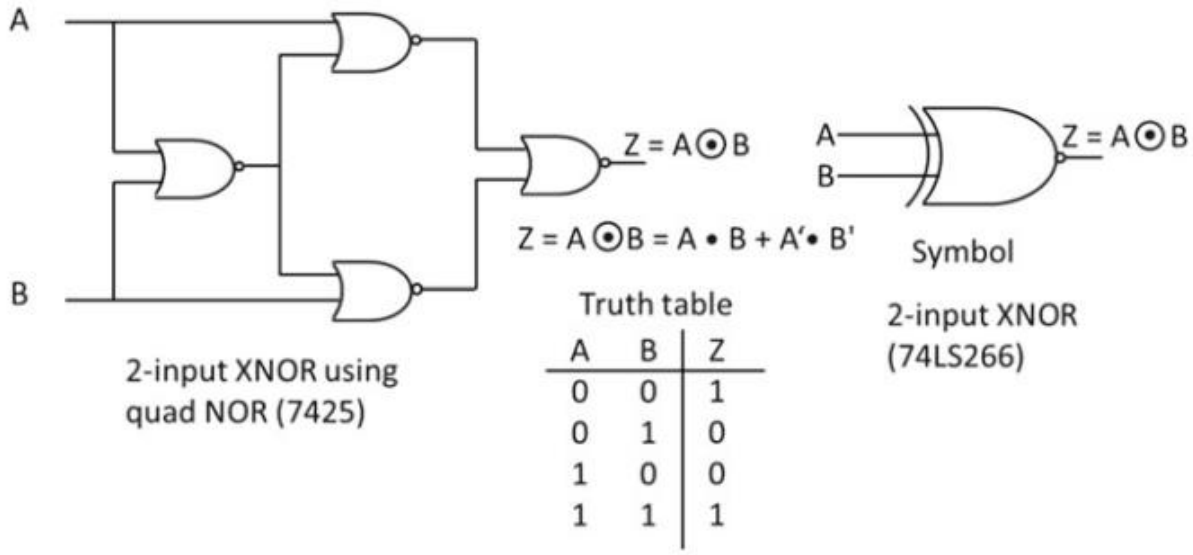


Fig. 4 Implementation of 2-input XNOR gate

$$Z = (A \odot B) = (A \oplus B)' = A \cdot B + A' \cdot B'$$

3.1 XNOR with Higher Order Inputs

XNOR function for 3 or more inputs (variables) is implemented by cascading 2-input XOR gates in a tree format except that the output XOR gate is replaced by XNOR gate. The implementation of 3-input and 4-input XNOR functions is shown in Fig. 5.

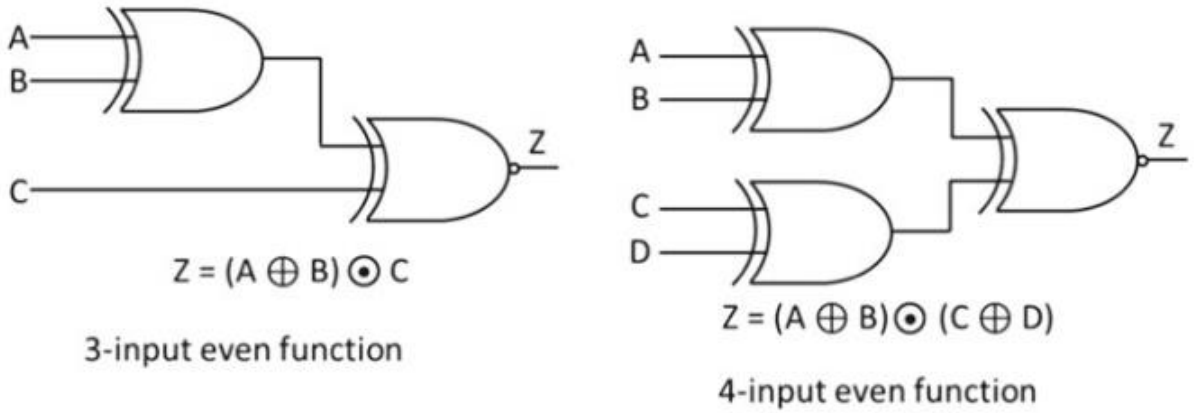
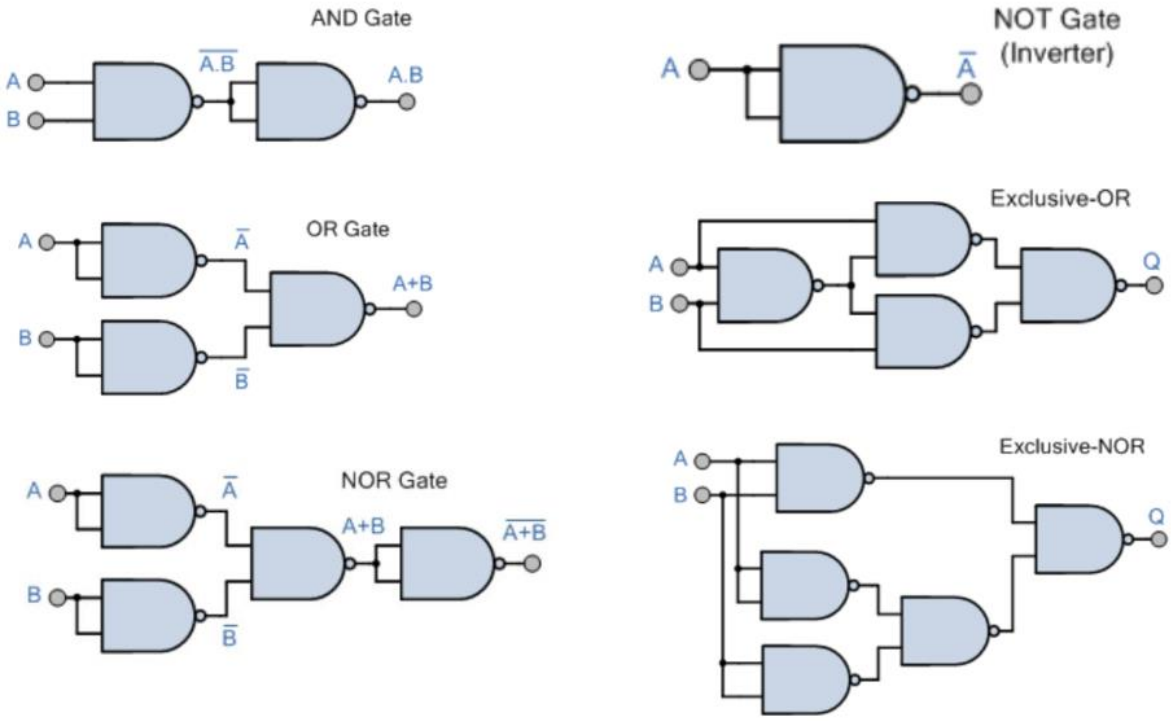


Fig. 5 Implementation of 3-input & 4-input even functions

3.2 Even Function

XNOR functions are even functions. The output of XNOR function is 1 when the number of input variables having logic 1 is even. The outputs of 2-input XNOR gate are 1 for the two inputs, 00 and 11. Similarly, the outputs of 3-input XNOR function are 1 for the inputs, 000, 011, 101 and 110.

4. Implementation of Gates Using NANAD Gate



Examples

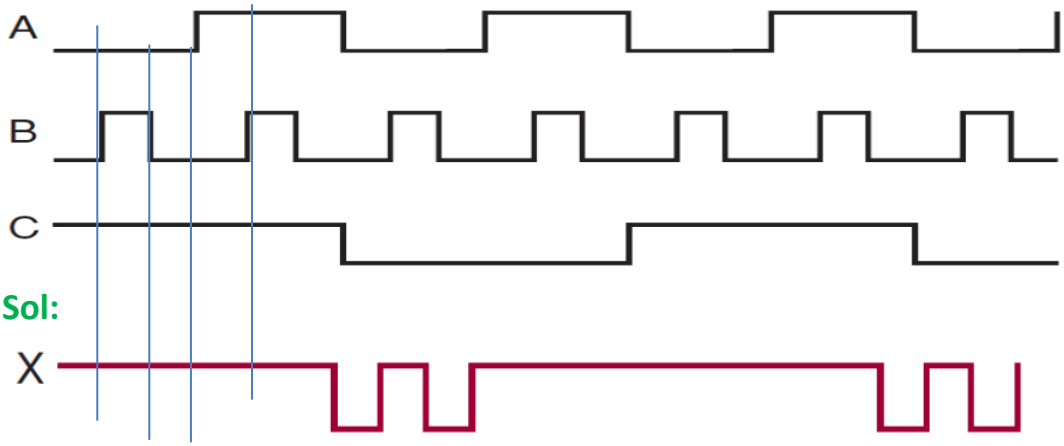
1. **Write the Boolean expression for a 3-input NAND gate.**

   Sol: The output Y of the NAND gate with inputs A, B, and C is $Y = \overline{A.B.C}$

2. **Which logic gate generates a HIGH output when an odd number of inputs are HIGH?**

   Sol. Exclusive-OR gate (EX-OR/XOR Gate)

3. **For the given input signals A, B, C, sketch the output for an OR gate.**

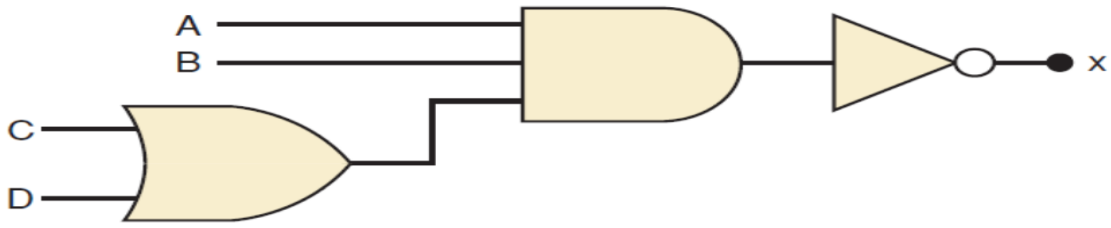


The output X = A + B + C is high when any of the inputs is high.

4. **For the given expression, draw the corresponding logic circuit, using AND, OR and NOT gates.**

$$x = \overline{A.B(C+D)}$$

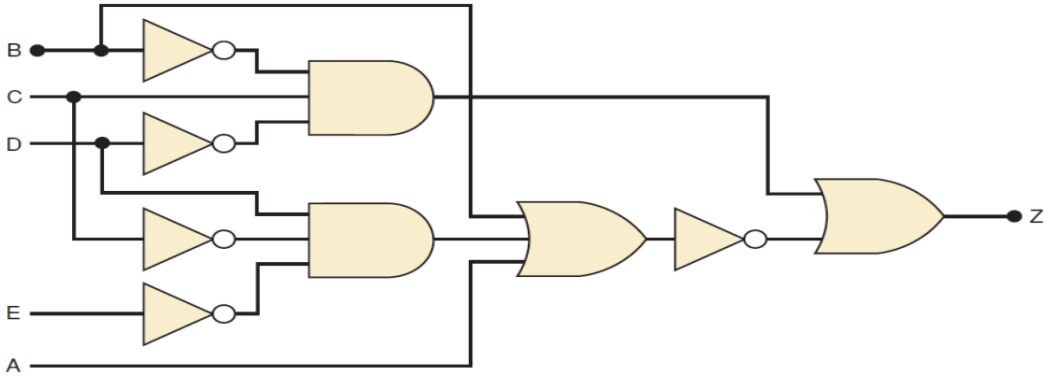
Sol:



5. **For the given expression, draw the corresponding logic circuit, using AND, OR and NOT gates**

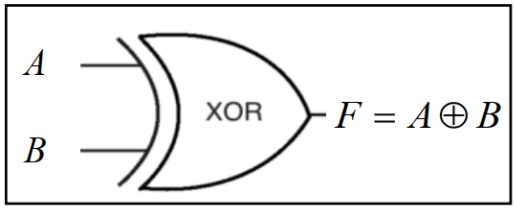
$$z = \overline{A + B + \overline{C}D\overline{E} + \overline{B}C\overline{D}}$$

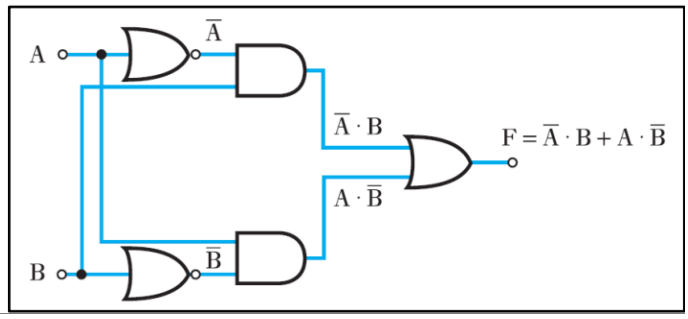
Sol:



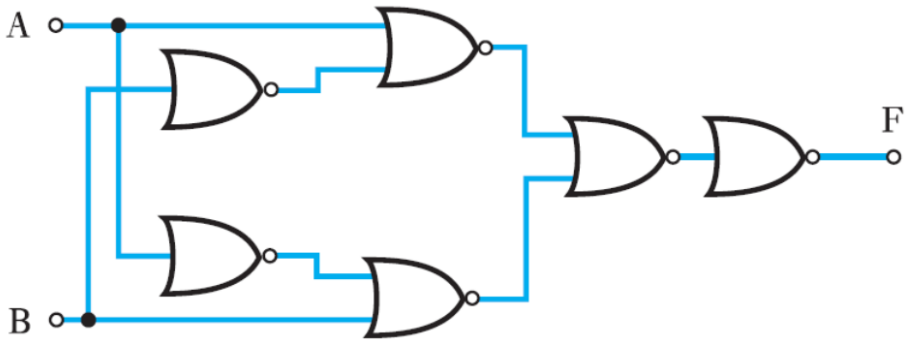
6. **Draw a logic circuit, incorporating any gates of your choice, which will produce an output 1 when its two inputs are different. Also draw the same logic circuit incorporating only NOR gates.**

Sol: The required function is $\mathbf{F = A \oplus B = (A \,.\, \overline{B}) + (\overline{A} \,.\, B)}$





Circuit for $\mathbf{F = A \oplus B = (A \cdot \overline{B}) + (\overline{A} \cdot B)}$ using only NOR gates (gates with single input imply that both inputs are same)



HW:

1- Draw the circuit diagram to implement the expression below

$$x = (A + B)(\overline{B} + C)$$

2- Draw the circuit diagram to implement the expression

$$x = AC + B\overline{C} + \overline{A}BC$$