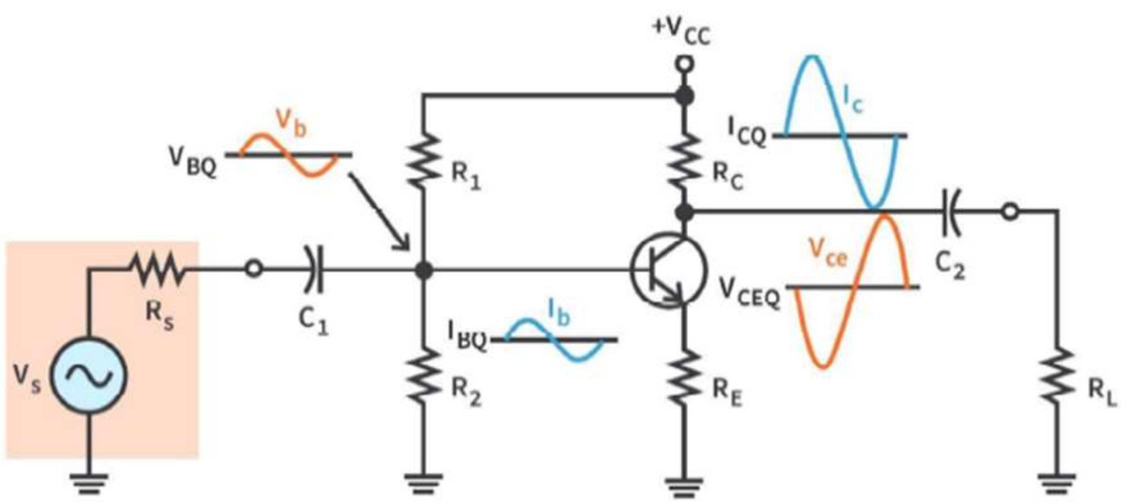
Electronic Circuit

Lecture 1 (1^{st} & 2^{nd} Week)

FET and JFET Small-Signal Amplifier



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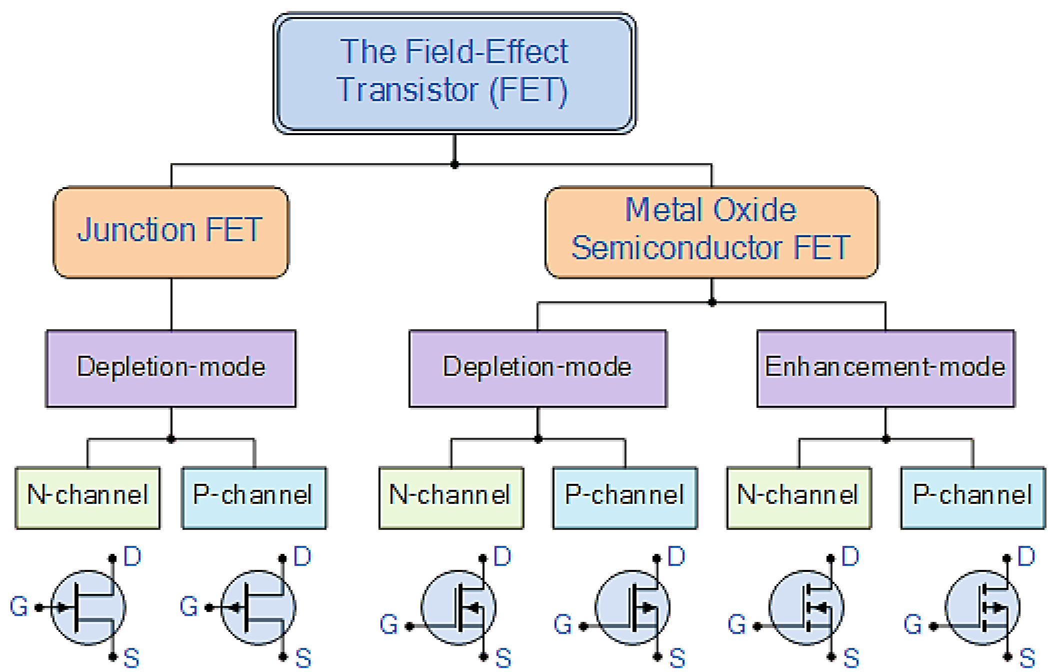
1.1. Introduction to FET Amplifiers

Field Effect Transistor (FET) amplifiers use the voltage applied to the gate terminal to control the current flowing through the device. Types of FETs used in amplifiers:

- JFET (Junction FET): High input impedance, simpler design.
- MOSFET (Metal-Oxide-Semiconductor FET): Higher switching speeds and better scalability.

FET amplifiers are commonly used in low-noise and RF circuits.



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The common FET amplifier configurations:

1. Fixed Bias Configuration: A fixed DC voltage gate is applied to the gate via a resistor gate.

2. Voltage Divider Bias Configuration: A voltage divider network (R1 and R2) sets the gate voltage.

3. Self-Bias Configuration: A resistor source is added to the source, creating a voltage drop that stabilizes the operating point automatically.

4. Common Source Configuration: The source serves as a common terminal for both the input and output signals.

5. Source Follower Configuration: Also called the "Common Drain Amplifier," where the source acts as the output.

6. Common Gate Configuration The gate is common to both input and output, and the signal is applied to the source.

Comparison of Configurations

Configuration	Stability	Complexity	Phase Inversion	Common Applications
Fixed Bias	Low	Simple	Yes	Educational purposes
Voltage Divider	High	Moderate	Yes	Practical and stable designs
Self-Bias	Moderate	Simple	Yes	Cost-effective amplifier designs
Common Source	High	Moderate	Yes	General-purpose voltage amplification
Source Follower	High	Simple	No	Buffer circuits
Common Gate	High	Moderate	No	High-frequency applications

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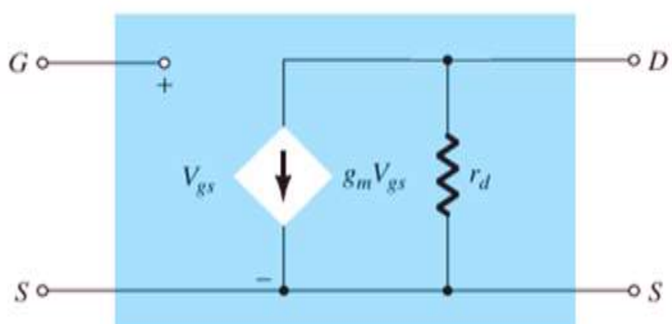
JFET Small Signal Model

The ac analysis of a JFET configuration requires that a small-signal ac model for the JFET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source. The gate-to-source voltage controls the drain-to-source (channel) current of a JFET. A dc gate-to-source voltage controls the level of dc drain current through a relationship known as Shockley's equation: ID = IDSS (1- VGS / VP)2. The change in drain current that will result from a change in gate-to-source voltage can be determined using the transconductance factor g m in the following manner:

$$\Delta I_D = g_m \, \Delta V_{GS}$$



The prefix trans - in the terminology applied to g_m reveals that it establishes a relationship between an output and an input quantity. The root word conductance was chosen because g_m is determined by a current-to-voltage ratio similar to the ratio that defines the conductance of a resistor, G = 1/R = I/V.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

The graphical procedure just described is limited by the accuracy of the transfer plot and the care with which the changes in each quantity can be determined.

Naturally, the larger the graph, the better is the accuracy, but this can then become a cumbersome problem. An alternative approach to determining g_m employs the approach used to find the ac resistance of a diode, where it was stated that: The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

To ensure a positive value for g_m . It was mentioned earlier that the slope of the transfer curve is a maximum at VGS=0V. Plugging in VGS=0 V into Eq. above results in the following equation for the maximum value of g m for a JFET in which I DSS and V P have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

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Where the added subscript 0 reminds us that it is the value of g_m when VGS=0V. Eq. above then becomes

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Example 1: For the JFET having the transfer characteristics with IDSS = 8 mA and VP =-4 V at the following dc bias points:

a. Find the maximum value of g_m.

b. Find the value of g m at each operating point of VGS =-0.5 V, -1.5V, -2.5V.

Solution:

a. $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\text{ mS}}$ (maximum possible value of g_m)

b. At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\text{ mS}}$$

At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\text{ mS}}$$

At $V_{GS} = -2.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\text{ mS}}$$

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JFET AC Equivalent Circuit Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the JFET transistor in the ac domain can be constructed. The control of I_D by Vgs is included as a current source gmVgs connected from drain to source as shown in Fig.2. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

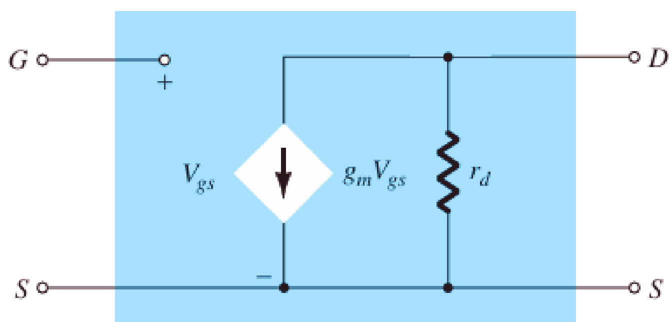

Fig.2. JFET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor rd from drain to source. Note that the gate-to-source voltage is now represented by Vgs (lowercase subscripts) to distinguish it from dc levels. In addition, note that the source is common to both input and output circuits, whereas the gate and drain terminals are only in "touch" through the controlled current source gmVgs.

In situations where rd is ignored (assumed sufficiently large in relation to other elements of the network to be approximated by an open circuit), the equivalent

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circuit is simply a current source whose magnitude is controlled by the signal Vgs and parameter gm clearly a voltage-controlled current source.

1.2. Fixed Bias Configuration

Now that the JFET equivalent circuit has been defined, a number of fundamental JFET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of Zi, Zo, and Av for each configuration. The fixed-bias configuration of Fig.3. includes the coupling capacitors C1 and C2, which isolate the dc biasing arrangement from the applied signal and load; they act as short circuit equivalents for the ac analysis.

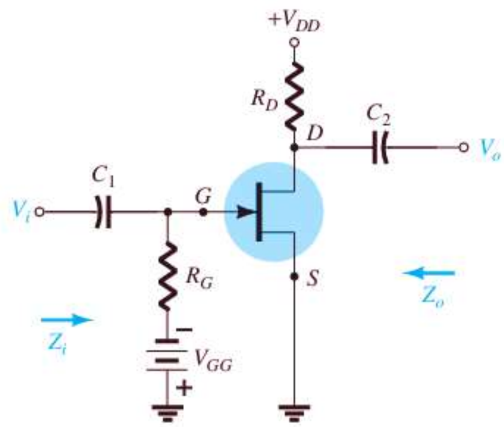

Fig.3. JFET fixed-bias configuration.

Once the levels of g m and r d are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the ap propriate terminals as shown in Fig.4. Note that both capacitors have the short-circuit equivalent because the reactance $XC = 1/(2\pi fC)$ is

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sufficiently small compared to other impedance levels of the network, and the dc batteries V GG and V DD are set to 0 V by a short-circuit equivalent. The network of Fig.4 is then carefully redrawn as shown in Fig.5. Note the de fined polarity of Vgs, which defines the direction of gmVgs. If Vgs is negative, the direction of the current source reverses. The applied signal is represented by Vi and the output signal across $RD \| rd$ by Vo.

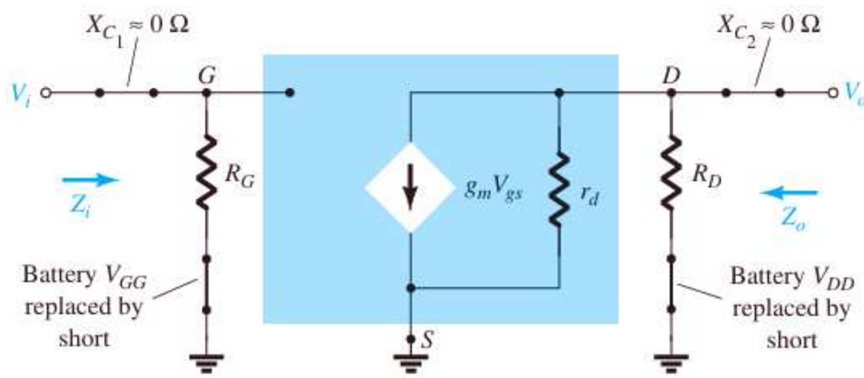

Fig.4. Substituting the JFET ac equivalent circuit unit into the network

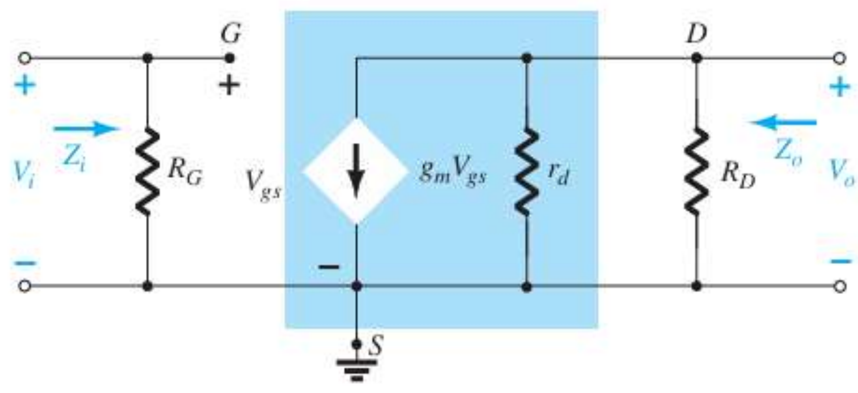

Fig.5. Redrawn network of Fig.4.

$$\boxed{Z_i = R_G}$$

because of the infinite input impedance at the input terminals of the JFET.

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Zo Setting Vi =0 V as required by the definition of Z o will establish Vgs as 0 V also. The result is gmVgs=0 mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig.6. The output impedance is

$$Z_o = R_D \| r_d$$

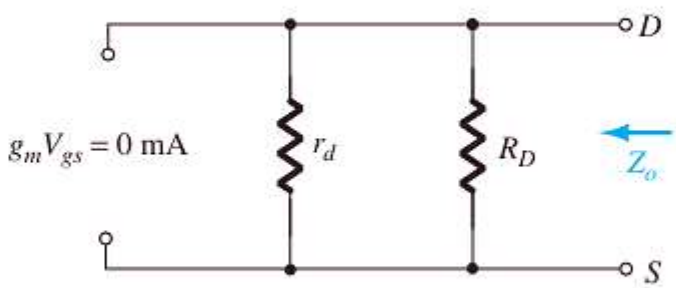

Fig.6. Determining Zo.

If the resistance r d is sufficiently large (at least 10:1) compared to RD, the approximation $rd\|RD = RD$ can often be applied and:

$$Z_o \cong R_D \qquad r_d \geq 10R_D$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m R_D \qquad r_d \geq 10R_D$$

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Example 2: The fixed-bias configuration of had an operating point defined by VGSQ =-2 V and IDQ =5.625 mA, with IDSS=10 mA and VP=-8 V. The network is redrawn as Fig.7. with an applied signal Vi. The value of yos is provided as 40μS.

a. Determine gm. b. Find rd. c. Determine Zi.
d. Calculate Zo. e. Determine the voltage gain Av.
f. Determine A v ignoring the effects of rd

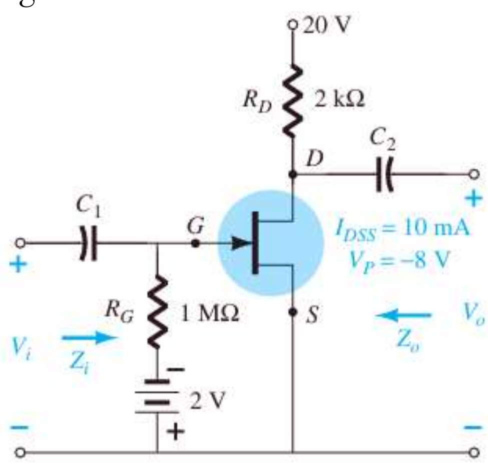

Fig.7. JFET configuration

Solution:

a. $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

b. $r_d = \frac{1}{y_{os}} = \frac{1}{40\ \mu\text{S}} = \mathbf{25\text{ k}\Omega}$

c. $Z_i = R_G = \mathbf{1\text{ M}\Omega}$

d. $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\text{ k}\Omega}$

e. $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$
$= \mathbf{-3.48}$

f. $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

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1.3. Common Gate Configurations

The last JFET configuration to be analyzed in detail is the common-gate configuration of Fig.8., which parallels the common-base configuration employed with BJT transistors. Substituting the JFET equivalent circuit results in Fig.9. Note the continuing requirement that the controlled source gmVgs be connected from drain to source with r d in parallel. The isolation between input and output circuits has obviously been lost since the gate terminal is now connected to the common ground of the network and the controlled current source is connected directly from drain to source.

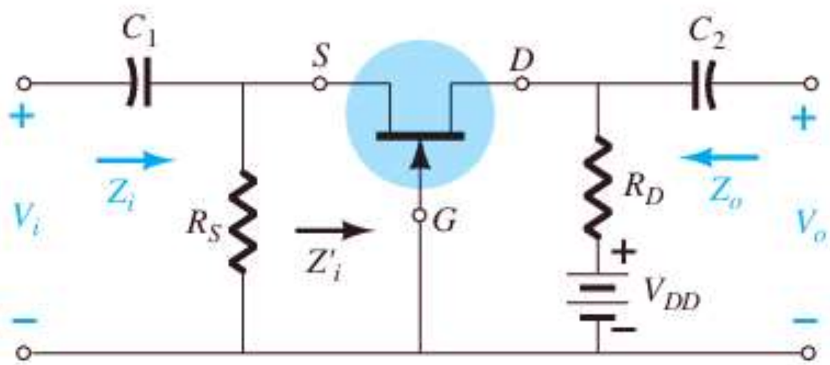

Fig.7. JFET common-gate configuration.

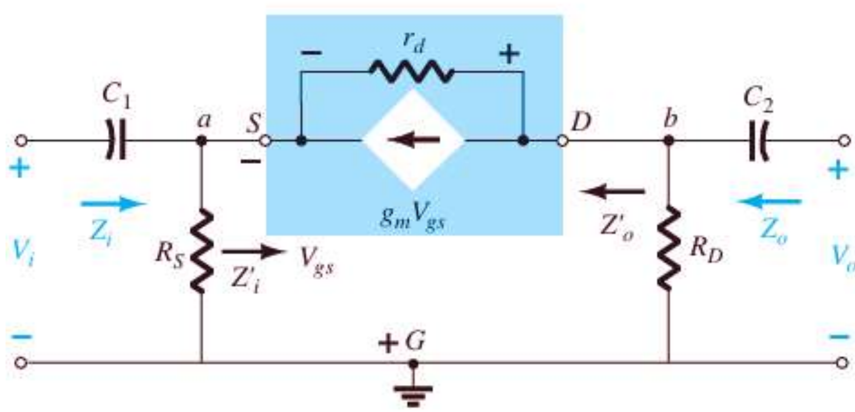

Fig.8.Network of Fig.7 following substitution of JFET ac equivalent model.

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Zi The resistor R S is directly across the terminals defining Zi Let us therefore find the impedance Zi of Fig.7, which will simply be in parallel with RS when Zi is defined.

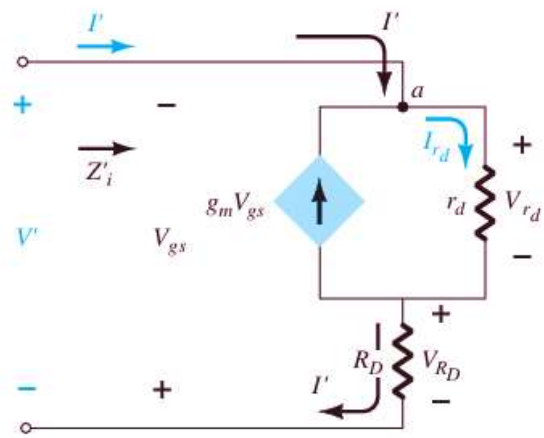

Fig. 9 Determining Zi for the network

$$Z_i' = \frac{V'}{I'} = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]}$$

$$Z_i = R_S \| Z_i'$$

$$Z_i = R_S \left\| \left[\frac{r_d + R_D}{1 + g_m r_d}\right]\right.$$

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If $r_d \geq 10R_D$, Eq. (8.33) permits the following approximation since $R_D/r_d \ll 1$ and $1/r_d \ll g_m$:

$$Z_i' = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]} \cong \frac{1}{g_m}$$

and

$$\boxed{Z_i \cong R_S \| 1/g_m} \quad {}_{r_d \geq 10R_D}$$

$\boldsymbol{Z_o}$ Substituting $V_i = 0$ V in Fig. 8.25 will "short-out" the effects of R_S and set V_{gs} to 0 V. The result is $g_m V_{gs} = 0$, and r_d will be in parallel with R_D. Therefore,

$$\boxed{Z_o = R_D \| r_d}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D} \quad {}_{r_d \geq 10R_D}$$

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]}}$$

For rd ≥ 10RD, the factor RD / rd of Eq. above can be dropped as a good approximation, and:

$$\boxed{A_v \cong g_m R_D} \quad {}_{r_d \geq 10R_D}$$

Example 3: Although the network of Fig.10 may not initially appear to be of the common-gate variety, a close examination will reveal that it has all the characteristics. If VGSQ =-2.2 V and IDQ = 2.03 mA:

a. Determine gm .

b. Find rd .

c. Calculate Zi with and without rd Compare results.

d. Find Z o with and without rd Compare results.

e. Determine V o with and without rd Compare results.

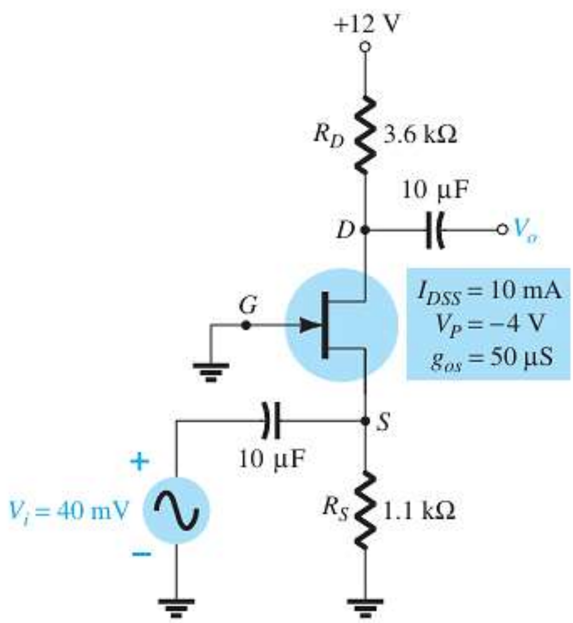

Fig.10. Network for Example

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 5\text{ mS}\left(1 - \frac{(-2.2\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.25\text{ mS}}$$

b. $r_d = \dfrac{1}{g_{os}} = \dfrac{1}{50\,\mu S} = \mathbf{20\text{ k}\Omega}$

c. With r_d,

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right] = 1.1\text{ k}\Omega \| \left[\frac{20\text{ k}\Omega + 3.6\text{ k}\Omega}{1 + (2.25\text{ mS})(20\text{ k}\Omega)}\right]$$
$$= 1.1\text{ k}\Omega \| 0.51\text{ k}\Omega = \mathbf{0.35\text{ k}\Omega}$$

Without r_d,

$$Z_i = R_S \| 1/g_m = 1.1\text{ k}\Omega \| 1/2.25\text{ ms} = 1.1\text{ k}\Omega \| 0.44\text{ k}\Omega$$
$$= \mathbf{0.31\text{ k}\Omega}$$

Even though the condition $r_d \geq 10R_D$ is not satisfied with $r_d = 20\text{ k}\Omega$ and $10R_D = 36\text{ k}\Omega$, both equations result in essentially the same level of impedance. In this case, $1/g_m$ was the predominant factor.

d. With r_d,

$$Z_o = R_D \| r_d = 3.6\text{ k}\Omega \| 20\text{ k}\Omega = \mathbf{3.05\text{ k}\Omega}$$

Without r_d,

$$Z_o = R_D = \mathbf{3.6\text{ k}\Omega}$$

Again the condition $r_d \geq 10R_D$ is *not* satisfied, but both results are reasonably close. R_D is certainly the predominant factor in this example.

e. With r_d,

$$A_v = \frac{\left[g_m R_D + \dfrac{R_D}{r_d}\right]}{\left[1 + \dfrac{R_D}{r_d}\right]} = \frac{\left[(2.25\text{ mS})(3.6\text{ k}\Omega) + \dfrac{3.6\text{ k}\Omega}{20\text{ k}\Omega}\right]}{\left[1 + \dfrac{3.6\text{ k}\Omega}{20\text{ k}\Omega}\right]}$$
$$= \frac{8.1 + 0.18}{1 + 0.18} = \mathbf{7.02}$$

and $\qquad A_v = \dfrac{V_o}{V_i} \Rightarrow V_o = A_v V_i = (7.02)(40\text{ mV}) = \mathbf{280.8\text{ mV}}$

Without r_d,

$$A_v = g_m R_D = (2.25\text{ mS})(3.6\text{ k}\Omega) = \mathbf{8.1}$$

with $\qquad V_o = A_v V_i = (8.1)(40\text{ mV}) = \mathbf{324\text{ mV}}$

In this case, the difference is a little more noticeable, but not dramatically so.

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1.4. Source Follower (Common Drain) Configuration

The JFET equivalent of the BJT emitter-follower configuration is the source-follower con figuration of Fig. 11. Note that the output is taken off the source terminal and, when the dc supply is replaced by it short-circuit equivalent, the drain is grounded (hence, the terminology common-drain). Substituting the JFET equivalent circuit results in the configuration of Fig. 12. The controlled source and the internal output impedance of the JFET are tied to ground at one end and RS on the other, with Vo across RS. Since gmVgs, rd, and R S are connected to.

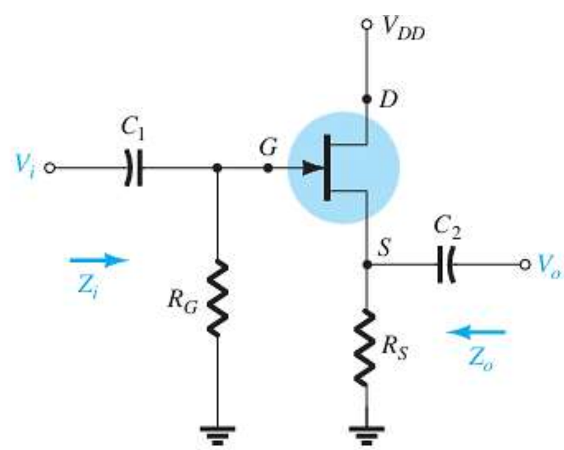

Fig.11. Zo JFET source-follower configuration.

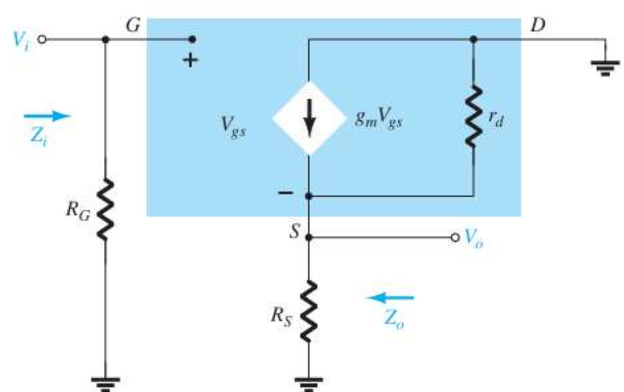

Fig.12. Network of Fig. 11 following the substitution of the JFET ac equivalent model.

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the same terminal and ground, they can all be placed in parallel as shown in Fig.13. The current source reversed direction, but Vgs is still defined between the gate and source terminals.

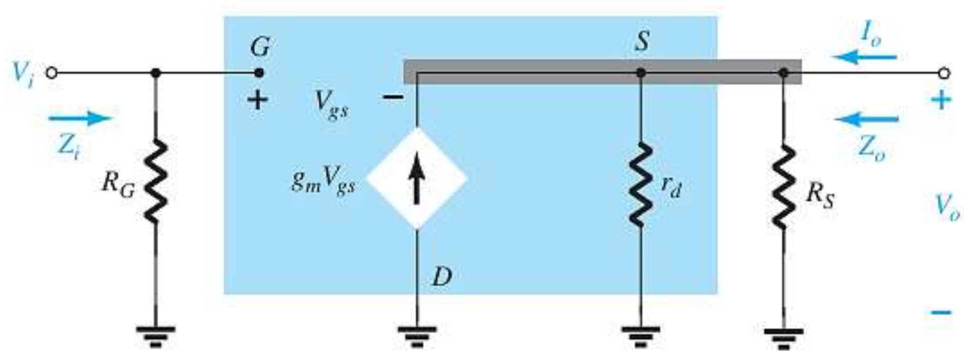

Fig.13. Network of Fig.12 redrawn.

Zi Figure.13. clearly reveals that Zi is defined by:

$$\boxed{Z_i = R_G}$$

Setting Vi = 0 V results in the gate terminal being connected directly to the ground as shown in Fig.14. The fact that Vgs and V o are across the same parallel network results in Vo =-Vgs.

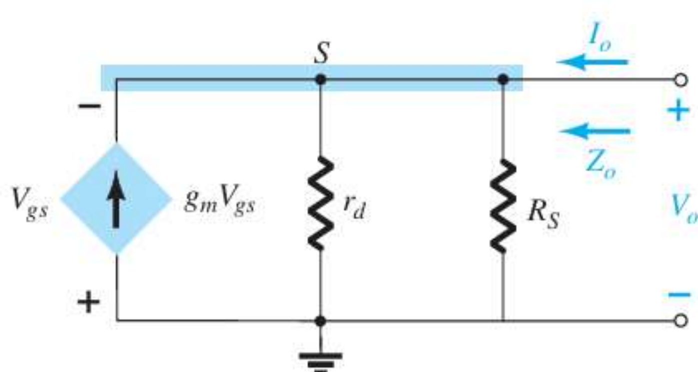

Fig.14. Determining Zo for the network of Fig.13.

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which has the same format as the total resistance of three parallel resistors. Therefore,

$$Z_o = r_d \| R_S \| 1/g_m$$

For $r_d \geq 10\,R_S$,

$$Z_o \cong R_S \| 1/g_m \qquad r_d \geq 10R_S$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$$

In the absence of r_d or if $r_d \geq 10\,R_S$,

$$A_v = \frac{V_o}{V_i} \cong \frac{g_m R_S}{1 + g_m R_S} \qquad r_d \geq 10R_S$$

Example 4: A dc analysis of the source-follower network of Fig.15 results in VGSQ =-2.86 V and IDQ =4.56 mA.

a. Determine gm.

b. Find rd.

c. Determine Zi.

d. Calculate Zo with and without rd Compare results.

e. Determine A v with and without rd Compare results.

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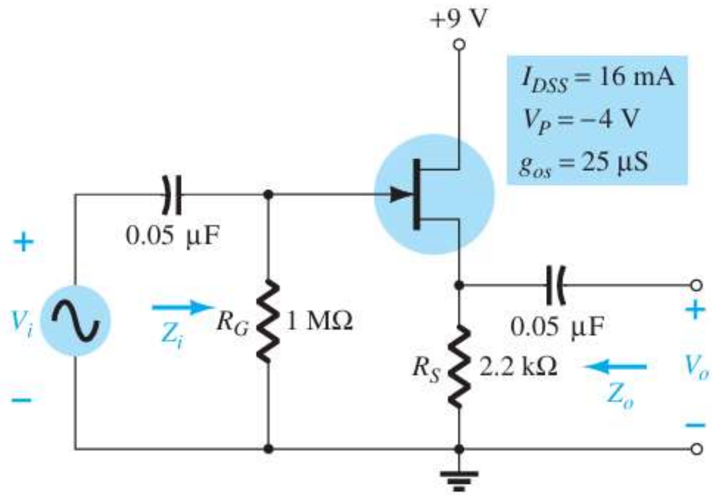

Fig.15. Network to be analyzed.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(16\text{ mA})}{4\text{ V}} = 8\text{ mS}$

$g_m = g_{m0}\left(1 - \dfrac{V_{GS_Q}}{V_P}\right) = 8\text{ mS}\left(1 - \dfrac{(-2.86\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.28\text{ mS}}$

b. $r_d = \dfrac{1}{g_{os}} = \dfrac{1}{25\ \mu S} = \mathbf{40\text{ k}\Omega}$

c. $Z_i = R_G = \mathbf{1\text{ M}\Omega}$

d. With r_d,

$$Z_o = r_d \| R_S \| 1/g_m = 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 1/2.28\text{ mS}$$
$$= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 438.6\ \Omega$$
$$= \mathbf{362.52\ \Omega}$$

which shows that Z_o is often relatively small and determined primarily by $1/g_m$.
Without r_d,

$$Z_o = R_S \| 1/g_m = 2.2\text{ k}\Omega \| 438.6\ \Omega = \mathbf{365.69\ \Omega}$$

which shows that r_d typically has little effect on Z_o.

e. With r_d,

$$A_v = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} = \frac{(2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}$$
$$= \frac{(2.28\text{ mS})(2.09\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.09\text{ k}\Omega)} = \frac{4.77}{1 + 4.77} = \mathbf{0.83}$$

which is less than 1, as predicted above.

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Without r_d,

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28 \text{ mS})(2.2 \text{ k}\Omega)}{1 + (2.28 \text{ mS})(2.2 \text{ k}\Omega)}$$

$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

which shows that r_d usually has little effect on the gain of the configuration.

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