COLLEGE OF ENGINEERING AND TECHNOLOGIES
ALMUSTAQBAL UNIVERSITY

Electronics Circuits

CTE 204

Lecture 2

- FET Biasing -

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Dr. Zaidoon AL-Shammari

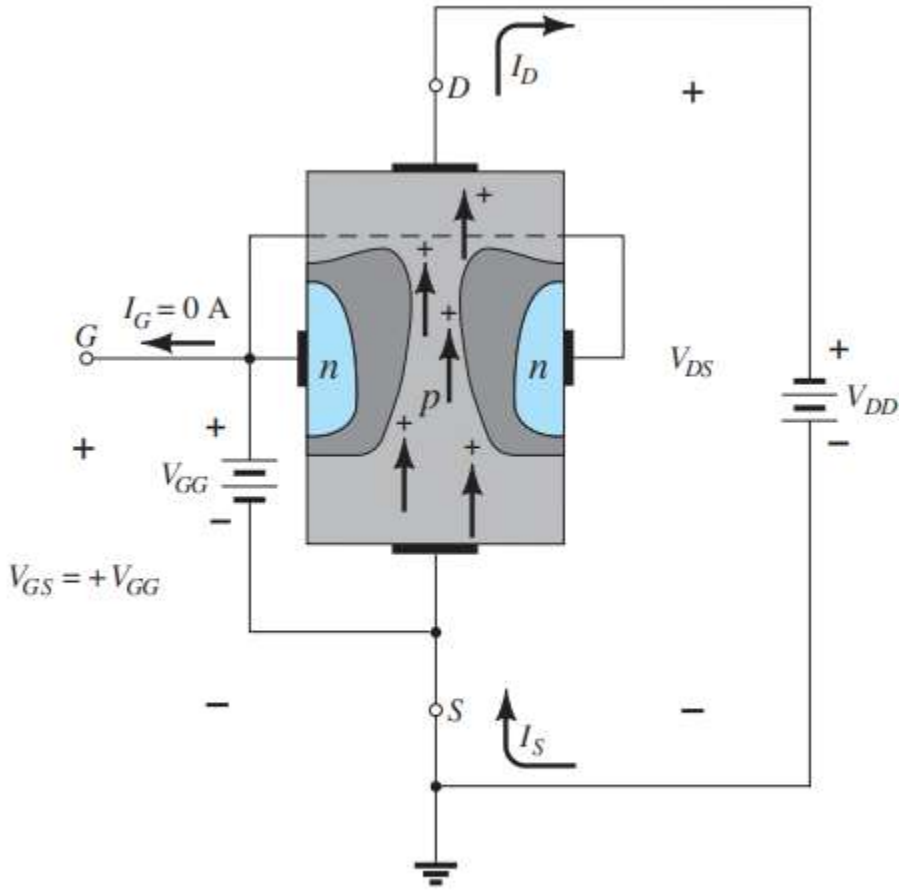
Lecturer / Researcher

zaidoon.waleed@mustaqbal-college.edu.iq

P - Channel Devices

- The p-channel JFET is constructed in exactly the same manner as the n-channel device, but with a reversal of the p and n type materials as shown in Figure below.

P - Channel Devices



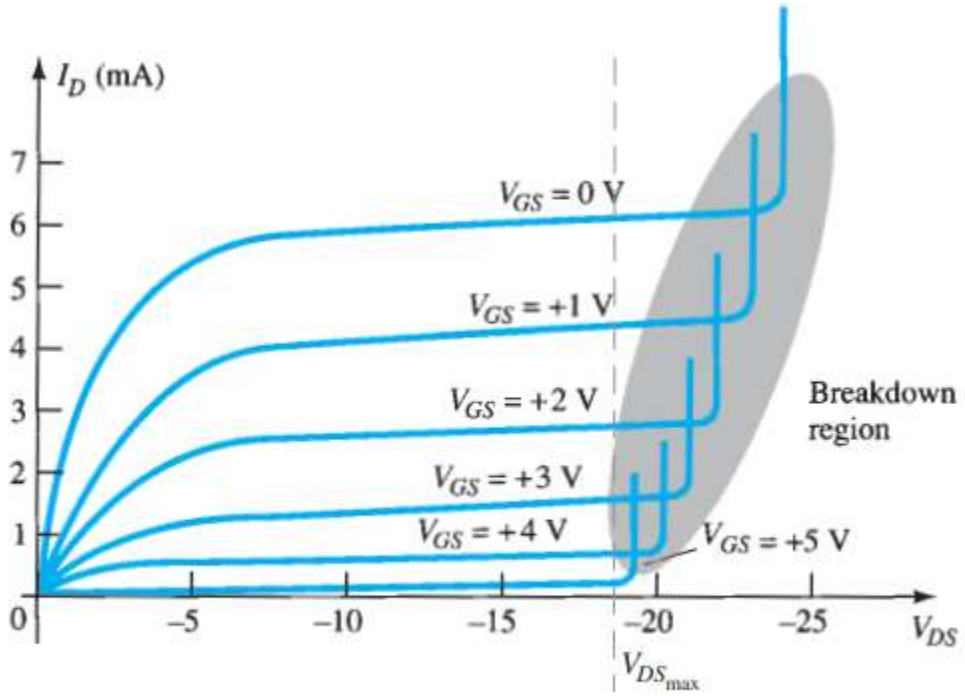
p-Channel JFET.

P - Channel Devices

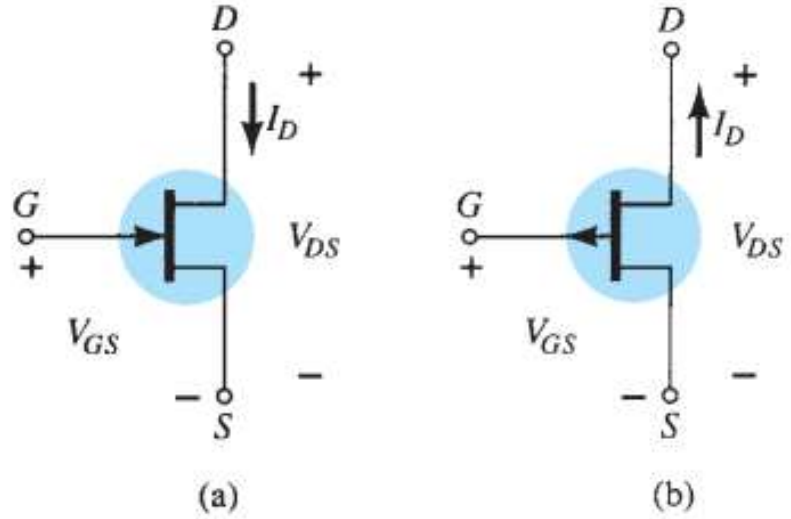
- The defined current directions are reversed, as are the actual polarities for the voltages VGS and VDS.

- For the p-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for VDS will result in negative voltages for VDS on the characteristics of Figure below.

P - Channel Devices



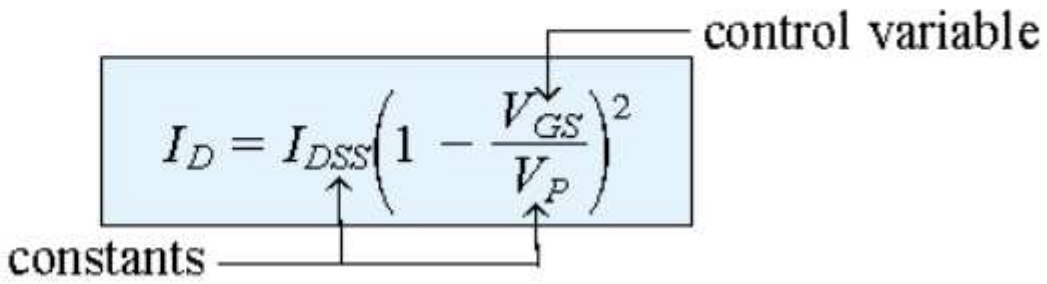
p-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.



JFET symbols: (a) n-channel; (b) p-channel.

Transfer Characteristics

The relationship between I_D and V_{GS} is defined by *Shockley'equation:*



- The squared term of the equation will result in a nonlinear relationship between ID and VGS, producing a curve that grows exponentially with decreasing magnitudes of VGS.

Transfer Characteristics

- The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

- By using basic algebra we can obtain an equation for the resulting level of VGS for a given level of ID.

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

- In the Figure below two graphs are provided, with the vertical scaling in milliamperes for each graph.

- One is a plot of ID versus VDS, while the other is ID versus VGS.

IMPORTANT RELATIONSHIPS:

JFET		*BJT*
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0\ \text{A}$	$\Leftrightarrow$	$V_{BE} \cong 0.7\ \text{V}$

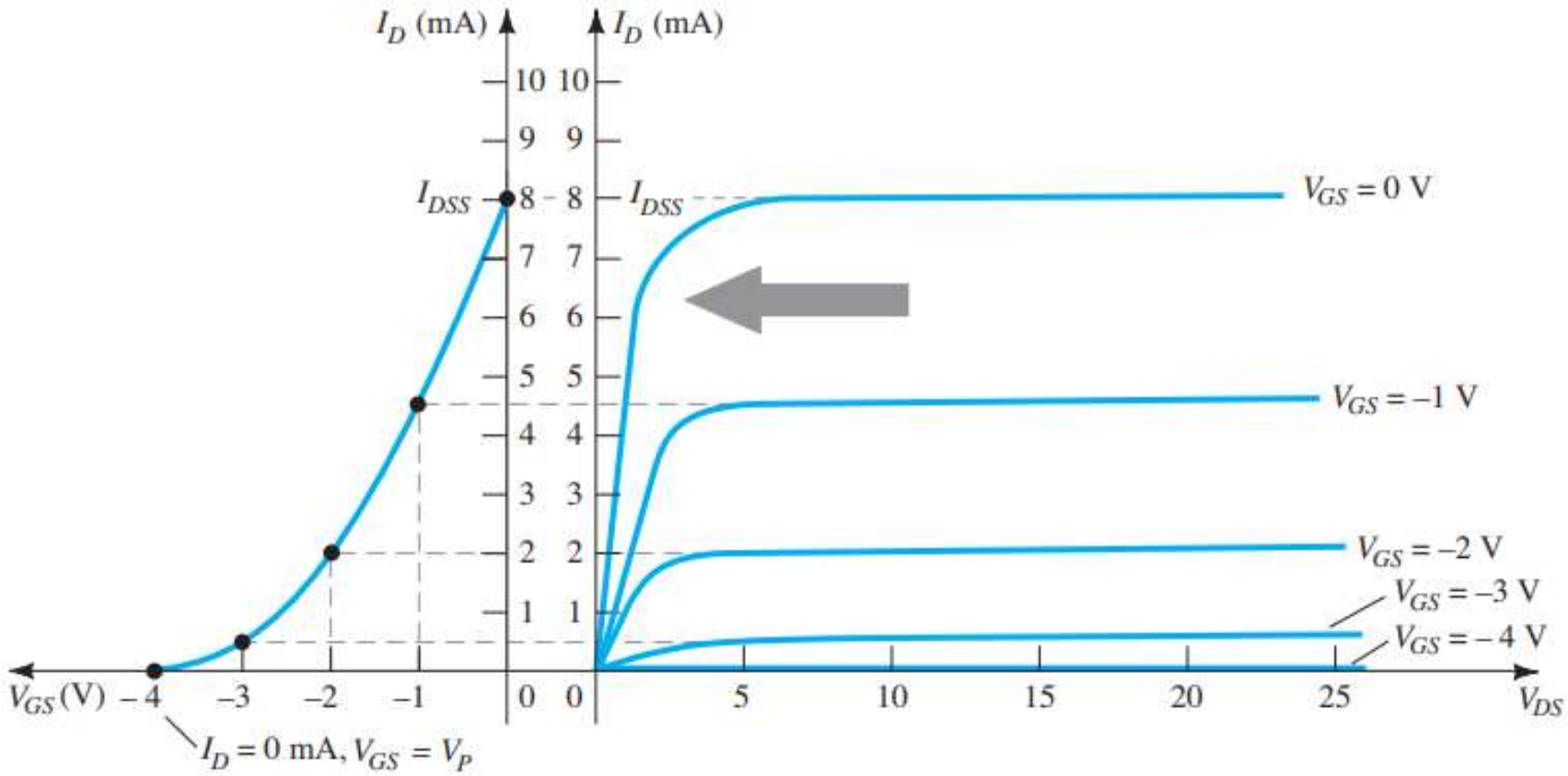
In review:

$$When\ V_{GS} = 0\ V,\ I_D = I_{DSS}\ ,\ and\ \ when\ V_{GS} = V_P,\ I_D = 0\ mA.$$

The total device dissipation at 25°C (room temperature) is the maximum power the device can dissipate under normal operating conditions and is defined by

$$P_D = V_{DS}\, I_D$$

Transfer Characteristics



Obtaining the transfer curve from the drain characteristics.

FET Biasing

- The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \approx 0 \text{ A} \qquad \text{and} \qquad I_D = I_S$$

- The simplest of biasing arrangements for the n-channel JFET appears in the Figure below.

- Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or graphical approach.

Fixed - Bias Configuration

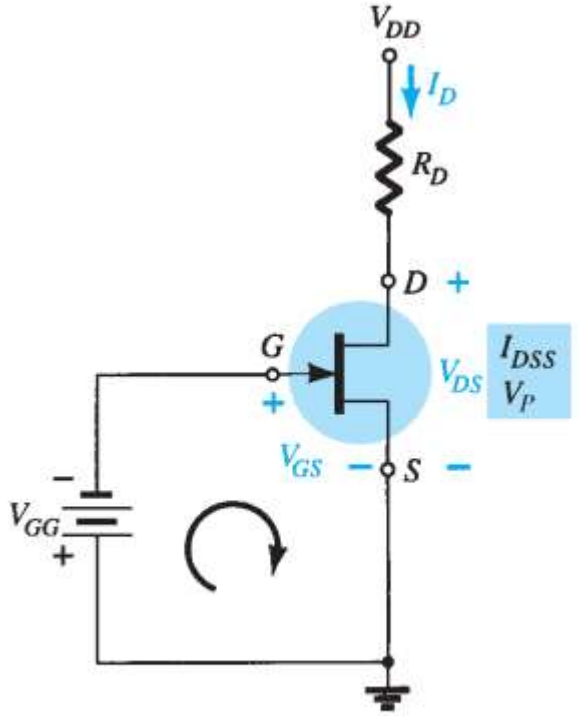
$I_G = 0\ \text{A}$ and $V_{RG} = I_G R_G = (0\ \text{A})R_G = 0\ \text{V}$

Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. will result in

$$-V_{GG} - V_{GS} = 0 \quad \text{and} \quad V_{GS} = -V_{GG}$$

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0 \quad \text{and} \quad V_{DS} = V_{DD} - I_D R_D$$



Network for dc analysis.

Fixed - Bias Configuration

For the configuration of Fig

$$V_S = 0$$

Using double-subscript notation:

$$V_{DS} = V_D - V_S \quad or \quad V_D = V_{DS} + V_S = V_{DS} + 0V \quad and \quad V_D = V_{DS}$$

In addition, $V_{GS} = V_G - V_S \quad or \; V_G = V_{GS} + V_S = V_{GS} + 0V \; and \; V_G = V_{GS}$

Fixed - Bias Configuration

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig.

$$\boxed{V_S = 0\,\text{V}}$$

Using double-subscript notation, we have

$$V_{DS} = V_D - V_S$$

or

$$V_D = V_{DS} + V_S = V_{DS} + 0\,\text{V}$$

and

$$\boxed{V_D = V_{DS}}$$

In addition,

$$V_{GS} = V_G - V_S$$

or

$$V_G = V_{GS} + V_S = V_{GS} + 0\,\text{V}$$

and

$$\boxed{V_G = V_{GS}}$$