COLLEGE OF ENGINEERING AND TECHNOLOGIES
ALMUSTAQBAL UNIVERSITY

Electronics Circuits

CTE 204

Lecture 1

- Field Effect Transistor (FET) -

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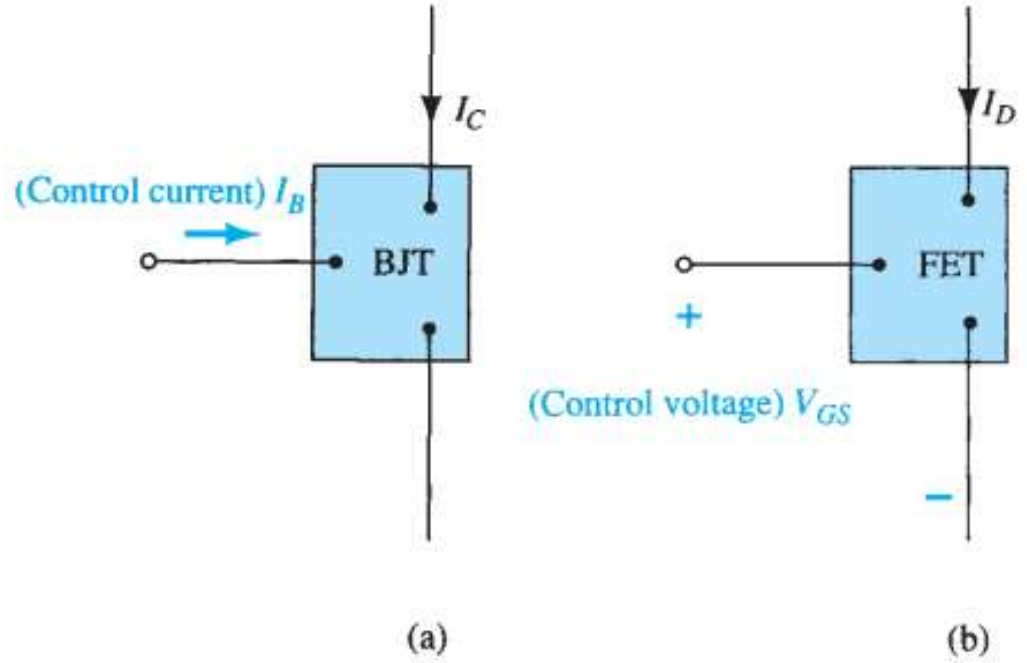
Introduction

- The field effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor.

- Although there are important differences between the two types of devices, there are also many similarities that will be pointed out in the sections to follow.

- The primary difference between the two types of transistors is the fact that the BJT transistor is a current-controlled device as depicted in Figure (a), while the JFET transistor is a voltage-controlled device as shown in Figure (b).



Introduction

- In other words, the current IC in Figure (a) is a direct function of the level of IB.
- For the FET the current I will be a function of the voltage VGS applied to the input circuit as shown in Figure (b).
- In each case the current of the output circuit is being controlled by a parameter of the input circuit in one case a current level and in the other an applied voltage.

Introduction

- There are n-channel and p-channel field-effect transistors
- Two types of FETs will be introduced:
  - The junction field-effect transistor (JFET) and
  - The metal-oxide-semiconductor field-effect transistor (MOSFET).

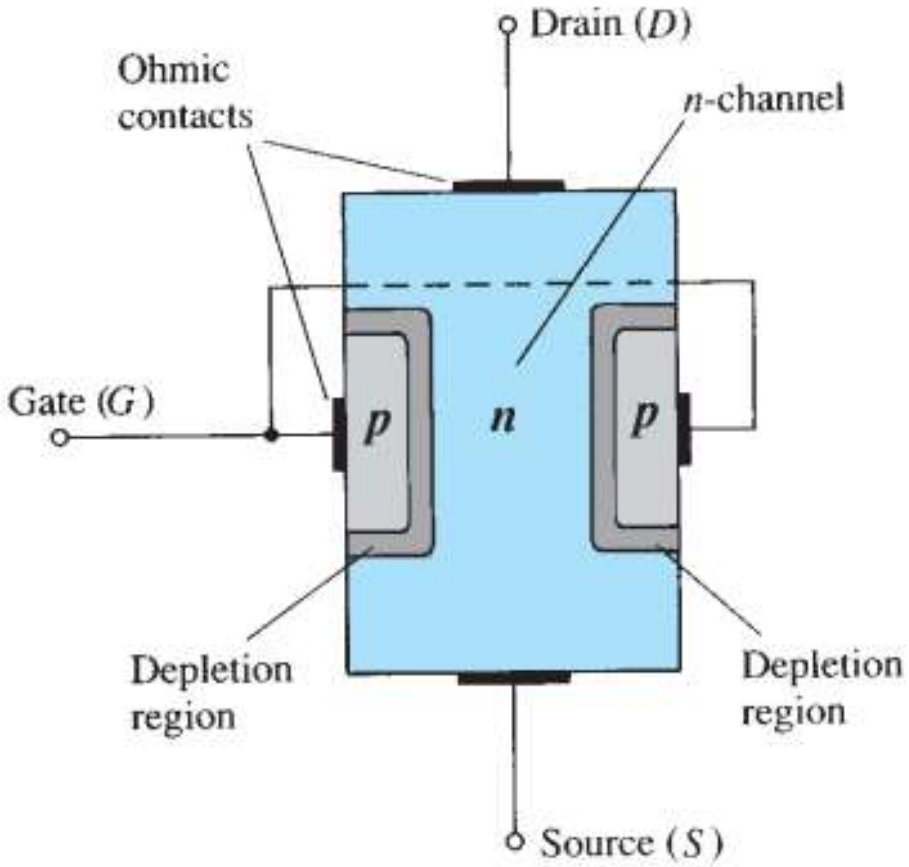
Construction and Characteristics of JFET

- The basic construction of the n-channel JFET is shown in Figure below.
- Note that the major part of the structure is the n-type material that forms the channel between the embedded layers of p-type material.
- The top of the n-type channel is connected through an ohmic contact to a terminal referred to as the drain (D), while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the source (S).

Construction and Characteristics of JFET

- The two p-type materials are connected together and to the gate (G) terminal.
- In essence, therefore, the drain and source are connected to the ends of the n-type channel and the gate to the two layers of p-type material.
- In the absence of any applied potentials the JFET has two p-n junctions under no-bias conditions.

Junction Field Effect Transistor



Junction field-effect transistor (JFET).

Construction and Characteristics of JFET

- In Figure below, a positive voltage VDS has been applied across the channel and the gate has been connected directly to the source to establish the condition VGS = 0 V.

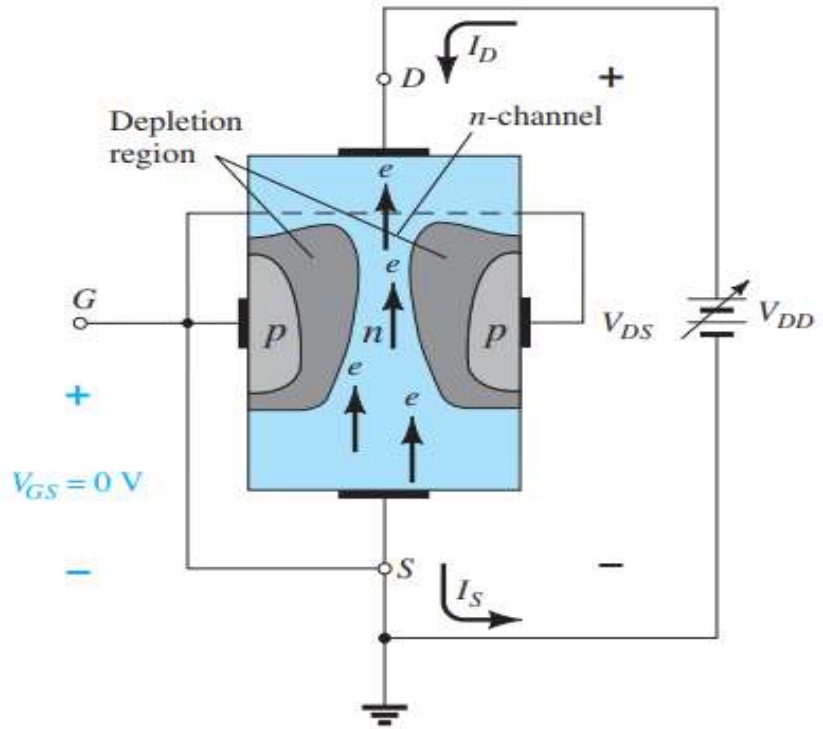
- As the voltage VDS is increased from 0 to a few volts, the current will increase as determined by Ohm's law and the plot of ID versus VDS will appear.

- If VDS is increased to a level where it appears that the two depletion regions would “touch”, a condition referred to as pinch-off will result.

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions

$V_{GS} = 0\ V$ and $V_{DS} > |V_p|$.

Construction and Characteristics of JFET



JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.

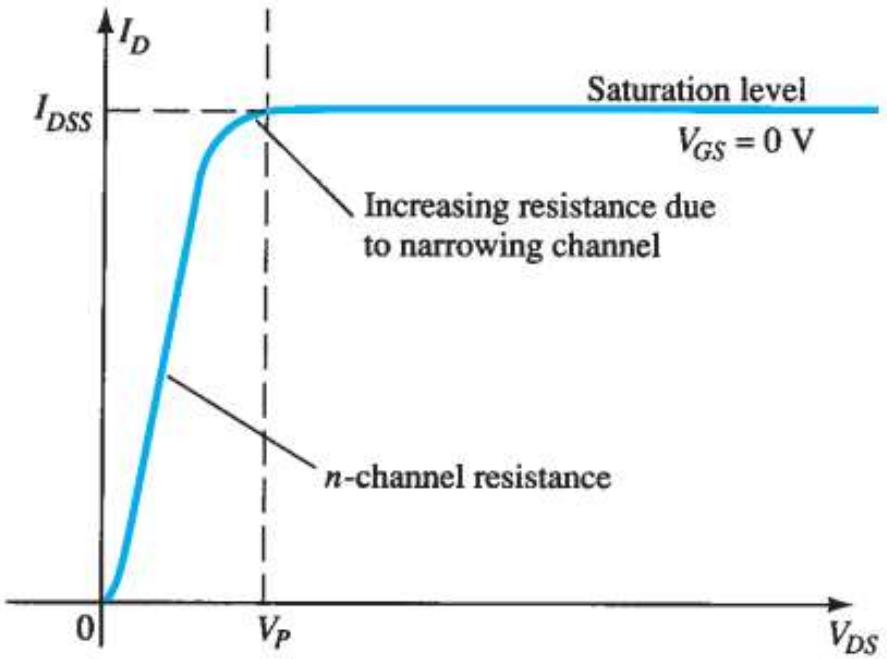


FIG. 6.7

I_D versus V_{DS} for $V_{GS} = 0$ V.

Construction and Characteristics of JFET

- The voltage from gate to source, denoted VGS, is the controlling voltage of the JFET, curves of ID versus VDS for various levels of VGS can be developed for the JFET.

- Note also on the Figure below how the pinch-off voltage continues to drop in a parabolic manner as VGS becomes more and more negative.

- Eventually, VGS when VGS = Vp will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been “turned off.”

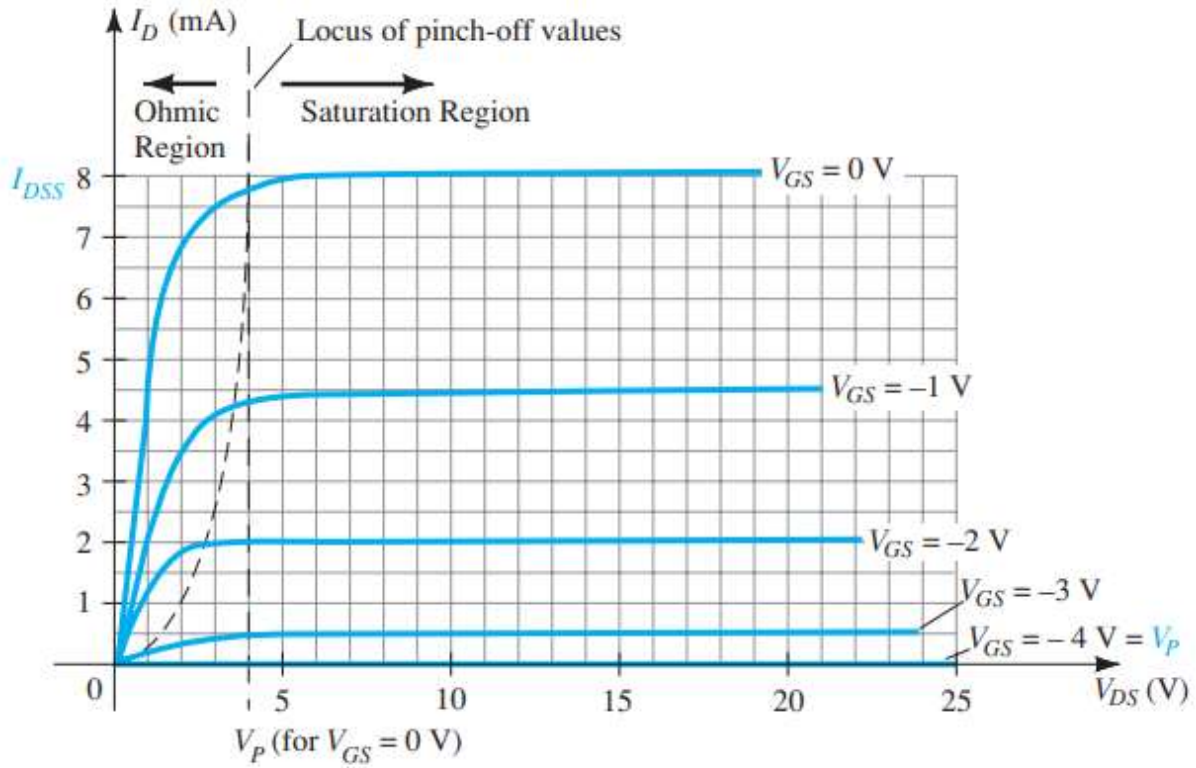
- The level of VGS that results in ID = 0 mA is defined by VGS = Vp , with Vp being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

Construction and Characteristics of JFET

- The region to the left of the pinch-off locus of this Figure is referred to as the ohmic or voltage-controlled resistance region.

- In this region the JFET can actually be employed as a variable resistor (possibly for an automatic gain control system) whose resistance is controlled by the applied gate-to-source voltage

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$



n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.