

Part I
Lectures 1-7
Diode Circuit Applications

The PN Junction Diode

Basic Construction:

When acceptor impurities are introduced into one side and donors into the other side of a single crystal of a semiconductor, a p-n junction is formed. In general, the acceptor ion is indicated by a minus sign because, after this atom "accepts" an electron, it becomes a negative ion. The donor ion is represented by a plus sign because, after this impurity atom "donates" an electron, it becomes a positive ion. Now, if a junction is formed between a sample of p-type and one of an n-type semiconductor, this combination possesses the properties of a rectifier (permits the flow of charge in one direction). Such a two-terminal device is called a p-n junction diode.

- ◀ The two single crystal semiconductors (having four valence electrons) used most frequently in the construction of p-n junction diodes are silicon (*Si*) and germanium (*Ge*).
- ◀ The **p-type** is created by introducing those impurity elements (**acceptors**) that have three valence electrons (trivalent), such as boron, gallium, and indium.
- ◀ The **n-type** is created by introducing those impurity elements (**donors**) that have five valence electrons (pentavalent), such as antimony, arsenic, and phosphorus.
- ◀ In a **p-type material the hole is the majority carrier** and the electron is the minority carrier.
- ◀ In an **n-type material the electron is called the majority carrier** and the hole the minority carrier.
- ◀ The electrons and holes in the region of the junction will combine, resulting in a lack of carriers in the region near the junction. This region of uncovered positive and negative ions is called the **"depletion region"** due to the depletion of carriers in this region.

Essential Characteristics:

The essential electrical characteristic of a p-n junction is that it constitutes a rectifier which permits the easy flow of charge in one direction but restrains the flow in the opposite direction. We consider now how this diode rectifier action comes about.

No Applied Bias ($V_D = 0$ V):

In the absence of an applied bias voltage, the net flow of charge in any one direction for a semiconductor diode is zero (see Fig. 1-1).

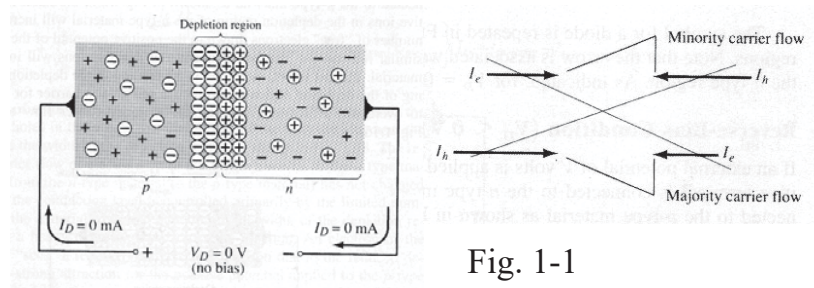
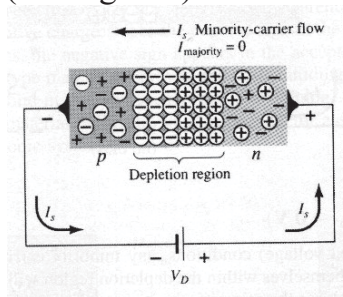


Fig. 1-1

Reverse Bias ($V_D < 0$ V):

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I_s (see Fig. 1-2).

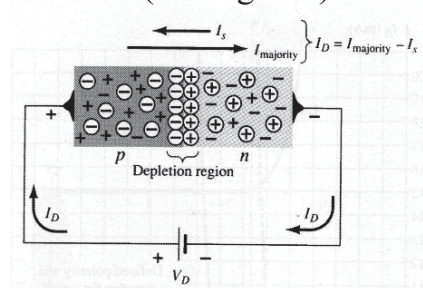
Fig. 1-2



Forward Bias ($V_D > 0$ V):

A semiconductor diode is forward-biased when the association p-type and positive and n-type and negative has been established (see Fig. 1-3).

Fig. 1-3



I-V Characteristic Curve and Current Equation:

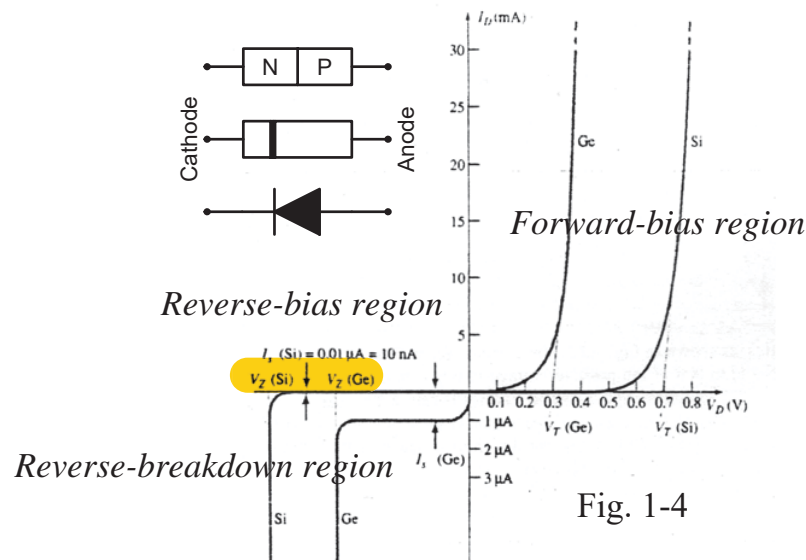


Fig. 1-4

$$I_D = I_s (e^{kV_D/T_K} - 1) \quad [1.1]$$

Where $k = 11600/\eta$ with $\eta = 1$ for Ge and $\eta = 2$ for Si for relatively low levels of diode current and $\eta = 1$ for Ge and Si for higher levels of diode current.

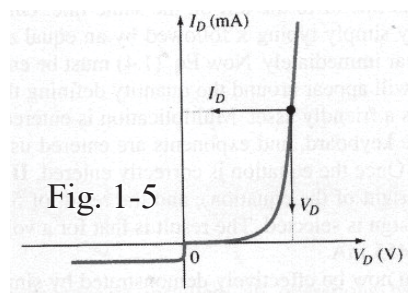
$$T_K = T_C + 273^\circ.$$

Resistance Levels:

1. DC or Static Resistance:

The application of a dc voltage to a circuit containing a p-n junction diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D as shown in Fig. 1-5 and applying the following equation:

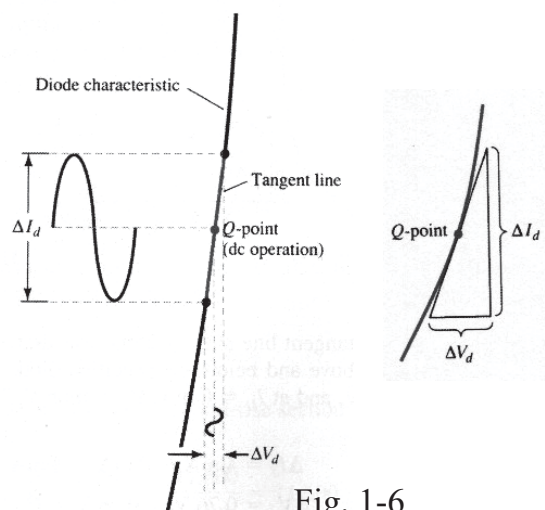
$$R_D = \frac{V_D}{I_D} \quad [1.2]$$



2. Ac or Dynamic Resistance:

If a sinusoidal rather than dc input is applied, the varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1-6. With no applied varying signal, the point of operation would be the Q -point determined by the applied dc levels. A straight line drawn tangent to the curve through the Q -point will define a particular change in voltage and current that can be used to determine the ac or dynamic resistance for this region of the diode characteristics. In equation form,

$$r_d = \frac{\Delta V_d}{\Delta I_d} \quad [1.3]$$



In differential calculus, the derivative of a function at a point is equal to the slope of the tangent line drawn at that point. Eq. [1.3], as defined by Fig. 1-6, is, therefore, essentially finding the derivative of the function at the Q -point of operation. If we find the derivative of the general Eq. [1.1] for the p-n junction diode with respect to the applied forward bias and then invert the result, we will have an equation for the dynamic or ac resistance in that region. That is;

$$\begin{aligned}\frac{d}{dV_D}(I_D) &= \frac{d}{dV}[I_S(e^{kV_D/T_K} - 1)] \\ \frac{dI_D}{dV_D} &= \frac{k}{T_K}(I_D + I_S) \\ \frac{dI_D}{dV_D} &\cong \frac{k}{T_K}I_D \quad (\text{Generally, } I_D \gg I_S) \\ \frac{dI_D}{dV_D} &= 38.93I_D \quad (\eta = 1 \text{ \& } T_K = 298^\circ \Rightarrow \frac{K}{T_K} = \frac{11600}{298} \cong 38.93) \\ r = v/i &= \frac{dV_D}{dI_D} \cong \frac{0.026}{I_D} \\ \boxed{r_d = \frac{26mV}{I_D}} & \quad [1.4]\end{aligned}$$

All the resistance levels determined thus far have been defined by the p-n junction and do not include the resistance of the semiconductor material itself (called **body resistance**) and the resistance introduced by the connection between the semiconductor material and the external metallic conductor (called **contact resistance**). These additional resistance levels can be included in Eq. [1.4] by adding resistance denoted by r_B appearing in Eq. [1.5].

$$\boxed{r'_d = \frac{26mV}{I_D} + r_B} \quad [1.5]$$

3. Average AC Resistance:

If the input signal is sufficiently large to produce a forward swing such as indicated in Fig. 1-7, the resistance associated with the device for this region is called the average ac resistance. The average ac resistance is, by definition, the resistance determined by a straight line drawn between the two intersection points established by the maximum and minimum value of input voltage. In equation form,

$$\boxed{r_{av} = \left. \frac{\Delta V_d}{\Delta I_d} \right|_{pt. \text{ to } pt.}} \quad [1.6]$$

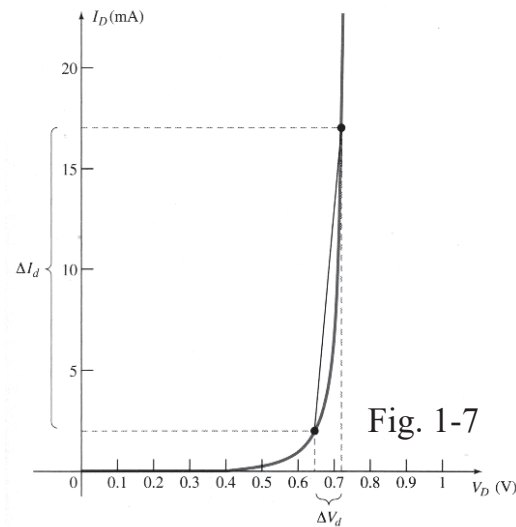
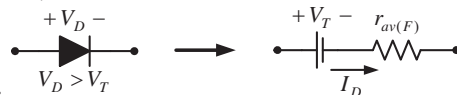


Fig. 1-7

Equivalent Circuits (Models):

1. Piecewise-Linear Model: (see Fig.1-8);

Forward-bias;



Reverse-bias;

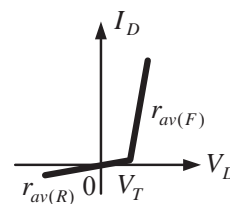


Fig. 1-8

2. Simplified Model: (see Fig. 1-9);

Forward-bias & $R_{network} \gg r_{av(F)}$;



Reverse-bias, $r_{av(R)} = \infty \Omega$ & $I_D = 0$ A;

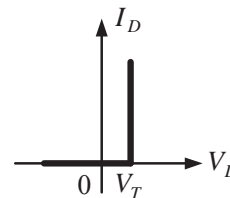


Fig. 1-9

3. Ideal Model: (see Fig. 1-9);

Forward-bias, $E_{network} \gg V_T$, $R_{network} \gg r_{av(F)}$ & $V_D = 0$ V;



Reverse-bias, $r_{av(R)} = \infty \Omega$ & $I_D = 0$ A;

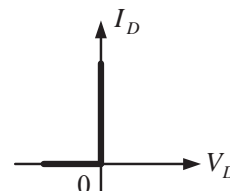
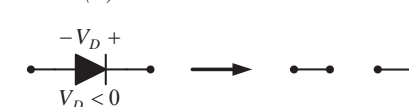


Fig. 1-10

Load-Line Analysis:

From Fig. 1-11:

$$E - V_D - V_R = 0$$

$$E = V_D + I_D R$$

$$I_D = -\frac{V_D}{R} + \frac{E}{R} \quad [1.7]$$

Eq. [1.7] is a linear equation;

$$y = mx + c,$$

where $m = -1/R$ & $c = E/R$.

$$\begin{aligned} I_D = 0 &\Rightarrow V_D = E \\ V_D = 0 &\Rightarrow I_D = \frac{E}{R} \end{aligned} \quad [1.8]$$

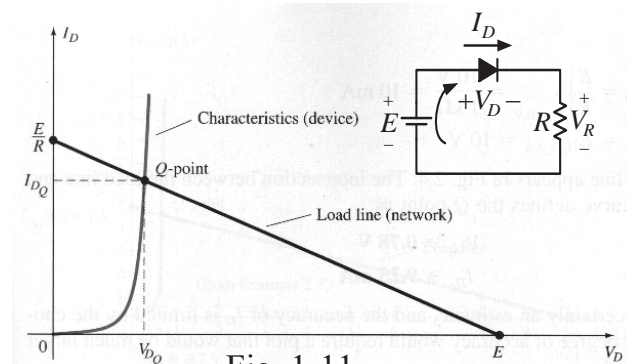


Fig. 1-11

Example 1-1:

Determine the currents I_{D1} , I_{D2} , and I_{R1} for the network of Fig. 1-12.

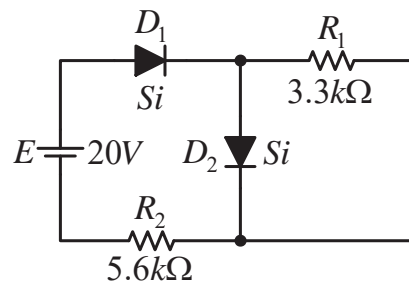


Fig. 1-12

Solution:

$$I_{R1} = \frac{V_{D2}}{R_1} = \frac{0.7}{3.3k} = 0.212mA.$$

Applying KVL yields:

$$-V_{R2} + E - V_{D1} - V_{D2} = 0$$

$$\text{and } V_{R2} = E - V_{D1} - V_{D2} = 20 - 0.7 - 0.7 = 18.6V,$$

$$\text{with } I_{D1} = \frac{V_{R2}}{R_2} = \frac{18.6}{5.6k} = 3.32mA.$$

$$\text{Finally, } I_{D2} = I_{D1} - I_{R1} = 3.32mA - 0.212mA = 3.108mA.$$