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Bus signal timing & I/O timing .

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1. Introduction to Bus Signals

- **What is a Bus?**
  - A bus is a collection of lines or wires used for transferring data between different components in a digital system.
  - It can be **unidirectional** (data flows in one direction) or **bidirectional** (data flows in both directions).
  - There are different types of buses, including **Data Bus**, **Address Bus**, and **Control Bus**.
- **What are Bus Signals?**
  - **Data Signals**: Carry the actual data being transferred.
  - **Address Signals**: Specify the address in memory or a device.
  - **Control Signals**: Control the flow of data across the bus (e.g., read/write signals).

2. **Timing Diagrams**: is a graphical representation of the signals of a system over time. In the case of the **8086 microprocessor**, timing diagrams are used to describe the sequence of events (signals) that occur during the execution of an instruction cycle.

T-state:

One sub division of an operation performed in one clock cycle is called a T-state . T1,T2,T3,T4 are called state.

Machine cycle :

Machine cycle: A group of state come together to perform one operation is called machine cycle. The basic operation of reading/writing a byte from/to a memory location/a port is called a machine cycle. The time taken to complete a machine cycle is represented as Tcy. A machine cycle is made up of many states.

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Instruction cycle: The total time for fetching and executing an instruction is called instruction cycle. An instruction cycle consists of one or more machine cycle. In 8086, the concept of a machine cycle is not so relevant. The Execution Unit (EU) executes instruction in certain clock periods. These clock cycles do not constitute any form of machine cycles. The Bus Interface Unit (BIU) fetches instructions and operands from the memory. Any external access either to the memory or I/O device requires four clock periods.

Key Signals in 8086 Timing Diagrams:

1. **Clock (CLK)**: This is the main timing signal, which is generated by an external oscillator. The clock cycles coordinate the timing of all other signals.
2. **Address Bus (A0-A19)**: The 8086 microprocessor uses a 20-bit address bus (A0-A19) to specify the memory or I/O address during operations. These signals are used to address memory locations or ports.
3. **Data Bus (D0-D15)**: The data bus is a 16-bit bus used to transfer data between the CPU and memory or I/O devices.
4. **Read (RD)**: The read signal indicates whether the 8086 is reading data from memory or an I/O port. When **RD** is low, it means the CPU is reading data.
5. **Write (WR)**: The write signal indicates whether the 8086 is writing data to memory or an I/O port. When **WR** is low, it means the CPU is writing data.
6. **Memory/IO (M/IO)**: This signal distinguishes between memory and I/O operations. When the signal is low, it indicates a memory operation; when it is high, it indicates an I/O operation.

8086 Instruction Cycle Timing Diagram:

The 8086 microprocessor follows a series of phases during the execution of an instruction, and these phases are represented in the timing diagram. Let's break down a basic example of an instruction cycle:

1. **Phase 1: Fetch Cycle**
    - **Address Bus (A0-A19)**: The 8086 places the address of the instruction in the address bus.
    - **ALE (Address Latch Enable)**: ALE goes low to latch the address into memory.
    - **RD (Read)**: The 8086 asserts the read signal to fetch data from memory.
    - **CLK**: The clock cycles coordinate the timing of these events.
2. **Phase 2: Operand Fetch**
    - **Data Bus (D0-D15)**: The CPU fetches the data (operand) from memory or I/O.
    - **RD (Read)**: This signal is asserted to read the operand.
3. **Phase 3: Execution**
    - During this phase, the CPU executes the operation (such as addition, subtraction, etc.). This phase is internal to the CPU and involves no external signals, but the CPU may interact with the data bus for reading/writing results.

Example Timing Diagram for a Memory Read (MOV AX, [BX]):

Let's consider the example instruction `MOV AX, [BX]`, which involves reading data from a memory address specified by the value in the **BX** register and storing it in the **AX** register. The following steps occur:

1. **Address Fetch**:
    - The **BX** register holds the address.
    - The 8086 places the address on the address bus (A0-A19).
    - The **ALE** signal is asserted to latch the address.
    - The **RD** signal is asserted to read from memory.
2. **Memory Read**:
    - The memory responds by placing the data on the data bus (D0-D15).
    - The **RD** signal stays low, indicating the data is being read.
3. **Store Data**:
    - The data is moved into the **AX** register.

Basic Timing Diagram Example (MOV AX, [BX]):

```
mathematica
Copy code
Clock Cycles      1      2      3      4      5      6      7      8      9
                  ------------------------------------------------------------
ALE                 ↑
Address Bus       A0-A19  A0-A19  A0-A19  A0-A19  A0-A19
Read (RD)                ↓      ↓      ↓      ↓      ↓      ↓      ↓
Write (WR)
Data Bus                        D0-D15  D0-D15  D0-D15
```

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