Department of Biomedical Engineering
Digital Electronics / Third stage
Lecturer: Dr. Hussam Jawad Kadhim AL_Janabi
Email: hussam.jawad@uomus.edu.iq

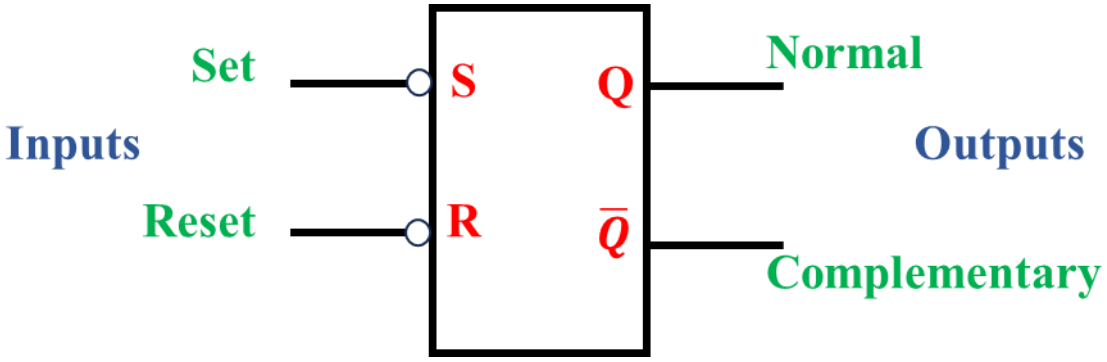
Lecture Six

Flip Flop

Logic circuits are classified into two broad categories. The combinational logic circuits and the sequential logic circuit. The basic building block of combinational logic is the logic gate. The basic building block of the sequential logic circuit is the *flip-flop* circuit.

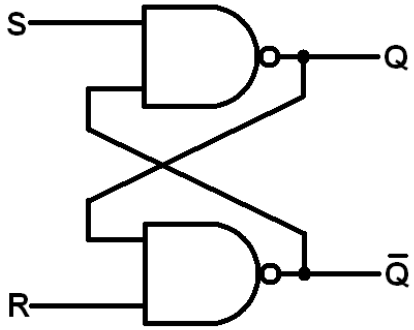
1- RS FLIP-FLOP

The most basic flip-flop is called the *RS flip-flop.* **A** block logic symbol for the *RS* flip-flop is shown in the figure below. The logic symbol shows two inputs, labeled *set* **(S)** and *reset (R),* on the left. The ***RS*** flip-flop in this symbol has **active LOW** inputs, shown as small bubbles at the **S** and *R* inputs. Unlike logic gates, flip-flops have two complementary outputs. The outputs are typically labeled Q and $\overline{Q}$.

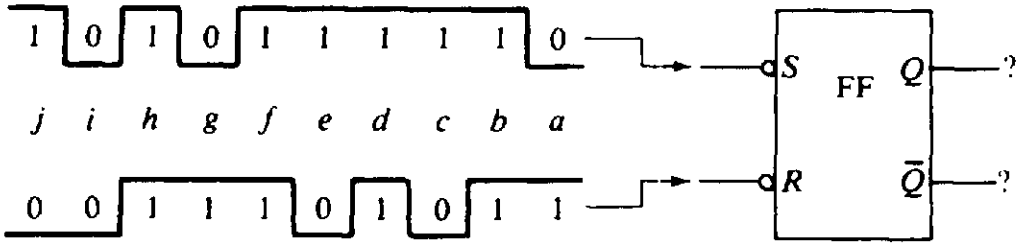


The ***RS*** flip-flop can be constructed from logic gates. ***An*** *RS* flip-flop is shown wired from two **NAND** gates. **As** with logic gates, a truth table defines the operation of the flip-flop. Line 1 of the truth table is called the *prohibited state* in that it drives both outputs to 1, or HIGH.

Mode of operation	Input		Output	
	S	R	Q	$\overline{Q}$
Prohibited	0	0	1	1
Set	0	1	1	0
Reset	1	0	0	1
Hold	1	1	No change	



Example: List the *binary* outputs at the normal output **(Q)** of the ***RS*** flip-flop shown in the Figure below.



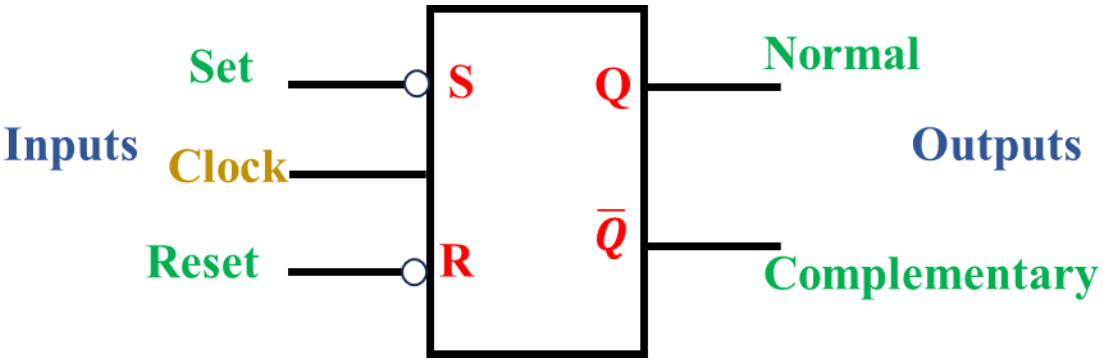
Solution

The binary output at the output Q is as follows:

a= 1, b= 1, c= 0, d= 0, e=0, f= 0, g=1, h=1, i=1 (prohibit state), j=0.

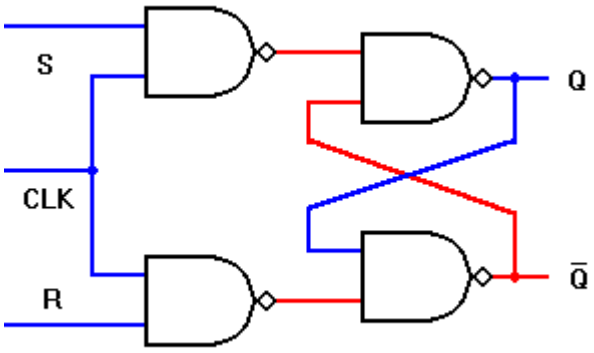
CLOCKED *RS* FLIP-FLOP

The clocked *RS* flip-flop *operates in step with the clock* or timing device. In other words, it operates synchronously. **A** logic symbol for the clocked *RS* flip-flop is shown below. It has the set ***(S)*** and reset *(R)* inputs and the added clock (CLK) input.

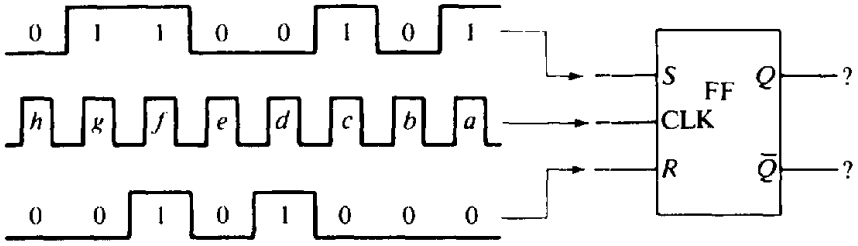


It should be emphasized that the **S** and *R* inputs are active during the entire time the clock pulse level is **HIGH**. The **HIGH** of the clock pulse may be thought of as an enabling pulse.

Mode of operation	Input		Output	
	S	R	Q	$\overline{Q}$
Hold	0	0	No change	
Reset	0	1	0	1
Set	1	0	1	0
Prohibited	1	1	1	1



Example: List the binary output at Q for the flip-flop shown in the figure below during the eight clock pulses.



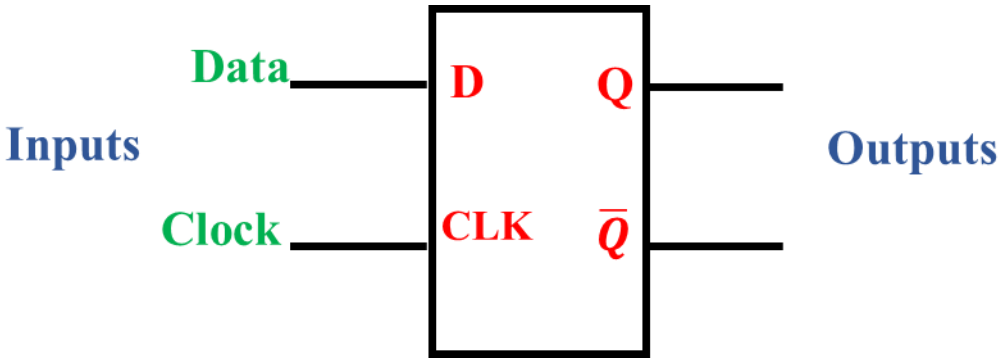
Solution:

The binary outputs at Q for the clocked ***RS*** flip-flop of is as follows:

a= 1, b= 1, c= 1, d= 0, e=0, f= 1 (Prohibit condition), g=1, h=1

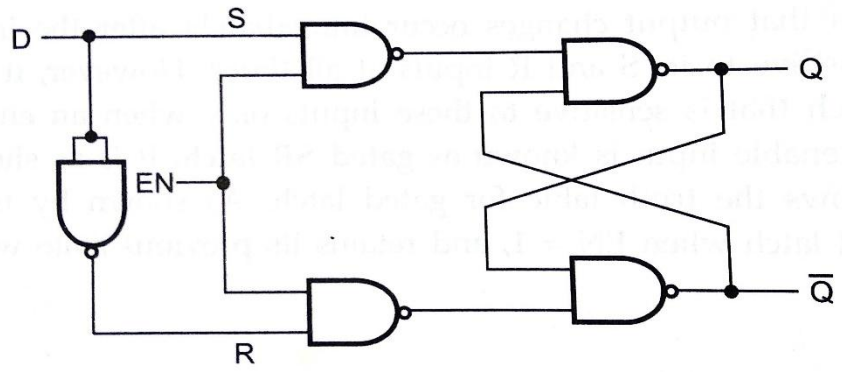
D FLIP-FLOP

The *D flip-flop* has only a single *data* input *(D)* and a clock input (CLK). The D flip-flop is often called a *delay* ***flip-flop.***

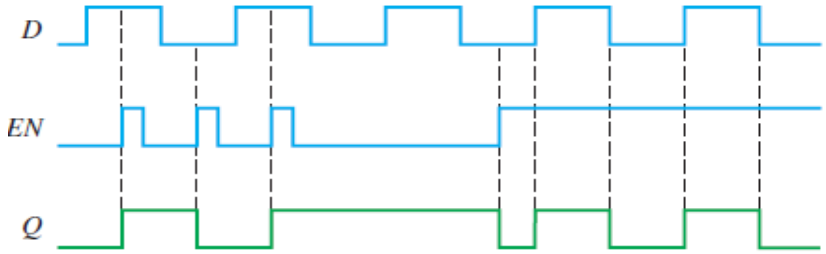


Lecturer: Dr. Hussam Jawad Kadhim AL_Janabi
Email: hussam.jawad@uomus.edu.iq

The clocked *RS* flip-flop can be converted to a ***D*** flip-flop **by** adding an inverter



Example: Determine the *Q* output waveform if the inputs shown in the figure below are applied to a D flip flop.

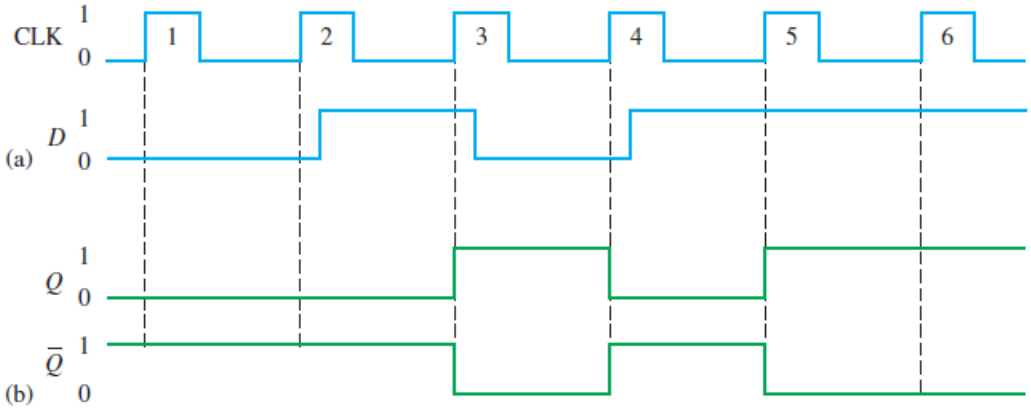


Solution

When *D* is HIGH and *EN* is HIGH, *Q* goes HIGH. When *D* is LOW and *EN* is HIGH, *Q* goes LOW.

Example 2Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Figure below for the D and CLK.

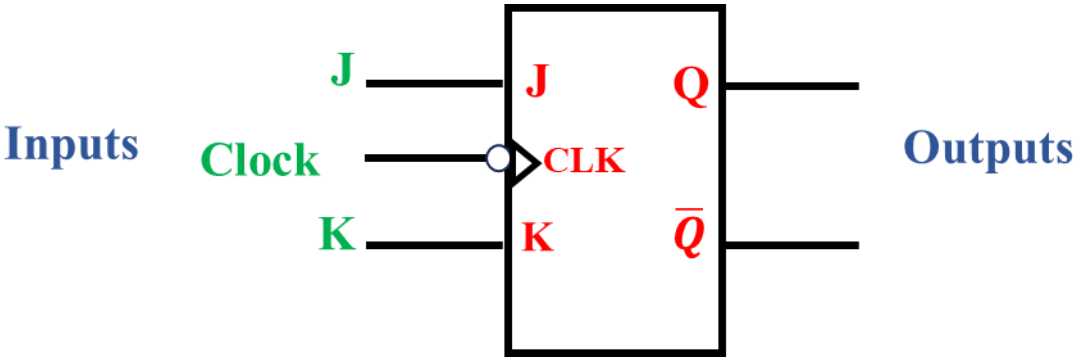
Solution



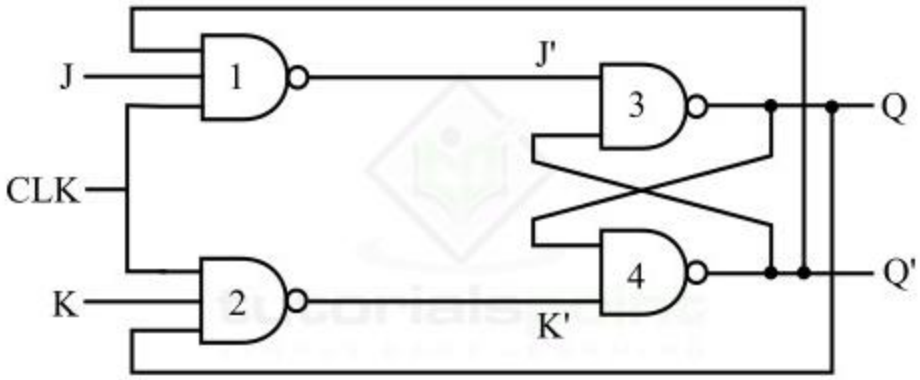
Department of Biomedical Engineering
Digital Electronics / Third stage
Lecturer: Dr. Hussam Jawad Kadhim AL_Janabi
Email: hussam.jawad@uomus.edu.iq

JK FLIP-FLOP

The logic symbol for a ***JK*** flip-flop is shown in the figure below. This device might be considered the universal flip-flop, other types can be made from it. The logic symbol has three synchronous inputs ***(J,*** *K*, and CLK).

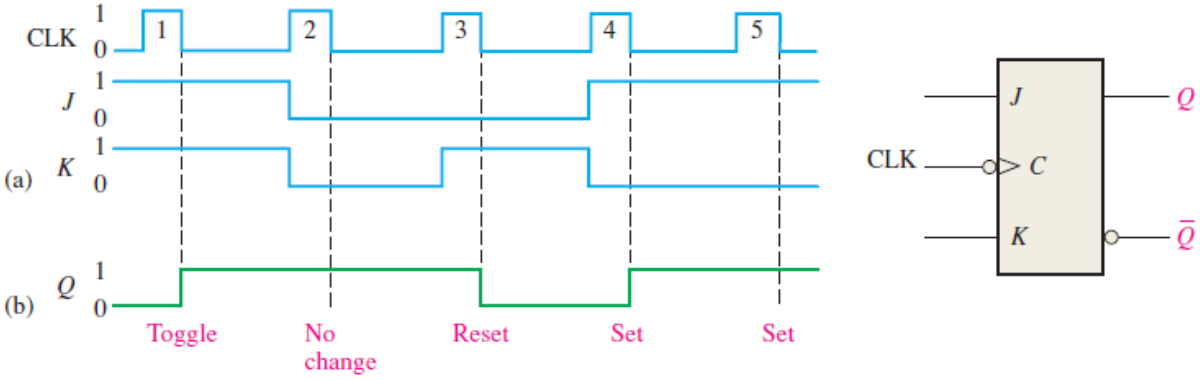


Mode of operation		Input		Output	
	CLK	J	K	Q	$\overline{Q}$
Hold	pulse	0	0	No change	
Reset	pulse	0	1	0	1
Set	pulse	1	0	1	0
Toggle	pulse	1	1	Opposite state	

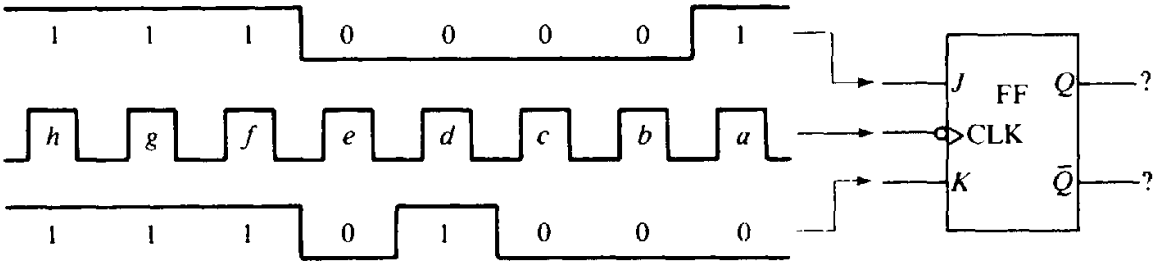


Example: The waveforms in the Figure below are applied to the *J*, *K*, and clock inputs as indicated. Determine the *Q* output.

Solution



Example 2: List the *binary* output at output Q of the *JK* flip-flop of the figure after each of the eight clock pulses.

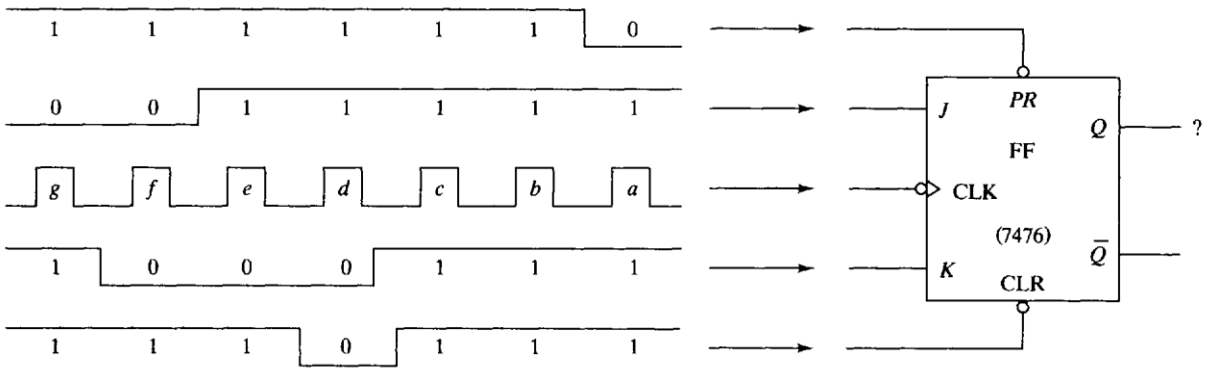


Solution

The binary output (Q) after each clock pulse is as follows:

a= 1, b= 1, c= 1, d= 0, e=0, f= 1, g=0, h=1

Example: List the mode of operation of the JK flip-flop during each of the seven clock pulses shown in the figure below



Solution

pulse is as follows:

pulse *a* = 1

pulse *b* = 0

pulse ***c*** = 1

pulse d = 0

pulse ***e*** = 1

pulse ***f*****= 1**

pulse g = 0