PC Interfacing

Fourth Level

6 lec

ADCs Converter with Parallel I/O Interface

Analogue-to-digital converters (ADC)

Flash: Highest conversion rate (speed), but low accuracy.

Dual slop: Highest conversion accuracy, but low speed.

Successive approximation: is a good compromise on speed & accuracy**.**

I/O Interface between converters and external circuits can be parallel or serial with control lines required for both.

A/D converters with parallel I/0 interface:-

(a) CA3306 Flash Converter:-

The principle of flash converters is that the input signal is compared with all possible subdivisions of a reference voltage at the same time (see Figure 6.1). The reference voltage (V ref) is divided by a series of resistors. The code generated by the comparators is converted to a binary code by an encode circuit. The number of comparators grows rapidly with the number of bits. An n-bit converter requires 2^n comparators!

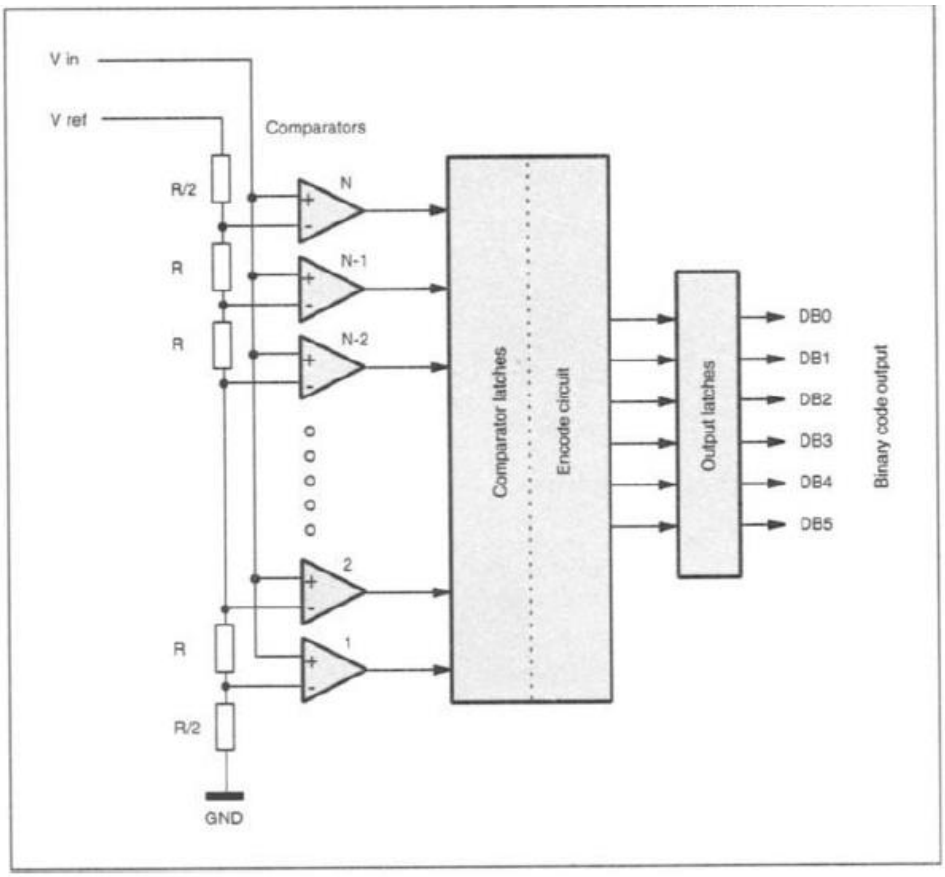

Figure 6.1 Principle of 6-bit flash A/D converters

The CA3306CE has a conversion rate of 15 MHz and 6-bit conversion accuracy. It has 64 comparators and requires a power supply from 3 to 7.5V. The power consumption

is about 50 mW. The pin-out of the chip is given in Figure 6.2. B1 through to B6 output the conversion data. There are two enable pins: CE2 (pin 5) and-CE1 (pin 6). When CE2-1 and -CE1-0, the conversion data appears on B1 to B6 outputs, otherwise the outputs are in the high impedance state. Pin 7 is a Clock input and pin 8 (Phase) controls the sequential operation of A/D conversion. When Phase is high, the rising edge of the clock starts a sampling cycle. When the clock is at the high state, comparators compare the input signal with the reference. At the falling edge of the clock, the converted data from the comparators is latched into the comparator latches. During the low state of the clock, the data propagates through the encode circuit and the encoded data appears at the input of the output latches. At the next rising edge of the clock, the data is latched into the output latches and appears on the pins. At the same time, it initializes a new sampling cycle. V ref- (pin 10) and V ref+ (pin 9) are the voltage reference to the converter.

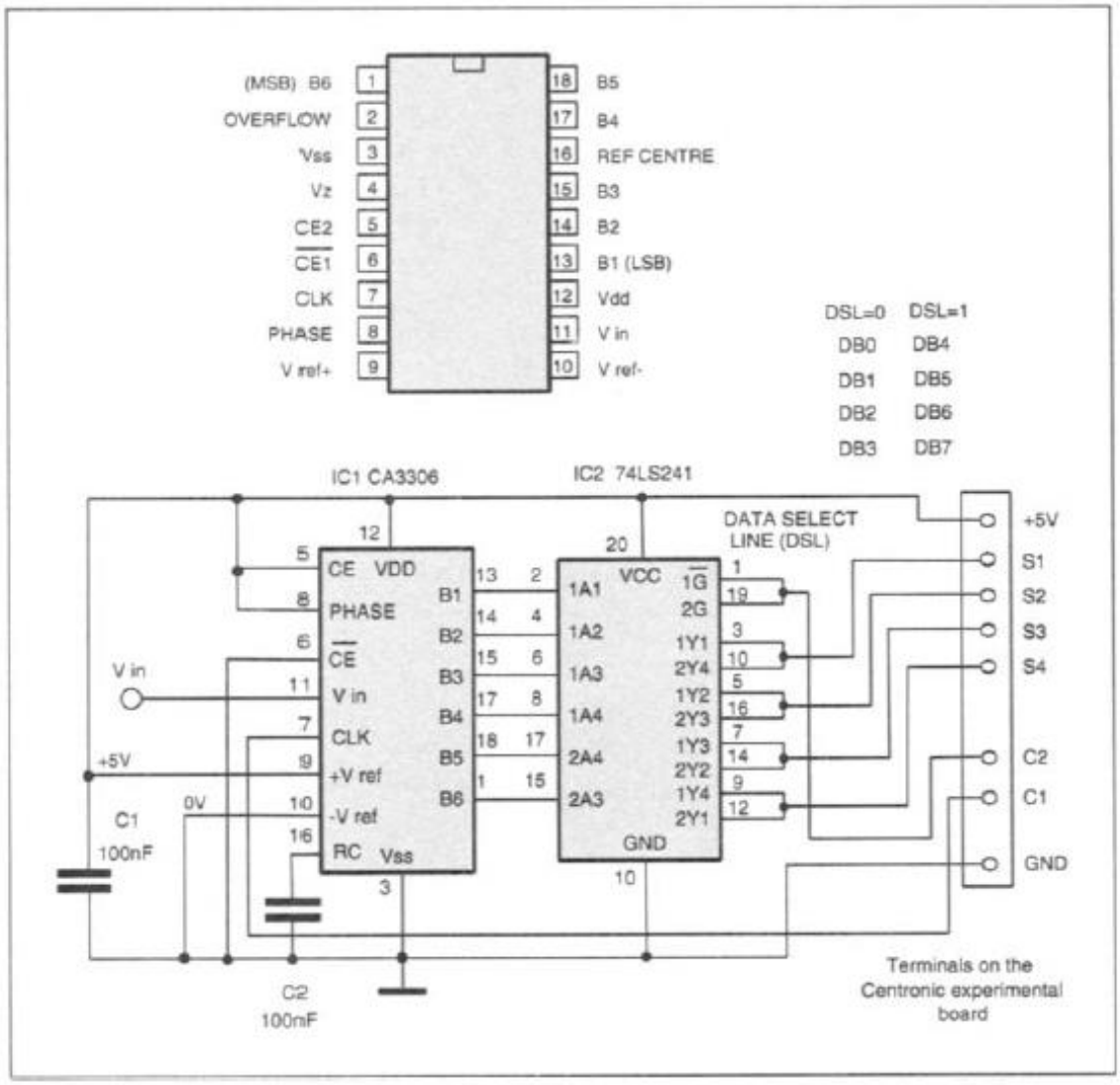

Figure 6.2 Pin-out and experimental circuit of the CA3306

The experimental circuit is given in Figure 6.2. It is connected to the Centronic experimental board. The circuit uses a 74LS241 buffer IC which allows the computer to read the 6-bit conversion data via four input lines. C1 from the Centronic experimental board is connected to the Clock input of the CA3306. To read the previous A/D conversion result and to start a new conversion. The 74LS241 splits the 6-bit data into two parts: the upper two bits and the lower four bits. The two parts are read into the computer in turns using the Data Select Line (DSL).

The data transfer between the CA3306 and the computer is too slow. A solution to this problem is to allow the flash A/D converter to write data temporally into memory buffers. The A/D conversion results can be stored in the buffer at a much higher speed. When the buffer is full, the data are downloaded into the computer.

(b) ZN449 Successive Approximation ADC:

A successive approximation analogue-to-digital converter consists of the following parts: a digital-to-analogue converter, a comparator and a successive-approximation register. Figure 6.3 shows the internal block diagram of a typical 8-bit successive approximation converter. Each bit is brought to logic high successively to test if the output voltage from the D/A converter is higher or lower than the input voltage. If the DAC voltage is higher than the input voltage, the value of the tested bit should return to zero. If the DAC voltage is lower than the input, the value of the tested bit is 1. By testing each bit in such a manner, a value can be established.

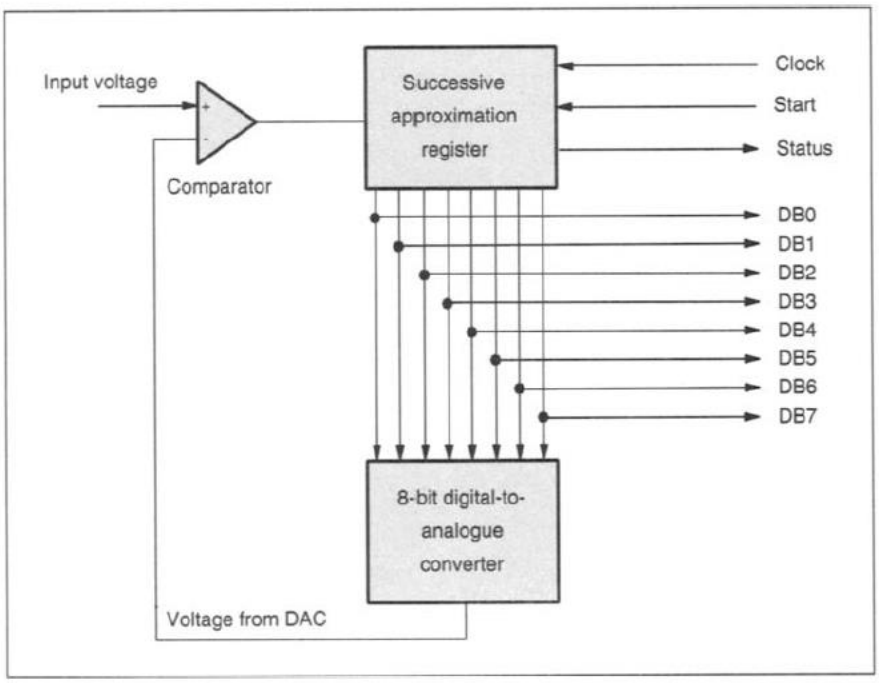

Figure 6.3 Successive approximation ADC

The ZN449 or ZN448 is an 8-bit successive approximation A/D converter. It has a minimum conversion time of 9 µs. An on-board clock generator. The pin-out of the converter is given in Figure 6.4. When the -CONVERT input (pin 4) becomes low, ADC begins an A/D conversion and the -BUSY output (pin 1) becomes low. The -BUSY output will go high at the end of the conversion indicating that the conversion is completed. The -RD input (pin 2) is the data enable line which is taken low to enable the data on the output lines (DB0 to DB7, pins 18 to 11) which otherwise are in the high impedance state.

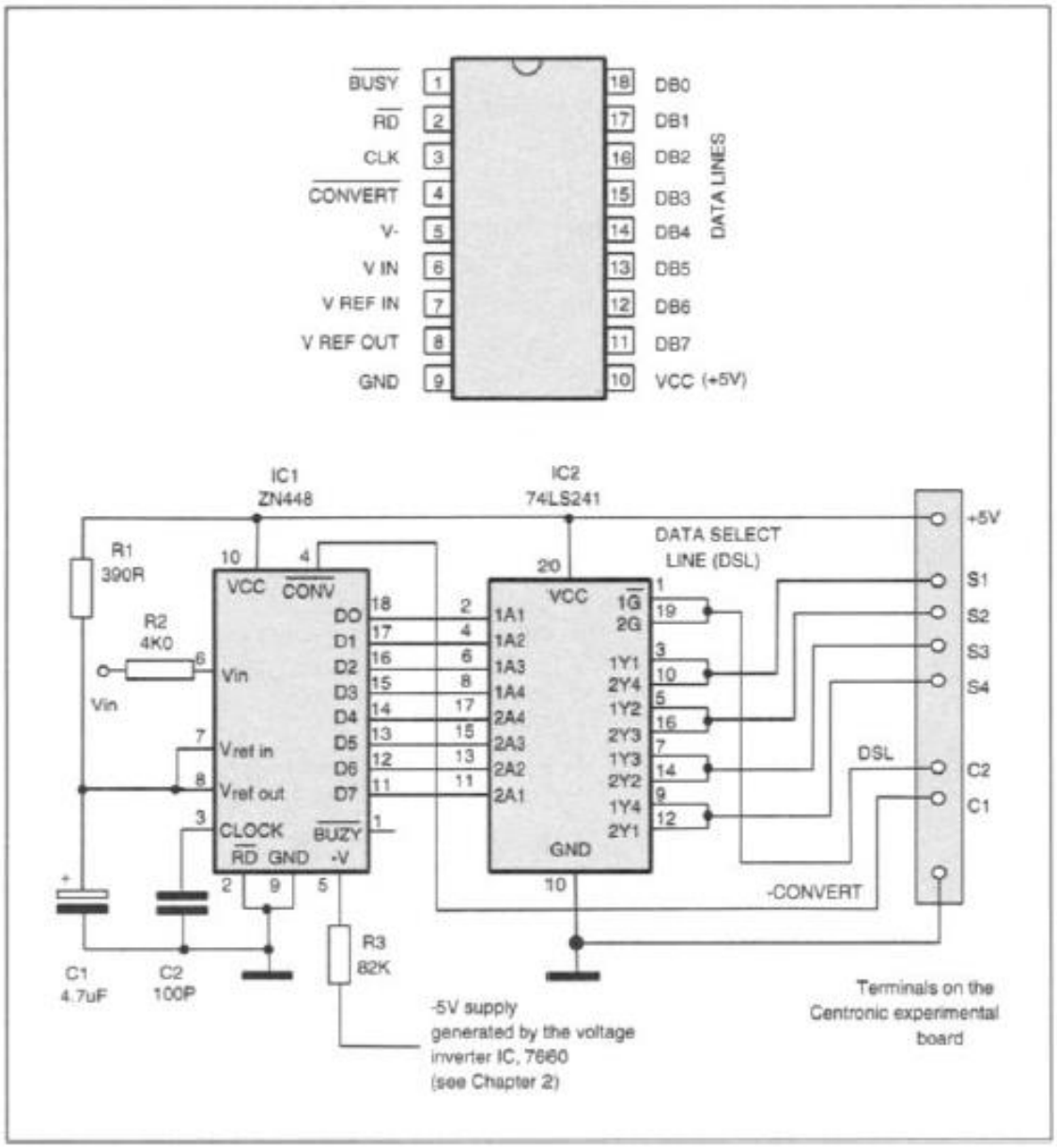

Figure 6.4 Pin-out of the ZN449 and experimental circuit

A clock capacitor (C2) is connected between pin 3 and the ground (pin 9) which enables the onboard clock generator to generate a clock signal. The maximum clock

frequency is obtained with a capacitor value of 100 pF. A negative power supply ranging from-3V to-30V can be supplied to pin 5 (-V) via a resistor. When the negative voltage is -5V, the resistor value is 82 K. Pin 8 is the output of the on-board 2.5V reference Vref out. The input voltage to be measured is fed to Vin (pin 6) via a 4K resistor. A 2.5V input voltage will produce a byte of 255 decimal at the output of the converter. The decimal values for other input voltages are calculated using the following equation:

Decimal value = (Input voltage x 255) / 2.5

The experimental circuit is shown in Figure 6.4. The circuit is connected to the Centronic experimental board. The -CONVERT is connected to C1 terminal; Data Select Line for the 74LS241 is connected to C2 terminal of the experimental board. The data is read into the computer via S1 to S4.

(c) ICL7109 12-bit Integrating A/D Converter (Dual – Slope):-

The working principle of an integrating A/D converter is described in Figure 6.5. The technique involves an integrator and a negative reference voltage. The conversion is in two phases: the signal integration phase and reference de-integration phase. In the first phase, S1 is closed (S2 open) to supply the input voltage to the integrator for a fixed period of time, T_{INT}. After this, the reference de-integration phase starts. S1 is open and S2 is closed. This action supplies the input of the integrator with the negative reference. The capacitor of the integrator starts to discharge at a rate determined by the reference voltage. After a period of T_{DEINT}, the output of the integrator crosses the zero volt level. Knowing the two time periods, the input voltage can be calculated using the following equation:

Input voltage = $(V_{ref} * T_{DEINT}) / T_{INT}$

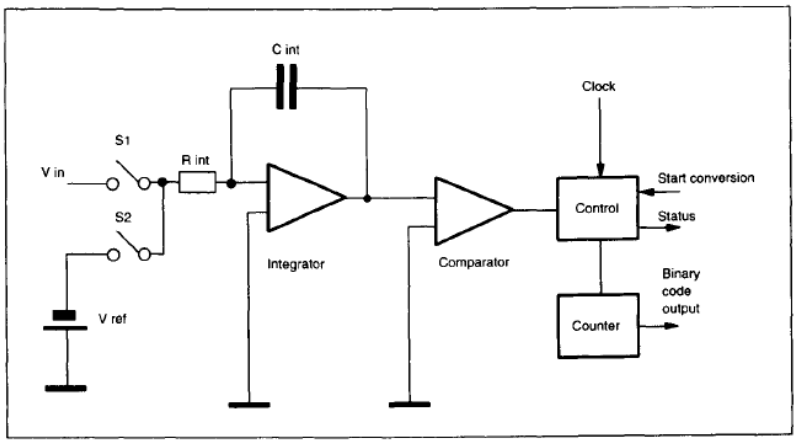

Figure 6.5 Dual-slope integrating A/D converter

An advantage of using a dual-slope converter is that random noise can be averaged to zero during the signal integration phase. It also provides noise rejection automatically. Interference signals with a fixed frequency can be removed by choosing the right integrating period. The integrating converters often have an integration period to reject 50/60Hz mains frequency interferences.

The ICL7109ACPL is a low-power, 12-bit integrating A/D converter. The pin-out is given in Figure 6.6.

The analogue section of the ICL7109 needs four external components. They are the reference capacitor, C_{REF}, the auto-zero capacitor, C_{AZ}, the integrating capacitor C_{INT} and the integrating resistance R_{INT}. The on chip oscillator operates with a 3.5795 MHz TV crystal giving 7.5 conversions per second. The device could work with a conversion rate of 30 samples per second. The IC also provides a reference voltage (pin 29) which is nominally 2.8V.

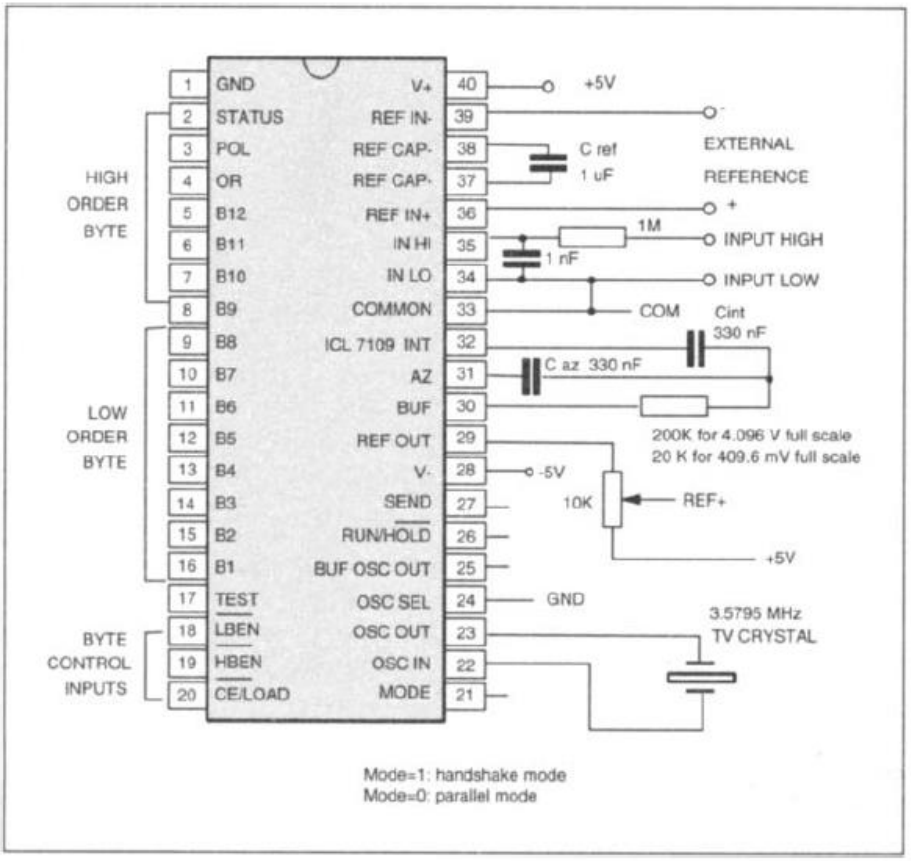

Figure 6.6 Pin-out of the ICL7109 and a typical connection

If RUN/-HOLD (pin 26) high state, the ADC performs conversions continuously. If it is low, the conversion is one shot. The conversion results appear at the 14 tri-state outputs B1 to B12. B1 through B12 give the conversion data.

Data can be read from in one of the two modes: the direct mode and the handshake mode. Data transfer mode is configured using the Mode (pin 21) input, MODE-0 to select the direct mode and MODE-1 to select the handshake mode. In the direct mode, the 12-bit conversion data is accessible from the output pins under the control of-CE/LOAD, and -LBEN. All the pins are active low. The chip enable -CE/LOAD is low to enable the IC. When -LBEN is low, B1 to B8 output the data. When -LBEN is high, B1 to B8 are in the high impedance state. During a conversion, the STATUS goes high. It goes low after the converted data is latched into the output latches. ICL7109 can be connected to a 6402 UART in the handshake mode.

When the ICL7109 operates in the direct mode, it can be connected to a computer via an 8255 PPI or a 16-to-1 data selector circuit. An experimental circuit diagram using two 4051 analogue switches is shown in Figure 6.7. The circuit is connected to the Centronic experimental board.

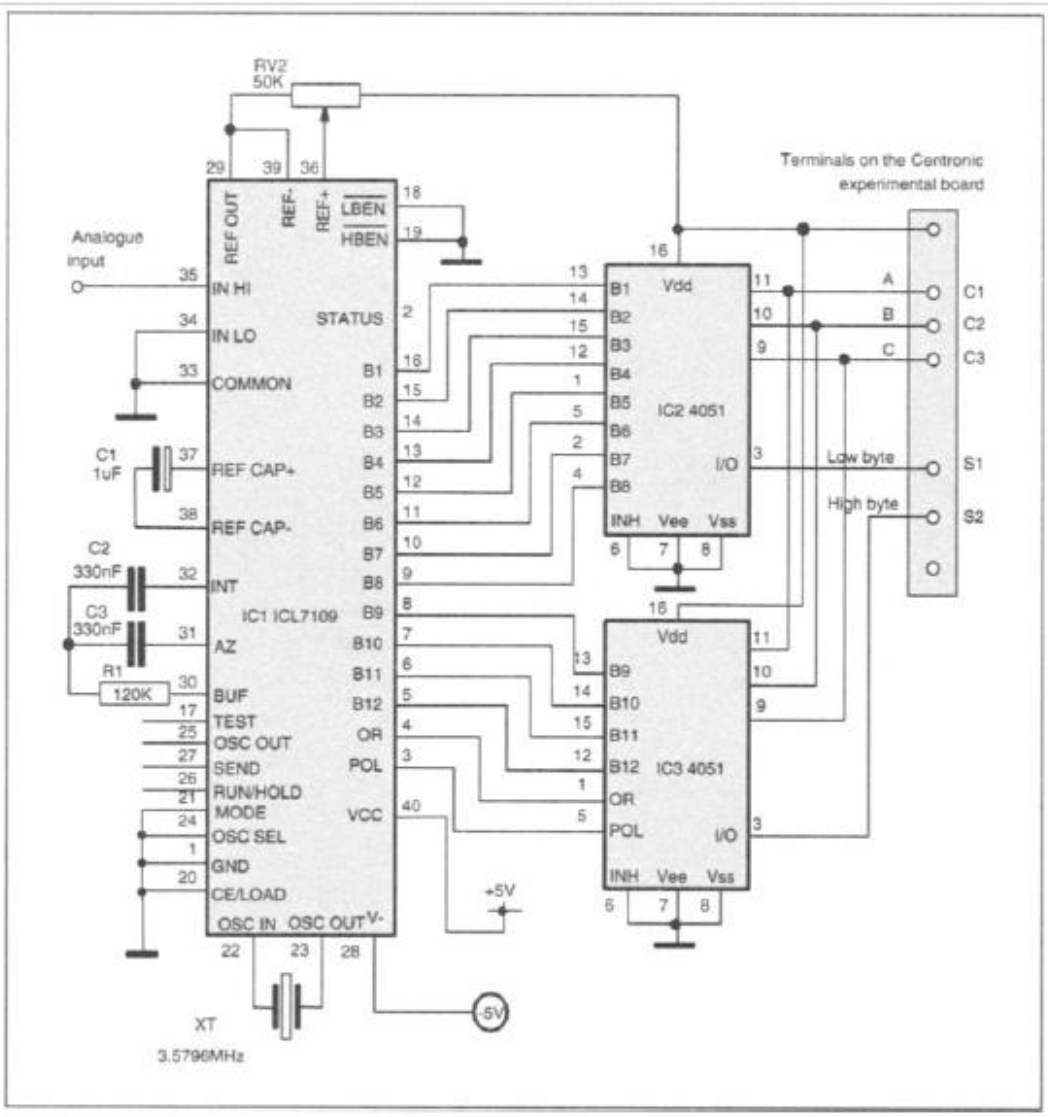

Figure 6.7 Experimental circuit of the ICL7109