**Name:**

Q1 - When an application program is tested on a microcomputer system with A code cache it is found that 900 instruction acquisition bus cycles are from the cache memory and 100 are from main memory. What is the hit rate? Assume Cache run in lone cycle 5ns, and main memory run 10 cycles what is over all access time?

Q2 - A processor has an on-chip cash that runs in one cycle of 5 ns. This cash has a hit rate of 90%. A second-level cache runs in three cycles and has a hit rate of 75% of all accesses that are not found and on-chip cache all accesses that are not found in either cash are found in main memory with an excess time of 50 ns. Calculate the overall memory access time.

Q3- Calculate the tag, word and block/set needed if the memory blocks 4K. Assume that the each line of the memory contain 27 words and the cache size is 2K, for the following cases:

1. Direct mapping. 2) 2-ways set associative mapping. 3) Associative mapping.

Q4- Compare between the SRAM and the DRAM.