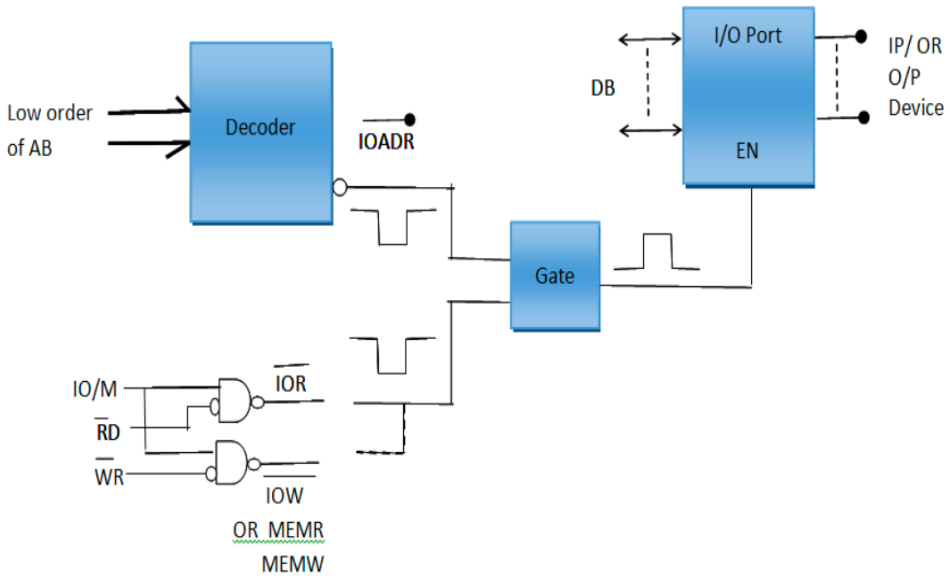
Interfacing I/O Devices

- I/O devices are the communications channels between the MP and the outside world.
- Data transfer
  - Parallel I/O mode (group of bits transferred simultaneously via group of lines)
  - Serial I/O mode (one bit is a transferred via single line at a time
- Interfacing techniques
  - Peripheral- mapped I/O
  - Memory – mapped I/O
- Typical block diagram representing the interfacing between MP and I/O device.



Explain:

1. **Decoder**:
   - The low-order address bus (AB) is given as input to the decoder.
   - It generates a specific I/O address (IOADR) for the required I/O device.
2. **Gate Control**:
   - The decoder's output is combined with the control signals to enable data transfer.
   - It ensures that only the addressed I/O port is activated.
3. **I/O Port**:
   - It serves as an interface between the microprocessor and the input/output device.
   - It connects to an external input (IP) or output (OP) device.
4. **Control Logic (AND Gates)**:
   - IO/$\overline{M}$, R$\overline{D}$, and W$\overline{R}$ signals determine whether the operation is a read or write.
   - **IOR (I/O Read)**: Generated when IO/$\overline{M}$ = 1 and R$\overline{D}$ = 0, indicating a read operation from an input device.
   - **IOW (I/O Write)**: Generated when IO/$\overline{M}$ = 1 and W$\overline{R}$ = 0, indicating a write operation to an output device.
5. **Data Bus (DB)**:
   - Transfers data between the microprocessor and the I/O port.

How It Works:

1. **I/O Read Operation**:
   - The microprocessor places the I/O address on the address bus.
   - The decoder selects the corresponding I/O port.
   - The control logic confirms IOR to enable data transfer from the input device to the microprocessor.
2. **I/O Write Operation**:
   - The microprocessor places the I/O address on the address bus.
   - The decoder selects the corresponding I/O port.
   - The control logic confirms IOW, allowing data transfer from the microprocessor to the output device.

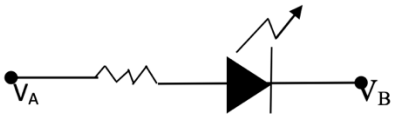
Peripheral- mapped	Memory- mapped
• I/O device is identified by 8 bit ($A_7 \longrightarrow A_0$) only i.e. 8085 MP can address 256 I/P 8256 O/P device.	• I/O device is identified by 16 bit (A15 ←A0) 8085 MP considers each device as a memory location.
• IOR & IOW are used to control the data transfer.	MEMR & MEMW are used to control the data transfer.
• IN & OUT instruction are used for programming.	• ALL memory related instructions for data transfer can be used e.g. MOV A, M, STA, LDA ….. etc.

BUS timing during the execution of IN & OUT instruction:

Ex. OUT FF Stored in M.L 2050 H, the content of Acc. Equals to (BBH)	• 2 byte instruction with opcode (D3)
	• During the execution of this instruction the content of register (A) is transferred to the O/P device through O/P port which is addressed by (FF)
	• Need O/P code fetch &memory read machine cycles for fetching part and I/O write machine cycle for execution part.

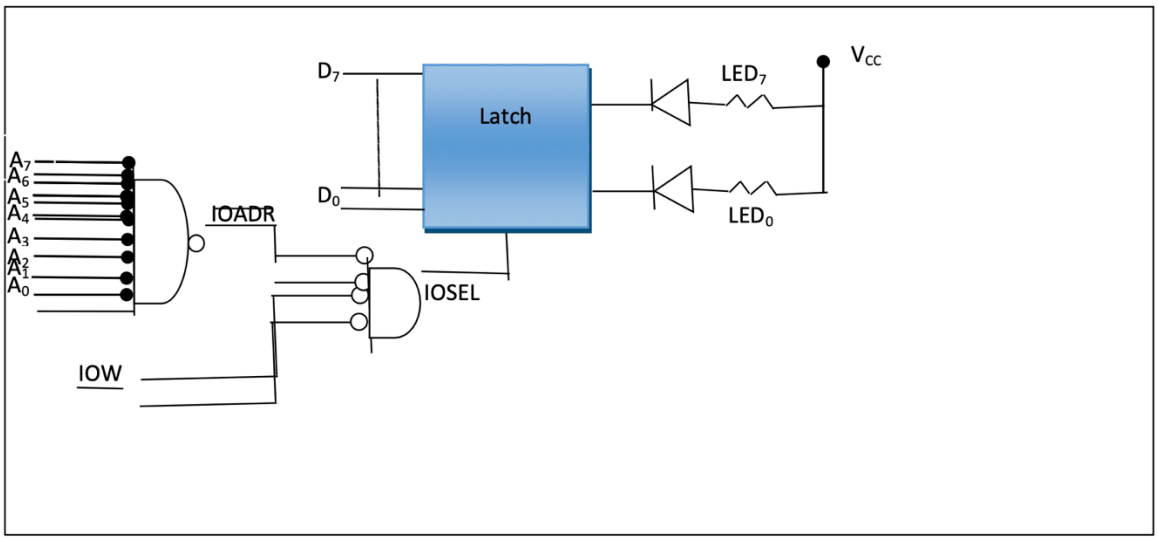
A. Interfacing O/P devices:

1. Lighting Emitting Diode (LED)



If $V_A > V_B$ ⟹ LED is in forward biasing ⟹ LED emits light ≡ logic (1)

Ex: Analyze the cct. Shown below:



Explanation of Components:

1. **Address Decoding (IOADR Generation)**:
   - The **low-order address bits (A0 to A7)** are provided as inputs to the **AND gate**.
   - This **AND gate** acts as a decoder, generating the **IOADR (I/O Address Recognition Signal)** when the specified address matches.
   - This ensures that only the intended I/O device is selected.
2. **Control Signal Generation (IOSEL - I/O Select)**:
   - The **IOW (I/O Write) signal** is combined with **IOADR** using another AND gate to generate **IOSEL**.
   - **IOSEL acts as an enabling signal** that activates the latch, allowing data transfer.
3. **Latch (Output Storage) for LED Control**:
   - The **latch stores the data (D0 to D7)** received from the microprocessor.
   - The stored data remains available even after the microprocessor moves on to other tasks.
   - This is crucial for output devices like LEDs, as they need to stay ON/OFF without continuous microprocessor intervention.
4. **LED Connection**:
   - Each **bit (D0 to D7) in the latch** corresponds to an LED.

- If a data bit is **high (1)**, the LED **turns ON**; if it is **low (0)**, the LED **turns OFF**.
- Current-limiting resistors are used to protect the LEDs.

5. **Power Supply (Vcc)**:
   - The LEDs are connected to **Vcc** and are controlled by the **latch outputs through transistors or drivers**.

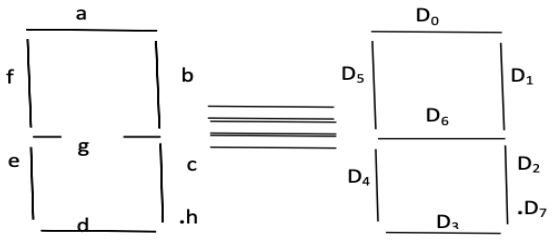
How It Works:

1. The **microprocessor sends an address** on the address bus.
2. The **decoder recognizes the address** and generates **IOADR**.
3. The microprocessor issues an **I/O Write (IOW) signal**.
4. The **AND gate combines IOADR and IOW** to generate **IOSEL**, enabling the latch.
5. The **latch captures the data from the data bus (D0 to D7)** and **holds it**.
6. The stored data **controls the LEDs**:

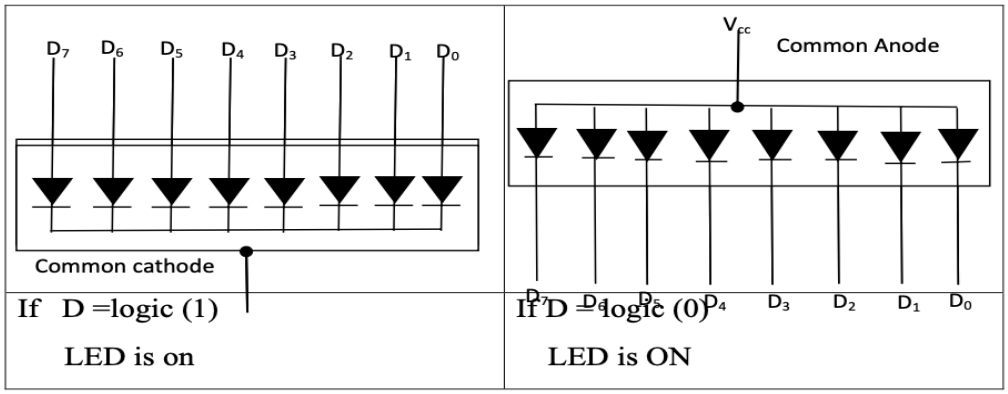
- A bit **1 (HIGH) → LED ON**.
- A bit **0 (LOW) → LED OFF**.

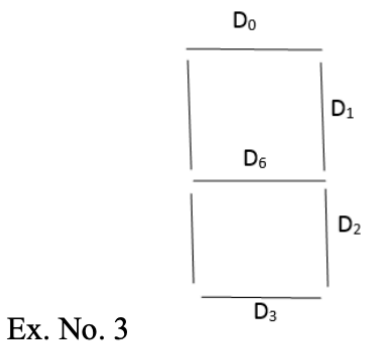
2. Segment Display:

Each segment is a LED



There are two types of 7segment display as below:-





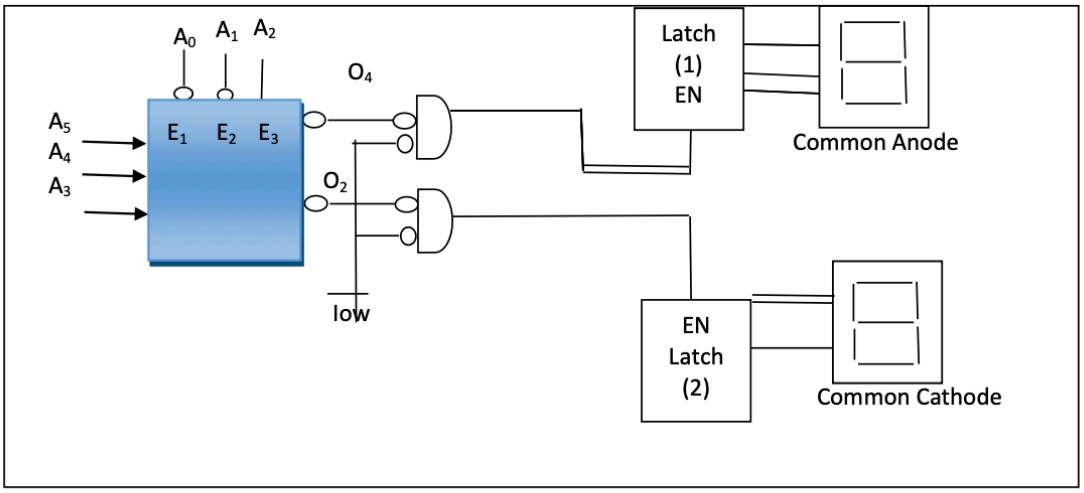
Ex. No. 3

DB= 4FH

Ex. No. 3

DB= BOH

Ex. What is the range of addresses, interfacing technique & type of decoding for each port in the following cct. What will be display if (Acc) = 06H



Sol: Both O/P port are interfaced through peripheral techniques both ports are identified by lines $A_7 \leftarrow A_0$.

Latch. (2)

Latch (2) can be address one of the following:

14H, 54H, 94H, D4H (linear decoding)

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X	X	0	1	0	1	0	0

Latch (1)

Latch (1) can be addressed by:

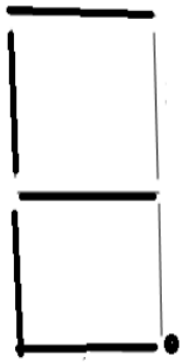
24H, 64H, A4H, E4H (linear decoding)

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X	X	1	0	0	1	0	0

To transfer (Acc) through latch (1)

MVI A,06

OUT 24 H, OUT A4H, OUT E4H, OUT 64H



E will be displayed

- To transfer (Acc) through latch (2), MVI A 06

  OUT 14, OUT 54, OUT 94, OUT D4

No. (1) will be displayed

The interfacing of Input Devices

- The basic concepts are similar to interfacing of output devices.
- The address lines are decoded to generate a signal that is active when the particular port is being accessed.
- An $IORD$ signal is generated by combining the IO/M and the RD signals from the microprocessor.
- A tri-state buffer is used to connect the input device to the data bus.
- The control (Enable) for these buffers is connected to the result of combining the address signal and the signal $IORD$.