

2nd term – Lecture No. & Lecture Name (Lec. 3- Microprocessor signals and machine cycle)

Microprocessor signals and machine cycle

Microprocessor signals

Microprocessor signals are the fundamental components that facilitate communication between the microprocessor and its external components, including memory, input/output devices, and peripheral units. These signals coordinate the operations of the microprocessor and enable it to interact with the system efficiently.

Types of Microprocessor Signals

Microprocessor signals can be broadly classified into the following categories:

- 1. Control Signals
- 2. Address Signals
- 3. Data Signals
- 4. Status Signals
- 5. Clock Signals

1. Control Signals

Control signals are used to manage and coordinate the operations of the microprocessor. These signals determine how the microprocessor interacts with memory, I/O devices, and other peripherals. Control signals are essential for the microprocessor to function properly.

Memory Read (RD):

Function: Activates the memory to read data from a specified memory location.

Signal Level: Typically, low (active low). When RD is active, it enables the data bus to carry the data from memory to the processor.

Memory Write (WR):

Function: Activates memory to write data to a specific memory location.

Signal Level: Typically, low (active low). When WR is activated, the data on the data bus is written to the address provided by the address bus.



Al-Mustaqbal University / College of Engineering & Technology Computer Techniques Department Stage 2 Subject (Microprocessor) / Code (UOMU022043)

Lecturer (Dr. Hussein Alkhamees)

2nd term – Lecture No. & Lecture Name (Lec. 3- Microprocessor signals and machine cycle)

I/O Read (IOR):

Function: Enables reading from an I/O device.

Signal Level: Typically, active low. When IOR is activated, it allows data to be transferred from the I/O device to the data bus.

I/O Write (IOW):

Function: Enables writing data to an I/O device.

Signal Level: Typically, active low. When IOW is activated, data on the data bus is written to an I/O device.

Interrupt Request (INT):

Function: Signals the processor that an interrupt is pending. It interrupts the current instruction cycle and forces the microprocessor to handle the interrupt.

Signal Level: Active low or high, depending on the system. A higher priority interrupt will often preempt a lower priority one.

Clock (CLK):

Function: Provides timing signals for synchronizing the operation of the microprocessor. Each clock pulse defines the time period for processing instructions.

Signal Level: Periodic waveform (square wave), typically oscillating between 0V and a higher voltage level.

Reset (RESET):

Function: Initializes or resets the microprocessor to its initial state, halting all operations and clearing internal registers.

Signal Level: Active low, used to restart the microprocessor from its reset state



2nd term – Lecture No. & Lecture Name (Lec. 3- Microprocessor signals and machine cycle)

2. Address Signals

Address signals are responsible for addressing memory locations and I/O ports. These signals define the specific location in memory or the I/O space the microprocessor wants to read from or write to.

Address Bus:

The address bus consists of several lines that carry the address of the memory or I/O location the processor wants to access.

The address bus width (e.g., 16-bit, 32-bit) determines how many locations the processor can address. For instance, a 16-bit address bus can address 65,536 locations (2^16), while a 32-bit address bus can address 4,294,967,296 locations (2³²).

Address Lines:

The microprocessor typically generates multiple address lines to specify the memory address. For example:

A0, A1, A2, ..., An represent address lines where n is the width of the address bus.

The address lines carry binary information to specify which memory or I/O location is being accessed.

3. Data Signals

Data signals are used to transfer actual data between the microprocessor and other components like memory and I/O devices.

Data Bus:

The data bus is a set of lines used to carry data to and from the microprocessor. Unlike the address bus, the data bus is bidirectional, meaning it can transfer data in both directions.

The width of the data bus (e.g., 8-bit, 16-bit, 32-bit) defines how much data can be transferred at a time. A wider data bus increases the throughput of the microprocessor.

Data lines (D0, D1, ..., Dn): These carry the data bits to and from the processor. If you have an 8-bit data bus, the data lines D0 to D7 would be used.



2nd term – Lecture No. & Lecture Name (Lec. 3- Microprocessor signals and machine cycle)

• Data Transfer:

Write Operation: The microprocessor sends data to memory or an I/O device by placing the data on the data bus and activating the appropriate control signal (e.g., WR or IOW).

Read Operation: The microprocessor retrieves data from memory or an I/O device by requesting the data to be placed on the data bus, usually triggered by a control signal (e.g., RD or IOR).

4. Status Signals

Status signals inform the microprocessor about the current state of the operation or the condition of the system.

• Zero Flag (Z):

Function: Indicates whether the result of the last arithmetic or logical operation was zero.

Signal Level: Active (set to 1) when the result is zero, inactive (set to 0) when the result is non-zero.

• Carry Flag (C):

Function: Indicates whether a carry occurred during an arithmetic operation.

Signal Level: Set to 1 if a carry-out occurred during addition, or if a borrow occurred during subtraction. It is used for multi-byte operations.

Sign Flag (S):

Function: Indicates whether the result of the last operation was negative (in two's complement representation).

Signal Level: Set to 1 if the result is negative.



2nd term – Lecture No. & Lecture Name (Lec. 3- Microprocessor signals and machine cycle)

Overflow Flag (O):

Function: Indicates whether an overflow occurred during an arithmetic operation. Overflow happens when the result of an operation exceeds the capacity of the processor's registers.

Signal Level: Set to 1 if overflow occurs.

• Parity Flag (P):

Function: Indicates whether the number of 1s in the result is odd or even.

Signal Level: Set to 1 if the number of 1s is even, and 0 if the number of 1s is odd.

5. Clock Signals

Clock signals play a crucial role in synchronizing the entire system. The clock signal provides a steady rhythm that the microprocessor uses to time its operations.

• Clock Pulse (CLK):

The clock is a periodic signal that governs when operations begin. The frequency of the clock determines how fast the microprocessor can process instructions (measured in Hz).

Each clock cycle corresponds to a unit of time, during which the microprocessor can perform specific operations. For instance, in an 8 MHz clock system, each clock cycle takes 125 nanoseconds.

• Phase:

In some systems, a **clock phase** is used to differentiate between the rising and falling edges of the clock signal. These edges dictate when the processor will read or write data.

6. Interaction of Signals

The control signals, address signals, and data signals work together to ensure that the microprocessor can perform its tasks effectively. For example, to fetch an instruction:

- The address of the instruction is placed on the address bus.
- The control signal triggers the memory to respond to the read command.
- The data bus carries the fetched instruction to the microprocessor.



2nd term – Lecture No. & Lecture Name (Lec. 3- Microprocessor signals and machine cycle)

Machine Cycle

A **machine cycle** refers to the sequence of operations a microprocessor performs to complete one instruction. The machine cycle is broken down into several steps and typically involves **fetching**, **decoding**, and **executing** the instruction. There are generally four main cycles involved in the operation of a microprocessor:

A. Fetch Cycle

- The **fetch cycle** is the first step in executing an instruction. The microprocessor fetches the instruction from memory.
- The address of the instruction is placed on the address bus, and the control signal tells the memory to send the instruction to the data bus.
- The instruction is then transferred to the instruction register for decoding.

B. Decode Cycle

- During the **decode cycle**, the microprocessor decodes the fetched instruction to understand what operation needs to be performed.
- The instruction is interpreted, and the microprocessor generates the necessary control signals to execute it.

C. Execute Cycle

- The **execute cycle** is the actual execution of the decoded instruction. This could involve:
 - ♦ Performing arithmetic or logical operations (ALU operations).
 - ♦ Transferring data between registers or memory locations.
 - ♦ Sending data to an output device.
- Depending on the instruction, it may require accessing memory, performing arithmetic, or interacting with I/O devices.

D. Memory/IO Access Cycle

- If the instruction involves reading or writing data from/to memory or I/O devices, the microprocessor performs the memory or I/O access cycle.
- During this cycle, the address of the location to be accessed is placed on the address bus, and the appropriate read or write control signals are asserted.