Lecturer: Dr. Hussam Jawad Kadhim AL_Janabi
Email: hussam.jawad@uomus.edu.iq

Lecture Seven

Counters

1- Asynchronous Counters

The term asynchronous refers to events that do not have a fixed time relationship with each other and, generally, do not occur at the same time. An asynchronous counter is one in which the flip-flops (FF) within the counter do not change states at exactly the same time because they do not have a common clock pulse.

A 2-bit Asynchronous Binary Counter

Figure 1 shows a 2-bit counter connected for asynchronous operation. Notice that the clock (CLK) is applied to the clock input (C) of *only* the first flip-flop, FF0, which is always the least significant bit (LSB). The second flip-flop, FF1, is triggered by the $\bar{Q}_0$ output of FF0. FF0 changes state at the positive-going edge of each clock pulse, but FF1 changes only when triggered by a positive-going transition of the $\bar{Q}_0$ output of FF0. Therefore, the two flip-flops are never simultaneously triggered, so the counter operation is asynchronous.

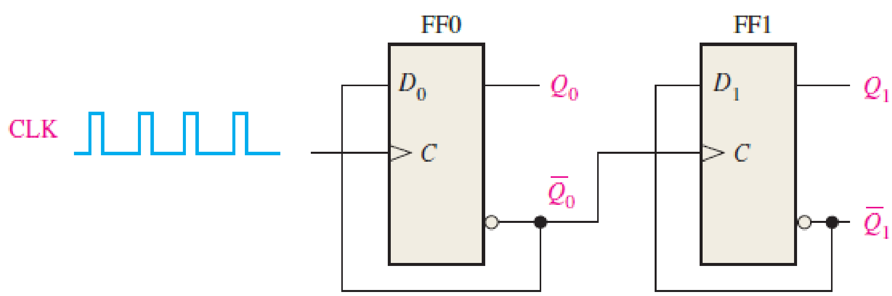


Figure 1

The Timing Diagram

Let's examine the basic operation of the asynchronous counter of Figure 1 by applying four clock pulses to FF0 and observing the Q output of each flip-flop. Figure 2 illustrates the changes in the state of the flip-flop outputs in response to the clock pulses. Both flip-flops are connected for toggle operation ($D = \bar{Q}$) and are assumed to be initially RESET (Q LOW).

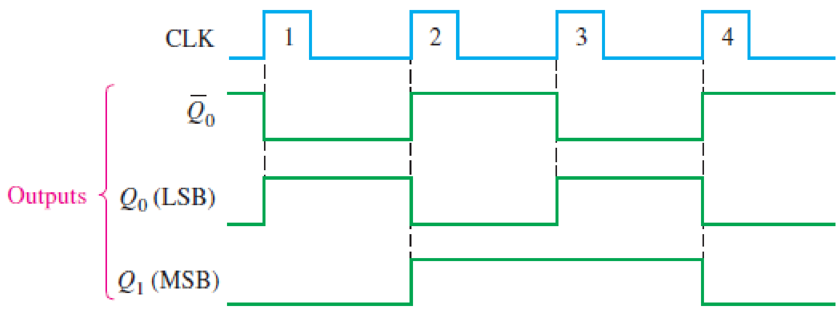


Figure 2

Table (1): The binary state sequence for the counter in Figure 1

Clock Pulse	Q_1	Q_2
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycle)	0	0

A 3-bit Asynchronous Binary Counter

The state sequence for a 3-bit binary counter is listed in Table 2, and a 3-bit asynchronous binary counter is shown in Figure 3(a). The basic operation is the same as that of the 2-bit

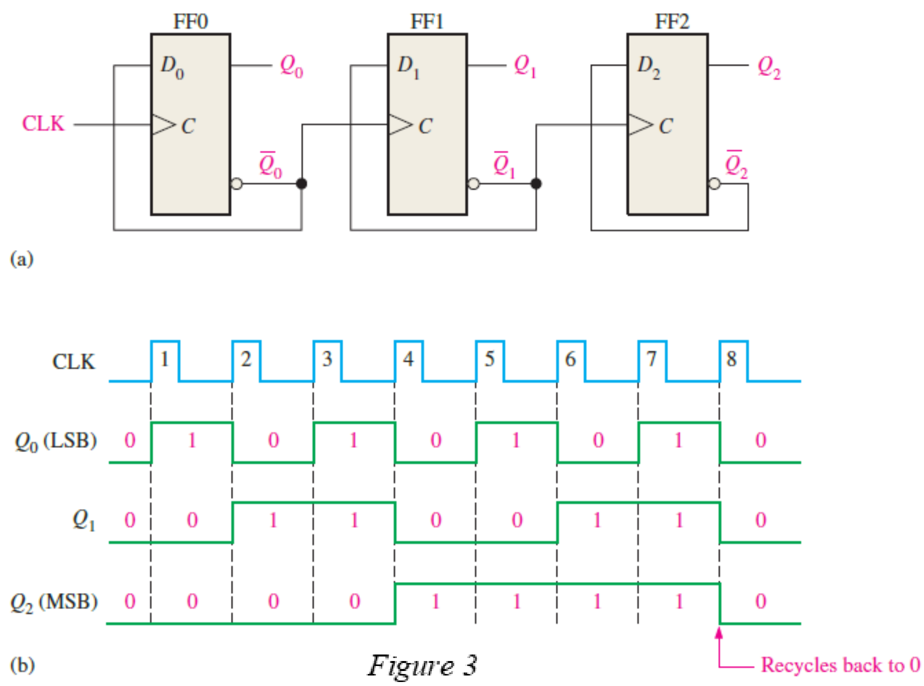


Figure 3

Table (2): State sequence for a 3-bit binary counter

Clock Pulse	Q2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycle)	0	0	0

Lecturer: Dr. Hussam Jawad Kadhim AL_Janabi
Email: hussam.jawad@uomus.edu.iq

Example (1)

Show how an asynchronous counter with J-K flip-flops can be implemented having a modulus of twelve with a straight binary sequence from 0000 through 1011.

Solution

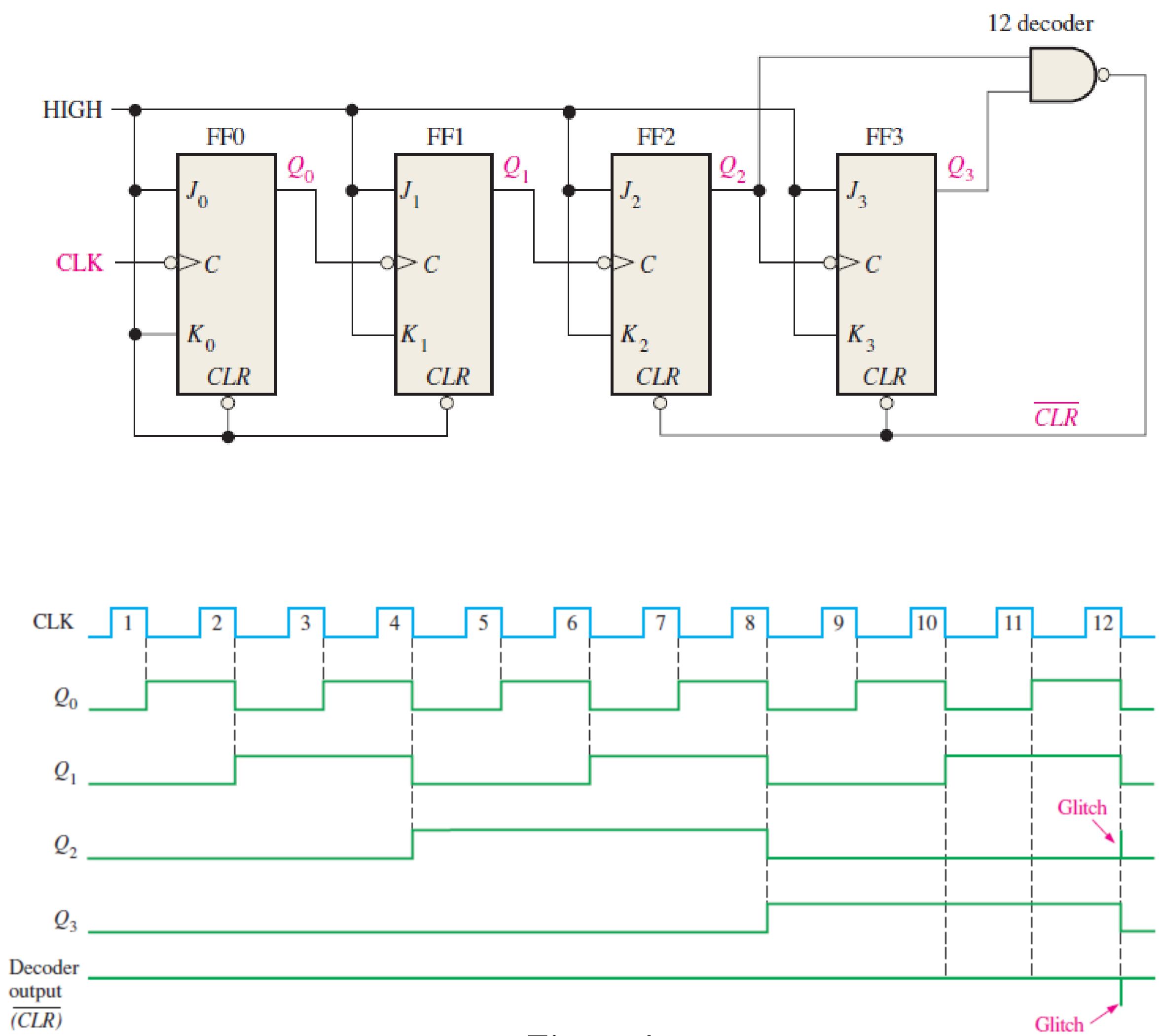


Figure 4

2- Synchronous Counters

The term **synchronous** refers to events that have a fixed time relationship with each other. J-K flip-flops are used to illustrate most synchronous counters.

A 2-Bit Synchronous Binary Counter

The operation of a J-K flip-flop synchronous counter is as follows:

First, assume that the counter is initially in the binary 0 state; that is, both flip-flops are RESET. When the positive edge of the first clock pulse is applied, FF0 will toggle and Q_0 will therefore go HIGH. What happens to FF1 at the positive-going edge of CLK1? To find out, let's look at the input conditions of FF1. Inputs J_1 and K_1 are both LOW because Q_0, to which they are connected, has not yet gone HIGH. Remember, there is a propagation delay from the triggering edge of the clock pulse until the Q output actually makes a transition. So, $J = 0$ and $K = 0$ when the leading edge of the first clock pulse is applied. This is a no-change condition, and therefore FF1 does not change state

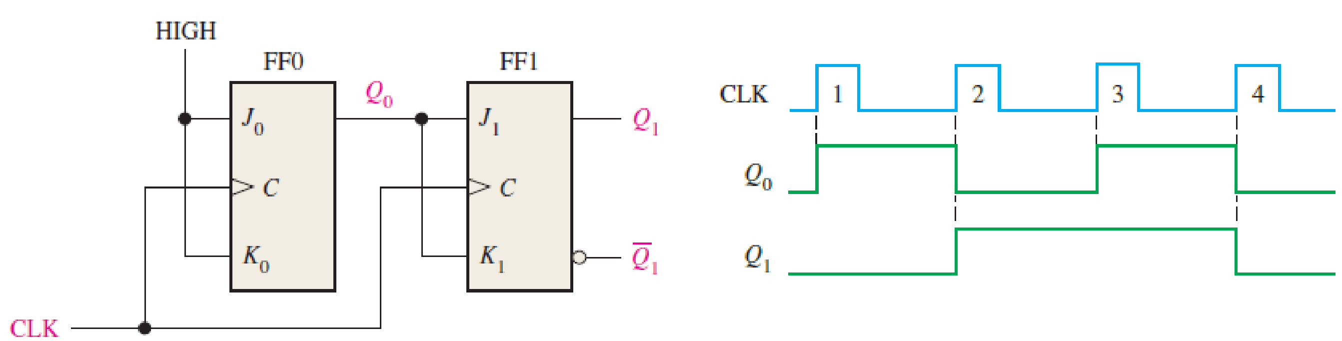
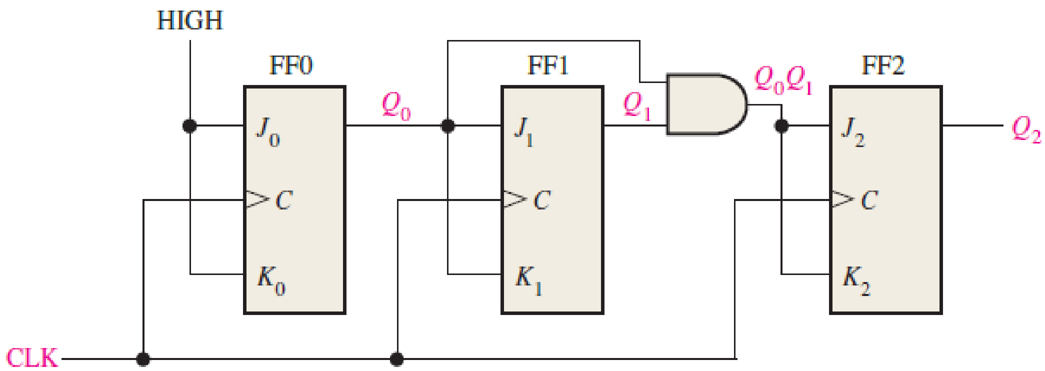
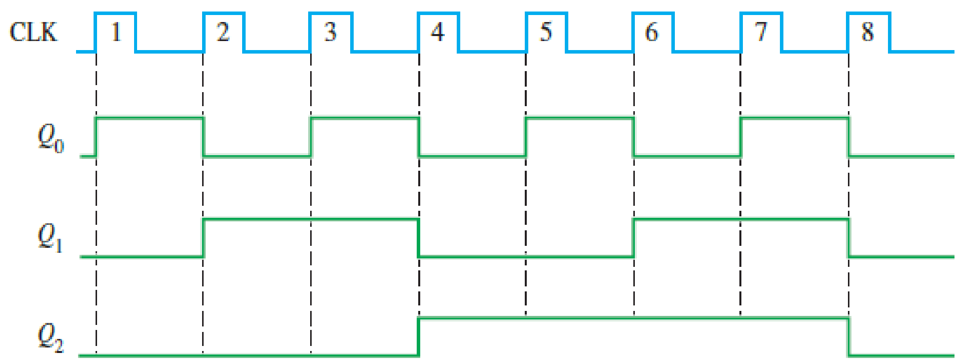


Figure 5

A 3-Bit Synchronous Binary Counter

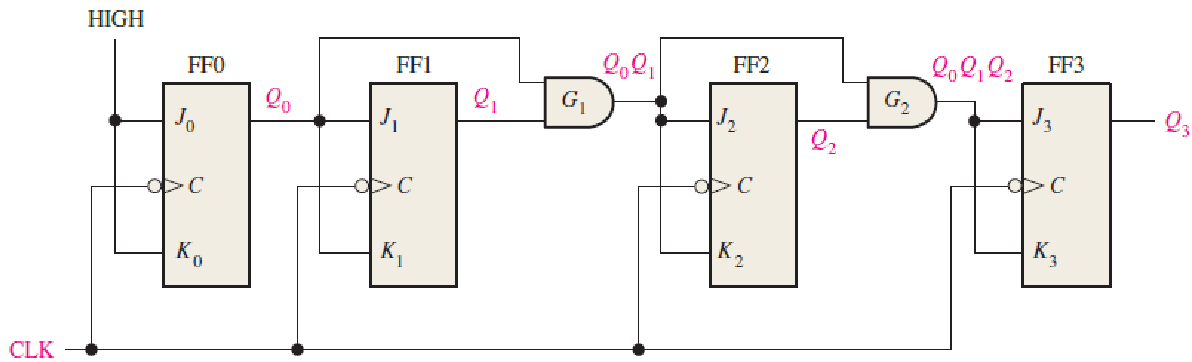


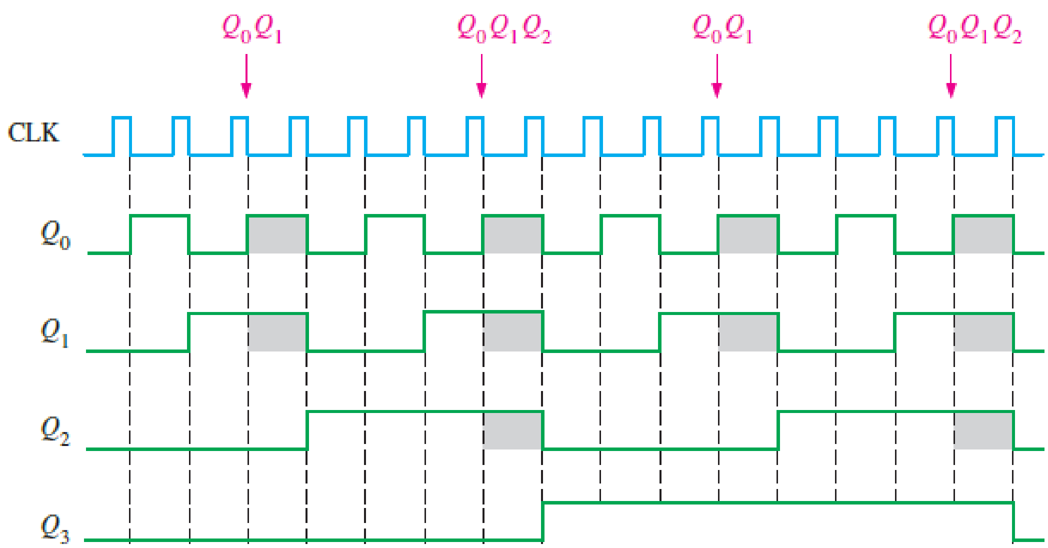


The state sequence for a 3-bit binary counter

Clock Pulse	Q2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

A 4-Bit Synchronous Binary Counter





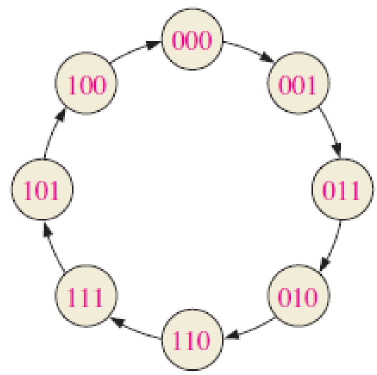
Lecturer: Dr. Hussam Jawad Kadhim AL_Janabi
Email: hussam.jawad@uomus.edu.iq

Design of Synchronous Counters

In this section, you will learn the six steps to design a counter (state machine).

Step 1: State Diagram

The first step in the design of a state machine (counter) is to create a state diagram. A state diagram shows the progression of states through which the counter advances when it is clocked.



Step 2: Next-State Table

Once the sequential circuit is defined by a state diagram, the second step is to derive a next-state table, which lists each state of the counter (present state) along with the corresponding next state. *The next state is the state that the counter goes to from its present state upon application of a clock pulse.* The next-state table is derived from the state diagram.

Next-state table for 3-bit Gray code counter.

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

Step 3: Flip-Flop Transition Table

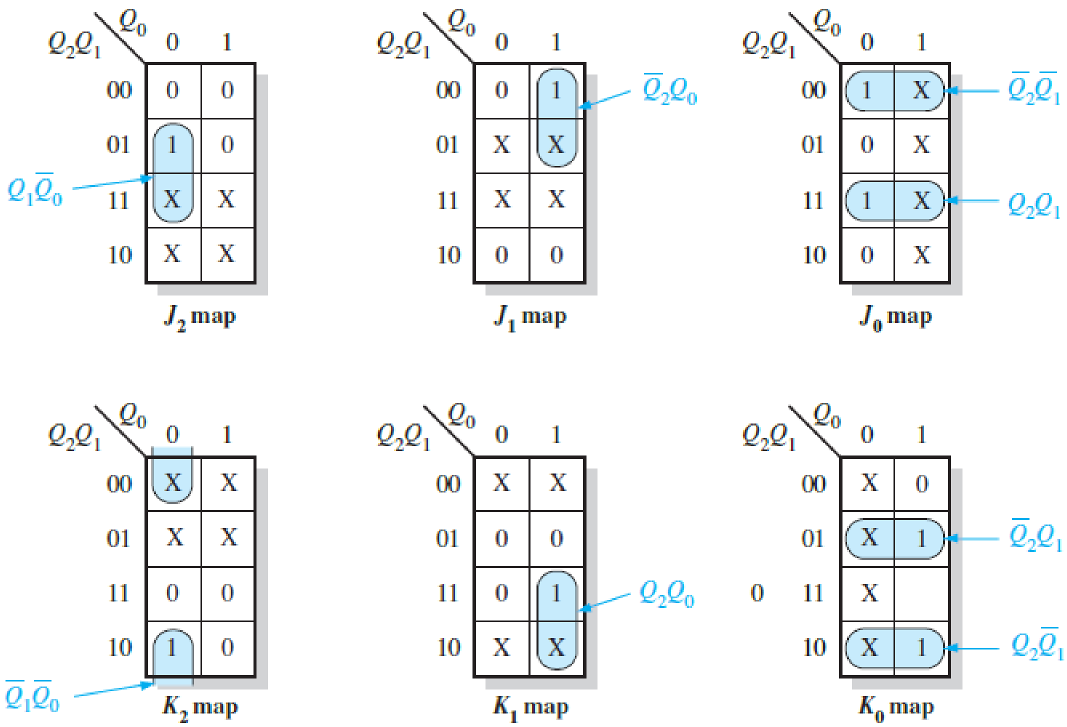
Table below is a transition table for the J-K flip-flop. All possible output transitions are listed by showing the *Q* output of the flip-flop going from the present states to the next states. Q_N is the present state of the flip-flop (before a clock pulse) and $QN + 1$ is the next state (after a clock pulse). For each output transition, the *J* and *K* inputs that will cause the transition to occur are listed. An X indicates a "don't care" (the input can be either a 1 or a 0).

Transition table for a J-K flip-flop

Output Transitions		Flip-Flop Inputs	
Q_n	Q_{n+1}	J	K
0 →	0	0	x
0 →	1	1	x
1 →	0	x	1
1 →	1	x	0

Step 4: Karnaugh Maps

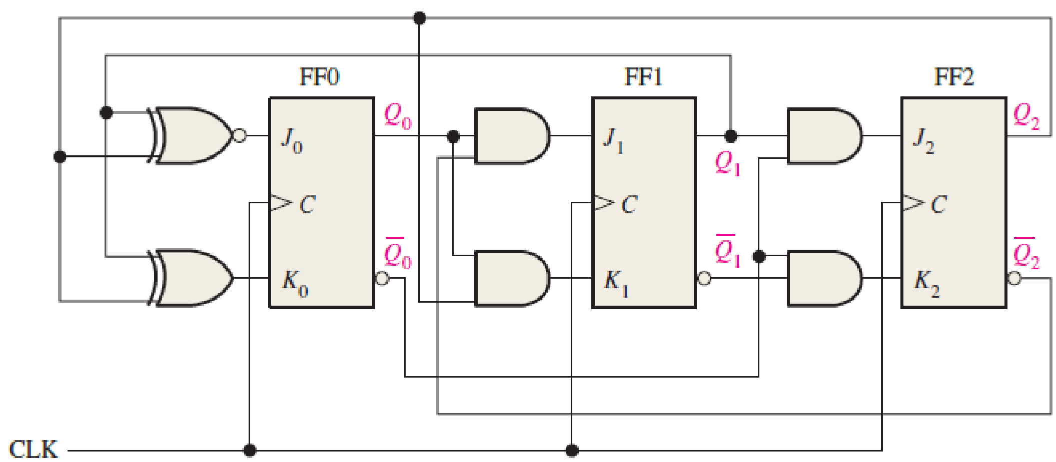
Karnaugh maps can be used to determine the logic required for the *J* and *K* inputs of each flip-flop in the counter. There is a Karnaugh map for the *J* input and a Karnaugh map for the *K* input of each flip-flop. In this design procedure, each cell in a Karnaugh map represents one of the present states in the counter sequence listed in the above table. From the *J* and *K* states in the transition table, a 1, 0, or X is entered into each present-state cell on the maps depending on the transition of the *Q* output for a particular flip-flop.



Step 5: Logic Expressions for Flip-Flop Inputs

$$J_0 = Q_2Q_1 + \overline{Q}_2\overline{Q}_1 = \overline{Q_2 \oplus Q_1}$$
$$K_0 = Q_2\overline{Q}_1 + \overline{Q}_2Q_1 = Q_2 \oplus Q_1$$
$$J_1 = \overline{Q}_2Q_0$$
$$K_1 = Q_2Q_0$$
$$J_2 = Q_1\overline{Q}_0$$
$$K_2 = \overline{Q}_1\overline{Q}_0$$

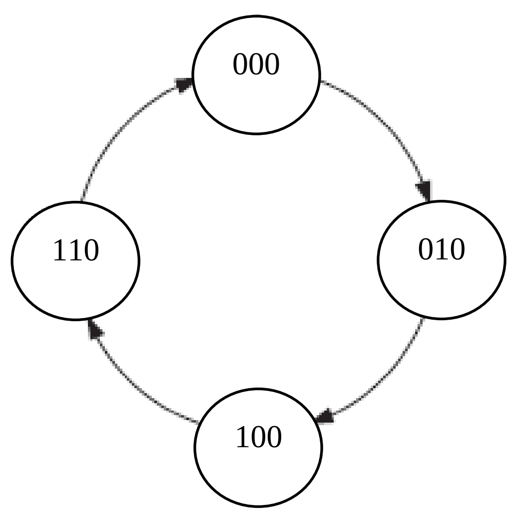
Step 6: Counter Implementation



Example: *Design a 3-bit synchronous even counter*

Solution

Step 1: State Diagram



Step 2: Next-State Table   *Step 3: Flip-Flop Transition Table*

Present State			Next State			J_2	K_2	J_1	K_1	J_0	K_0
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0						
0	0	0	0	1	0	0	x	1	x	0	x
0	1	0	1	0	0	1	x	x	1	0	X
1	0	0	1	1	0	x	0	1	x	0	X
1	1	0	0	0	0	x	1	x	1	0	X

Output Transitions		Flip-Flop Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Step 4: Karnaugh Maps and Step 5: Logic Expressions for Flip-Flop Inputs

Q_2Q_1 \ Q_0	0	1
00	0	X
01	1	X
11	X	X
10	X	X

$J_2 = Q_1$

00	X	X
01	X	X
11	1	X
10	0	X

$K_2 = Q_1$

00	1	X
01	X	X
11	X	X
10	1	X

$J_1 = 1$

00	X	X
01	1	X
11	1	X
10	X	X

$K_1 = 1$

00	0	X
01	0	X
11	0	X
10	0	X

$J_0 = 0$

00	X	X
01	X	X
11	X	X
10	X	X

$K_0 = 1$

Department of Biomedical Engineering
Digital Electronics / Third stage
Lecturer: Dr. Hussam Jawad Kadhim AL_Janabi
Email: hussam.jawad@uomus.edu.iq

Step 6: Counter Implementation