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**Department of Cyber Security**

**Subject:**

**MICROPROCESSORS**

**Lecture: (3)**

**8086 Internal Architecture**

**Class: Second**

**Lecturer: M.Sc.Muntather AL-mussawee**

# **8086 Microprocessor**

# It is a 16-bit Microprocessor (up). It's ALU, internal registers

# works with 16 bit binary word.

# 8086 has a 20 bit address bus can access up to = 1 MB memory

# locations.

# 8086 has a 16 bit data bus. It can read or write data to a

# memory/port either 16 bits or 8 bit at a time.

# It can support up to 64K I/O ports.

# Frequency range of 8086 is 6-10 MHz.

# It has multiplexed address and data bus ADO- AD15 and A16-

# A19.

# It can pre-fetch up to 6 instruction bytes from memory and queues

# them in order to speed up instruction execution.

# It requires +5V power supply.

# A 40 pin dual in line package.

# 8086 is designed to operate in two modes, Minimum mode and

# Maximum mode.

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# **8086 Internal Architecture:**

# Fig shows a block diagram of the 8086 internal architecture. It is

# internally divided into two separate functional units. These are the Bus

# Interface Unit (BIU) and the Execution Unit (EU). These two functional

# units independently, and it operate parallel at the same time

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# (BIU): Fetches instruction, reads and writes data, and computes the

# 20-bit address.

# (EU): Decode and executes the instruction using the 16-bit ALU.

# **BUS INTERFACE UNIT (BIU):**

# This unit consists of 4 sub-units which are:

# 1. Instruction queue.

# 2. Segment registers.

# 3. Instruction pointer.

# 4. Address adder.

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# **BUS INTERFACE UNIT (BIU) is responsible of the following:**

# full 16 bit bidirectional data bus and 20 bit address bus.

# connects the microprocessor to external devices. Instruction

# fetching.

# Reading and writing data of data operands for memory

# . Inputting/outputting data for input/output peripherals.

# functions related to instruction and data acquisition.

# The BIU uses a mechanism known as an instruction stream queue

# to implement pipeline architecture.

# 

# 

# **Execution Unit (EU):**

# This unit consists of 7 sub-units which are:

# 1. Control unite.

# 2. Instruction decoder.

# 3. Arithmetic and logical unit (ALU).

# 4. General register.

# 5. Flag register.

# 6. Pointers.

# 7. Index registers.

# **Execution Unit (EU) is responsible of the following:**

# The Execution unit is responsible for decoding and executing all

# instructions

# . It performs various arithmetic and logic operation over the data

# using unit (ALU).

# It coordinate of all other units of the processor using control unit.

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# **The EU mechanism as follows:**

# 1. EU extracts instructions from top of queue in BIU.

# 2. Decode the instruction.

# 3. Generates operands if necessary.

# 4. Passes operands to BIU and requests it to perform read or write bus

# cycles to memory or 1/0.

# 5. Perform the operation specified by the instruction on operands.

# 6. Branch or jump instruction

