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**Department of Cyber Security**

**Subject:**

**MICROPROCESSORS**

**Lecture: (2)**

**microprocessor**

**Class: Second**

**Lecturer: M.Sc.Muntather AL-mussawee**

**Microprocessor Pin**

**Address/Data bus**

Low order address bus

these are multiplexed with data.

When AD lines are used to transmit memory address the symbol A is used Instead at AD,

for example A0-A15

When data are transmitted over AD lines the symbol D ls used in place to AD,

for example D0-D7 D8-D15 or D0-D15

**AD16/S3 AD18/S5**

**AD17/S4 AD19/S6**

High order address bus

These are multiplexed with status signals

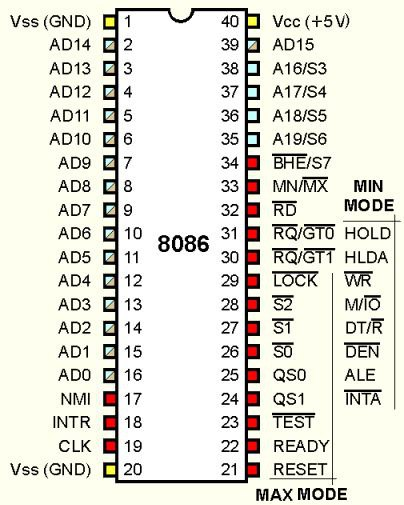
**34)** (Active Low)/S,(Output)

Bus High Enable/Status

It is used to enable data onto the most significant half of data bus,

D8-D15, 8-blt device connected to upper half of the data bus use (BHE)

(Active Low) signal. It is multiplexed with status signal S,.



**33) MN/**

MINIMUN/ MAXIMUN

This pin signal indicates what mode the processor is to operate in.

**32)**  (Read) (Active Low)

The signal is used for read operation.

It is an output signal

It is active when low.

**23)**

TEST Input is tested by the (WAIT) instruction.

8086 will enter a wait state after execution

of the WAIT instruction and will resume execution only when the TEST is made low by an active hardware.

This is used to synchropters an external

activity to the Processor internal operation.

**22) READY**

It is available at pin 22. It is an acknowledgement signal from I/O devices that data is transferred. It is an active high signal. When it is high, it indicates that the device is ready to transfer data. When it is low, it indicates wait state

**21) RESET** **(Input)**

Causes the processor to immediately terminate its present activity.

The signal must be active HIGH for at least four clock cycles.

**19) CLK**

Clock signal is provided through Pin-19. It provides timing to the processor for operations. Its frequency is different for different versions, i.e. 5MHz, 8MHz and 10MHz

**18) INTR Interrupt Request**

It is available at pin 18. It is an interrupt request signal, which is sampled during the last clock cycle of each instruction to determine if the processor considered this as an interrupt or not

**Min/ Max Pins**

The 8068 microprocessor can work in two modes of operations: Minimum mode and Maximum mode

In the minimum mode of operation the Microprocessor do not associate with any co-processors and can not be used for

multiprocessor systems

In the maximum mode the 8086 can work in multi-processor or

Co-processor configuration.

Minimum or maximum mode operations are decided by the

pin MN/ MX(Active low).

When this pin is high 8086 operates in minimum mode

otherwise it operates in Maximum mode.

**Minimum mode signals**

Pins 24-31

For minimum mode operation , the MN/ MX is tied

to VCC ( logic high)

8086 itself generates all the bus control signals

**27) DT/ R̅ (Data Transmit/ Receive)**

It stands for Data Transmit/Receive signal and is available at pin 27. It decides the direction of data flow through the trans receiver. When it is high, data is transmitted out and vice-a-versa

**26)**

(Data Enable) Output signal from the processer

used as output enable for the transceivers.

**25)**

(Address Latch Enable) Used to de multiplex the

address and data lines using external latches.

**28) M/**

Used to differentiate memory access and I/O access. for memory reference instructions, It is high. For IN and OUT instructions , It is Low

**29)**

Write control signal; asserted low Whenever processor writes data to memory or I/0 port.

**24)**

(interrupt Acknowledge) When the interrupt request is accepted by the processor , the output is low on this line.

**31) HOLD**

Input signal to the processor form the bus masters as a request to grant the control of the bus.

Usually used by the DMA controller to get the control of the bus.

**30) HLDA**

(hold Acknowledge) Acknowledge signal by the processor to the bus master requesting the central of the bas through HOLD.

The acknowledge is asserted High, when the

processor accepts HOLD.

**Maximum mode signals**

During maximum mode operation, the MN/ MX is grounded (logic low)

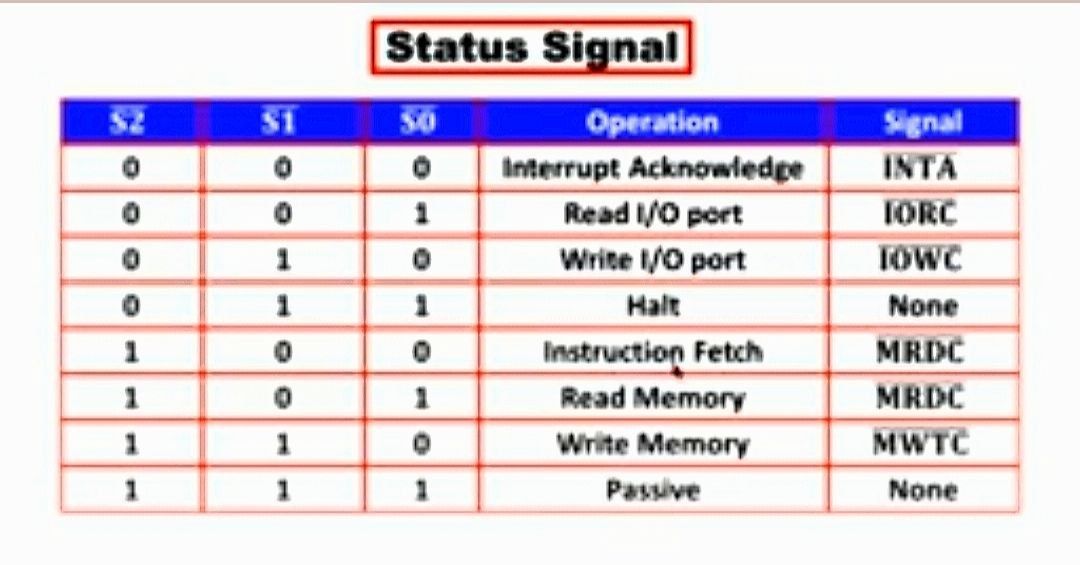
Pins 24--31 are reassigned

**, ,**

Status signals ; used by the 8086 bus controller to

generate bus timing and control signals. There are

decoded as shown :



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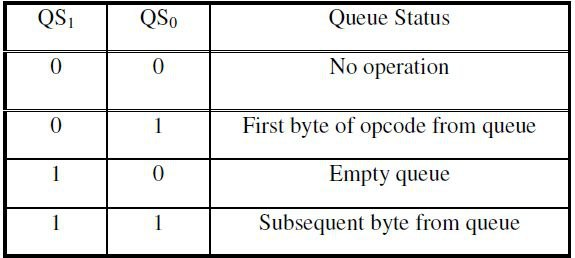
(Queue Status) The processer provides the status

of queue in these lines.

The queue status can be used by external device to

track the internal status of the queue in 8066.

The output on QS0 and QS1 can be interpreted as shown in the table



**/**

**/**

These are the Request/Grant signals used by the other processors requesting the CPU to release the system bus. When the signal is received by CPU, then it sends acknowledgment. RQ/GT0 has a higher priority than RQ/GT1.