Al-Mustaqbal University
Medical Instrumentation Techniques Engineering Department
المرحله : الثانية
اسم الماده : تقنيات رقمية
اسم المحاضر : مدرس جابر حميد

Flip-Flops

For

Second Class

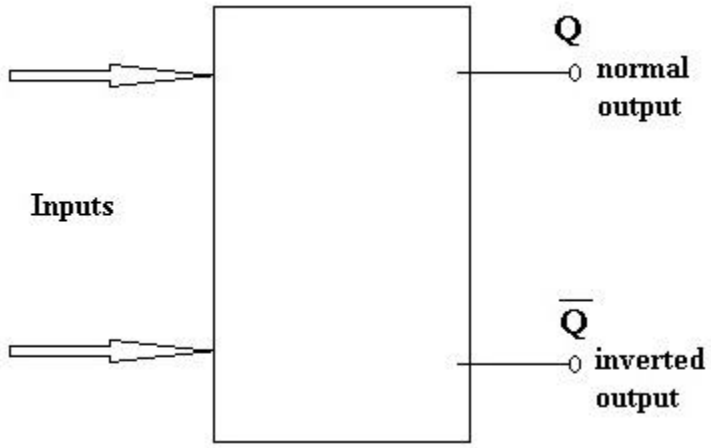
By l. Jaber hamed

Email **(jabber.hamed.majeed@uomus.edu.iq)**

Flip-Flops:-

Flip-flop(FF) is the most important memory element which is made up of an assembly of logic gates. Even though a logic gate, by itself, has no storage capability, several can be connected together in ways that permit information to be stored.

The general form of FF's is shown in the figure below

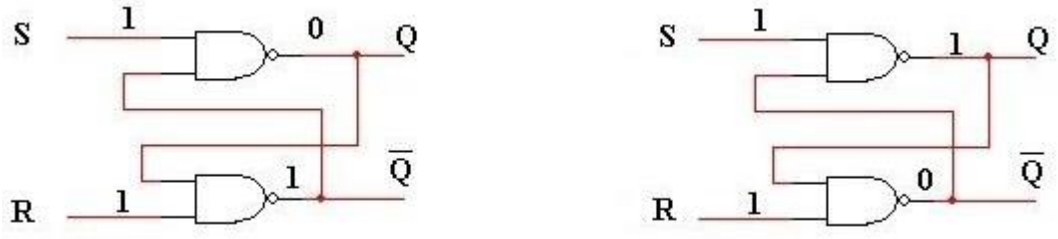


If : Q =1 $\bar{Q} = 0$ called High or 1 state, also called Set state.

If : Q =0 $\bar{Q} = 1$ called Low or 0 state, also called Reset state.

NAND Gate Latch:-

The most basic FF circuit can be constructed from either two NAND gated or two NOR gates. The NAND gate version, called a NAND gate latch or simply a latch, is shown in the figure below.

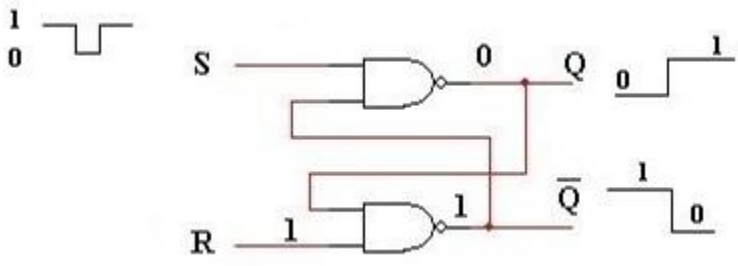


$S = R = 1$ (*reseting state*

The above figure shows the two possibility for resting case (the S and R are normally resting in High state).

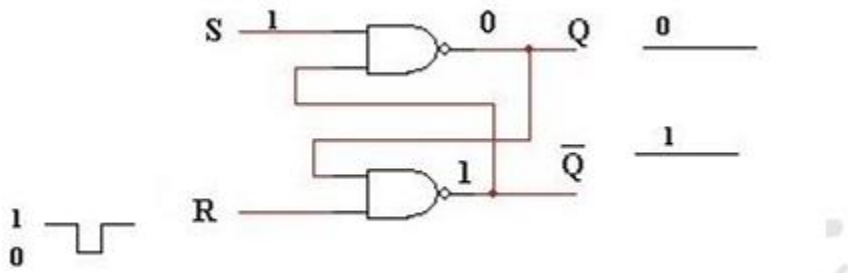
Setting the latch (FF) :-

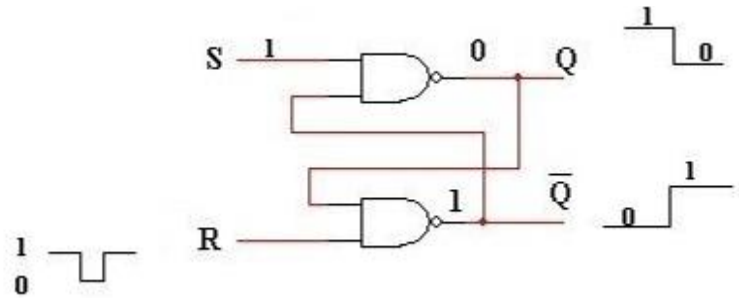
It is performed when the input S is momentarily pulsed Low while R is kept High as shown in the figure below.



Clearing the latch (FF) :-

It is performed when R input is pulsed Low while S is kept High. The following figure shows the two possibilities.

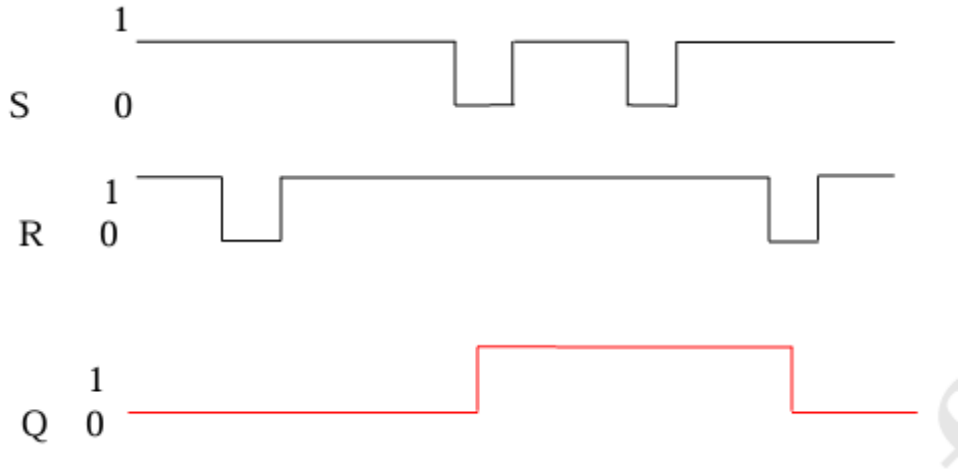




The operation described above can be conveniently in a truth table :

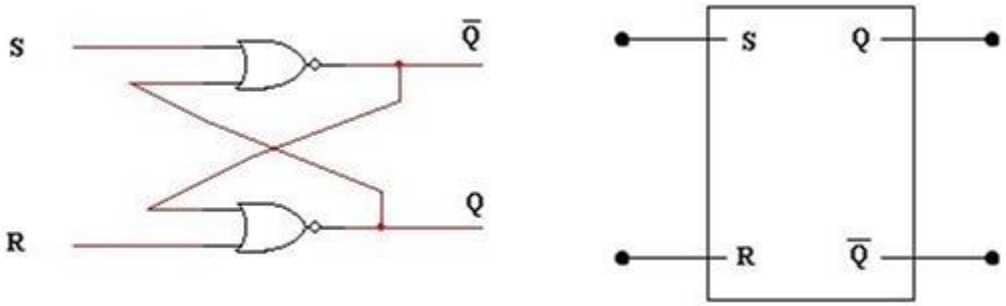
S	R	Q	$\overline{Q}$
0	0	No change	
0	1	1	0
1	0	0	1
1	1	Invalid produces $Q = \overline{Q}$ =1	

The waveforms shown below are applied to the NAND latch. Assume that initially Q=0, determine the Q waveform.



NOR Gate Latch FF:-

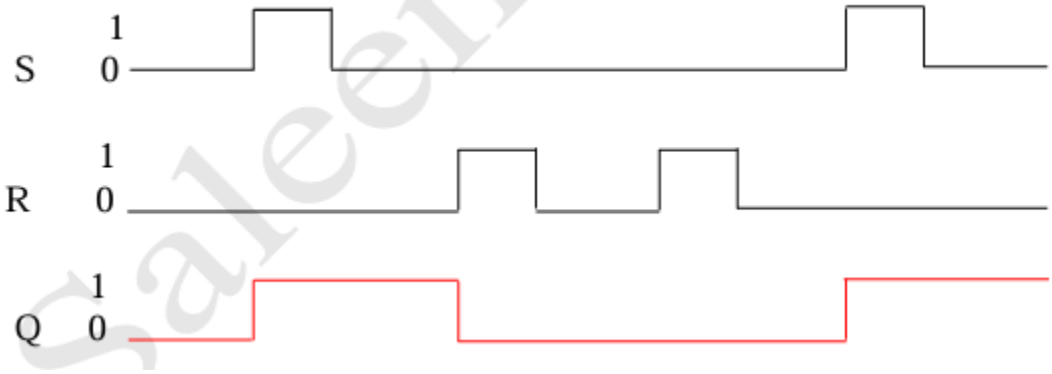
The arrangement of this latch (FF) is shown below :



S	R	Q
0	0	No change
0	1	0
1	0	1
1	1	invalid

Example :

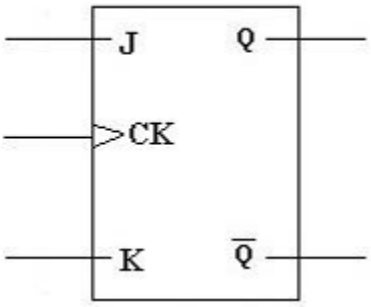
Assume that Q=0 initially, determine the Q waveform for the NOR latch with inputs shown below.



Clocked J-K FF :-

The JK flip-flop augments the behavior of the SR flip-flop (J=Set, K=Reset) by interpreting the S = R = 1 condition as a "flip" or toggle command. Specifically, the combination J = 1, K = 0 is a command to set the flip-flop; the combination J = 0, K = 1 is a command to reset the flip flop; and the combination J = K = 1 is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value.

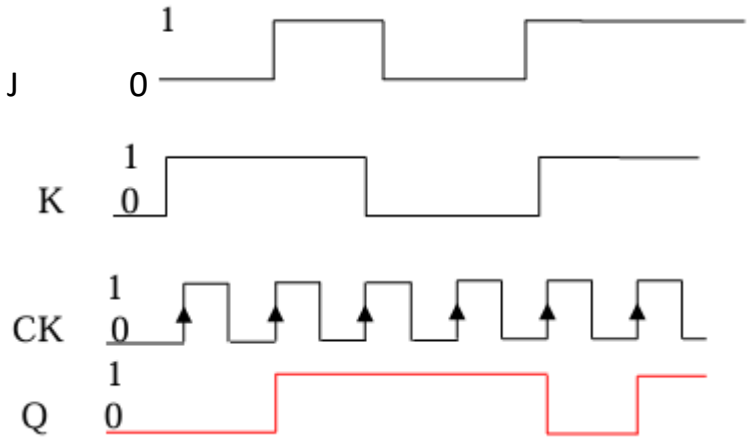
The figure below shows the symbol of J-K FF :-



A circuit symbol for a Positive edge triggered JK flip-flop, where > is the clock input, J and K are data inputs, Q is the stored data output, and Q' is the inverse of Q The characteristic equation of the JK flip-flop is:

$$Q_{next} = J\overline{Q} + \overline{K}Q$$

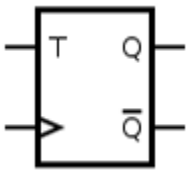
J	K	CK	Q
0	0	↑	Q_0(No change)
0	1	↑	0
1	0	↑	1
1	1	↑	$\overline{Q_0}$(Toggle)



T-type FF :-

A circuit symbol for a T-type flip-flop, where > is the clock input, T is the toggle input and Q is the stored data output. If the T input is high, the T flip-flop changes state ("toggles") whenever the clock input is strobed. If the T input is low, the flip-flop holds the previous value. This behavior is described by the characteristic equation :

$$Q_{next} = T \oplus Q = T\overline{Q} + \overline{T}Q$$



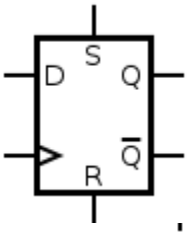
expanding the XOR operator and can be described in a truth table:

Characteristic table				Excitation table			
T	Q	Q_{next}	comment	Q	Q_{next}	T	comment
0	0	0	Hold state (no CLK)	0	0	0	No change
0	1	1	Hold state (no CLK)	1	1	0	No change
1	0	1	Toggle	0	1	1	Complement
1	1	0	Toggle	1	0	1	complement

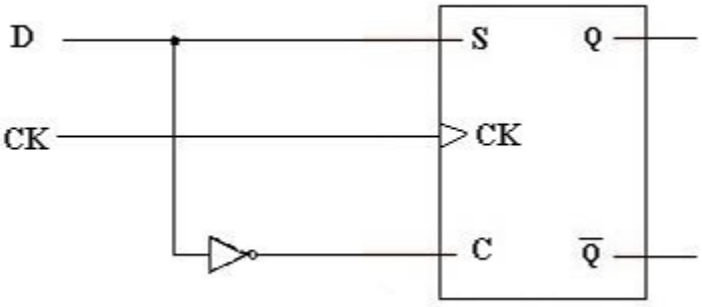
When T is held high, the toggle flip-flop divides the clock frequency by two; that is, if clock frequency is 4 MHz, the output frequency obtained from the flip-flop will be 2 MHz.

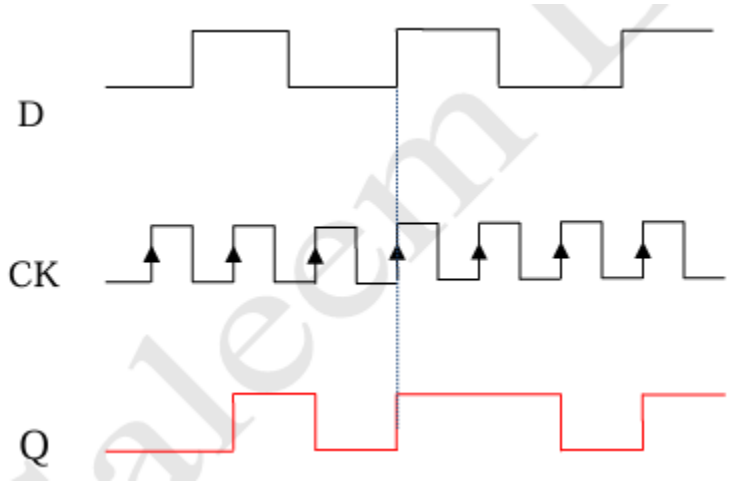
D (Delay) flip flop :

The figure below shows the symbol, truth table and internal circuit of D-FF.



D	CK	Q
0	↑	0
1	↑	1





The D flip-flop is the most common flip-flop in use today. It is better known as delay flip-flop (as its output Q looks like a delay of input D) or data latch.

The Q output takes on the state of the D input at the moment of a positive edge at the clock pin (or negative edge if the clock input is active low). It is called the D flip-flop for this reason, since the output takes the value of the D input or Data input, and Delays it by maximum one clock count.