Al-Mustaqbal University / College of Engineering & Technology
Department (Communication Technical Engineering) 1
Class (First)
Subject (ELECTRONIC CIRCUITS) / Code (UOMU028022)
Lecturer (Prof.Dr.Haider J Abd)
2nd term – Lecture No. & Lecture Name (Lec3: DC Biasing Circuits of BJTs)

DC Biasing Circuits of BJTs

Basic Concepts:

The analysis or design of a transistor amplifier requires a knowledge of both the dc and ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality, the improved output ac power level is the result of a transfer of energy from the applied dc supplies. The analysis or design of any electronic amplifier therefore has two components: the dc portion and the ac portion. Fortunately, the superposition theorem is applicable and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa.

The term ***biasing*** appearing in the title of this lecture is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an ***operating point*** on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the ***quiescent point*** (abbreviated ***Q***-point). By definition, ***quiescent*** means quiet, still, inactive. Fig. 9-1 shows a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the ***active region***.

Email (haider.jabber@uomus.edu.iq)

The maximum ratings are indicated on the characteristics of Fig. 9-1 by a horizontal line for the maximum collector current I_{Cmax} and a vertical line at the maximum collector-to-emitter voltage V_{CEmax}. The maximum power constraint is defined by the curve P_{Cmax} in the same figure. At the lower end of the scales are the ***cutoff region***, defined by $I_B \leq 0$ μA, and the ***saturation region***, defined by $V_{CE} \leq V_{CE(sat)}$.

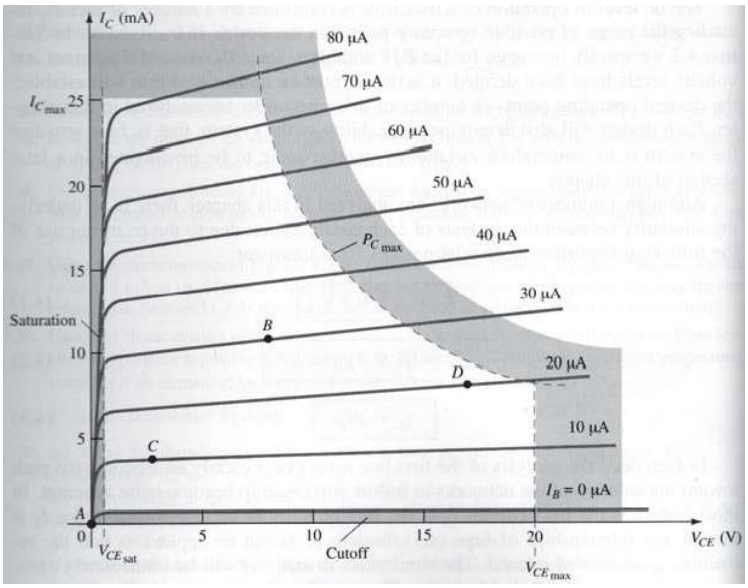


Fig. 9-1

Standard Biasing Circuits:

1. Fixed-Bias Circuit:

Fig. 9-2a shows a fixed-bias circuit.

Analysis:

◀ For the input (base-emitter circuit) loop as shown in Fig. 9-2b:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \qquad [9.1a]$$

◀ For the output (collector-emitter circuit) loop as shown in Fig. 9-2c:

$$I_C = \beta I_B$$

$$+V_{CE} + I_C R_C - V_{CC} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \qquad [9.1b]$$

◀ For the transistor terminal voltages:

$$\boxed{\begin{aligned} V_E &= 0V \\ V_B &= V_{CC} - I_B R_B = V_{BE} \\ V_C &= V_{CC} - I_C R_C = V_{CE} \end{aligned}} \qquad [9.1c]$$

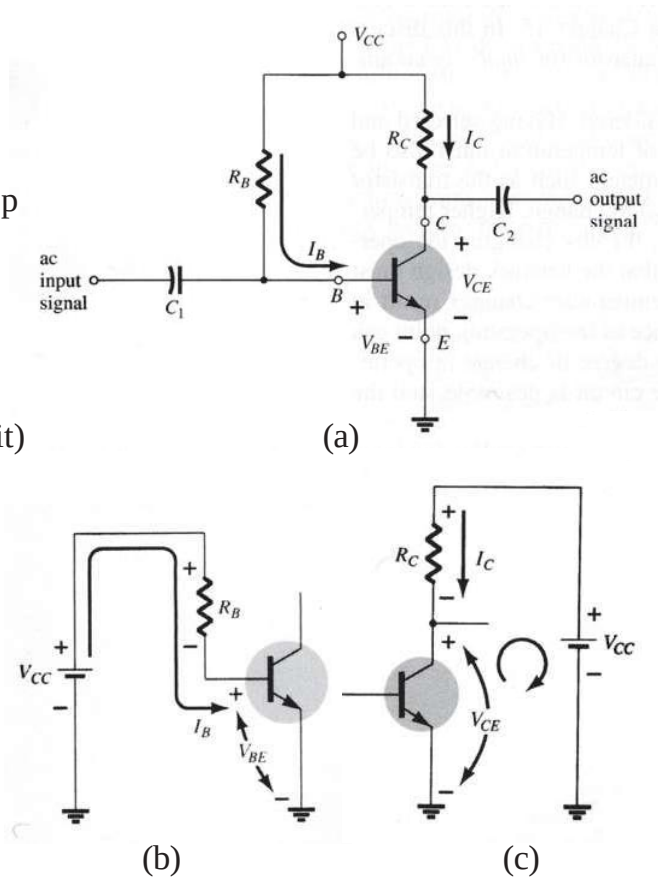


Fig. 9-2

Load-Line Analysis:

From Eq. [9.1b] and Fig. 9-3:

◀ At cutoff region:

$$\boxed{V_{CE} = V_{CC}\big|_{I_C=0}} \qquad [9.2a]$$

◀ At saturation region:

$$\boxed{I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE}=0}} \qquad [9.2b]$$

Design:

For an optimum design:

$$\boxed{\begin{aligned} V_{CEQ} &= \frac{1}{2}V_{CC} \\ I_{CQ} &= \frac{1}{2}I_{C(sat)} = \frac{V_{CC}}{2R_C} \end{aligned}} \qquad [9\text{-}3]$$

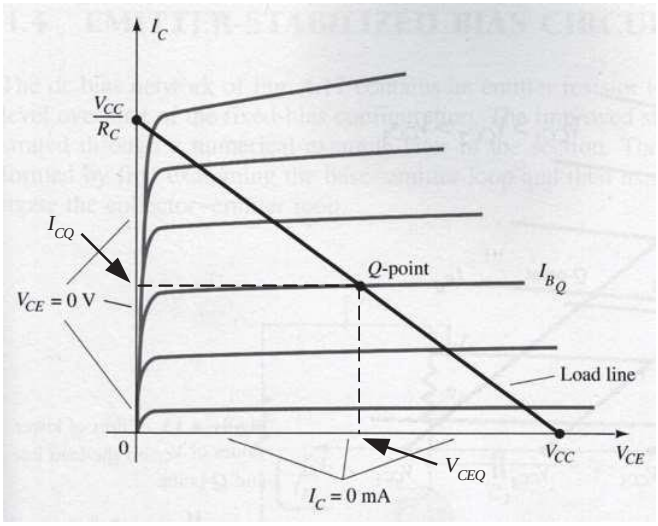


Fig. 9-3

2. Emitter-Stabilized Bias Circuit:

Fig. 9-4a shows an emitter-stabilized bias circuit.

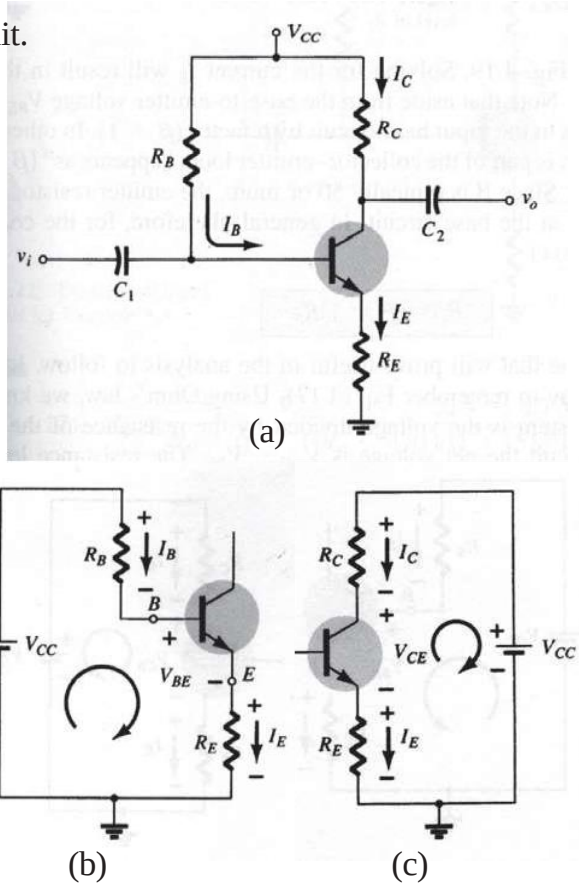


Fig. 9-4

Analysis:

◀ For the input (base-emitter circuit) loop as shown in Fig. 9-4b:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}} \qquad [9.4a]$$

◀ For the output (collector-emitter circuit) loop as shown in Fig. 9-4c:

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

$$I_E \cong I_C$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)} \qquad [9.4b]$$

◀ For the transistor terminal voltages:

$$\boxed{\begin{aligned} V_E &= I_E R_E \\ V_B &= V_{CC} - I_B R_B = V_E + V_{BE} \\ V_C &= V_{CC} - I_C R_C = V_E + V_{CE} \end{aligned}} \qquad [9.4c]$$

Load-Line Analysis:

From Eq. [9.4b] and Fig. 9-5:

◀ At cutoff region:

$$\boxed{V_{CE} = V_{CC}\big|_{I_C = 0}} \qquad [9.5a]$$

◀ At saturation region:

$$\boxed{I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0}} \qquad [9.5b]$$

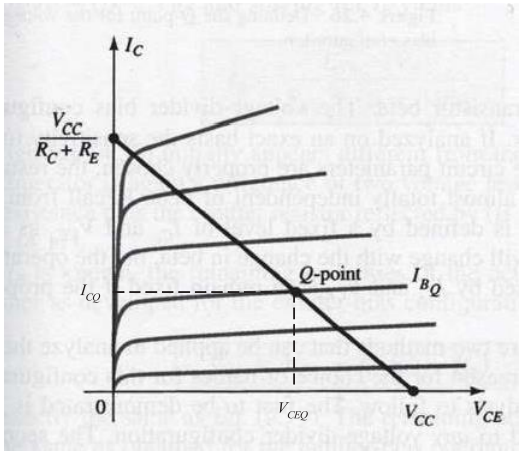


Fig. 9-5

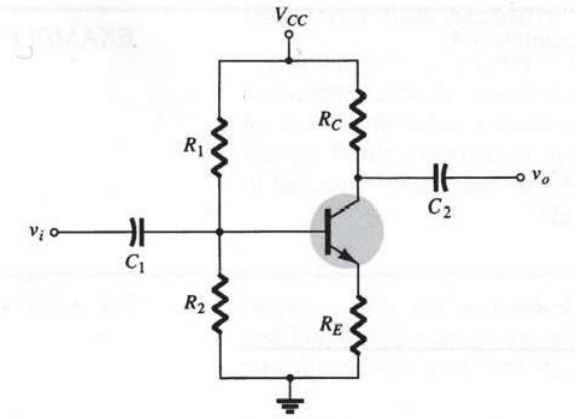
Design:

For an optimum design:

$$\boxed{\begin{aligned} V_{CEQ} &= \frac{1}{2} V_{CC} \\ I_{CQ} &= \frac{1}{2} I_{C(sat)} = \frac{V_{CC}}{2(R_C + R_E)} \\ V_E &= \frac{1}{10} V_{CC} \end{aligned}} \qquad [9\text{-}6]$$

3. Voltage-Divider Bias Circuit:

Fig. 9-6a shows a voltage-divider bias circuit.



(a)

Analyses:

◀ For the input (base-emitter circuit) loop:

Exact Analysis:

From Fig. 9-6b:

$$R_{Th} = R_1 \| R_2 \qquad [9.7a]$$

From Fig. 9-6c:

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \qquad [9.7b]$$

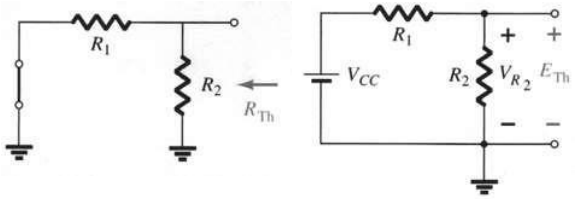
From Fig. 9-6d:

$$+E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E} \qquad [9.7c]$$

$$I_C = \beta I_B$$



(b) (c)

Approximate Analysis:

From Fig. 9-6e:

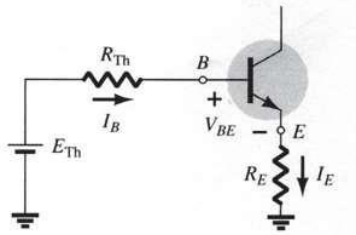
If $R_i >> R_2$ => $I_2 >> I_B$.

Since $I_B \approx 0$ => $I_1 \cong I_2$.

Thus R_1 in series with R_2.

That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \qquad [9.8a]$$



(d)

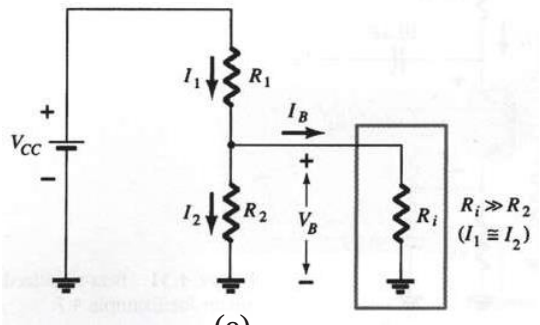
Since $R_i = (\beta + 1) R_E \underset{\cong \beta}{} R_E$ the condition that will define whether the approximation approach can be applied will be the following:

$$\beta R_E \geq 10 R_2 \qquad [9.8b]$$

and

$$V_E = V_B - V_{BE}$$

$$I_C \cong I_E = \frac{V_E}{R_E} \qquad [9.8c]$$



(e)

Fig. 9-6

◀ For the output (collector-emitter circuit) loop:

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \qquad [9.9]$$

Load-Line Analysis:

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 9-5. The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configuration.

Design:

For an optimum design:

$$V_{CEQ} = \frac{1}{2}V_{CC}$$

$$I_{CQ} = \frac{1}{2}I_{C(sat)} = \frac{V_{CC}}{2(R_C + R_E)}$$

$$V_E = \frac{1}{10}V_{CC}$$

$$R_2 \leq \frac{1}{10}\beta R_E$$

[9.10]

Example 9-1:

Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig. 9-6a with the following parameters: V_{CC} = +22 V, β = 140, R_1 = 39 kΩ, R_2 = 3.9 kΩ, R_C = 10 kΩ, and R_E = 1.5 kΩ.

Solution:

Exact:

$$R_{Th} = R_1 \| R_2 = 39k \| 3.9k = 3.55\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9k)(22)}{39k + 3.9k} = 2V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2 - 0.7}{3.55k + (141)(1.5k)} = 6.05\mu A$$

$$I_{CQ} = \beta I_B = (140)(6.05\mu) = 0.85mA$$

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$

$$= 22 - (0.85m)(10k + 1.5k)$$

$$= 12.23V$$

Approximate:

Testing: $\beta R_E \geq 10R_2$

$$(140)(1.5k) \geq 10(3.9k)$$

$$210k\Omega > 39k\Omega \quad \text{(satisfied)}$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9k)(22)}{39k + 3.9k} = 2V$$

$$V_E = V_B - V_{BE} = 2 - 0.7 = 1.3V$$

$$I_{CQ} = I_E = \frac{V_E}{R_E} = \frac{1.3}{1.5k} = 0.867mA$$

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$

$$= 22 - (0.867m)(10k + 1.5k)$$

$$= 12.03V$$