EXAMPLE 6.18

Determine I_{DQ}, V_{GSQ}, and V_{DS} for the *p*-channel JFET of Fig. 6.56.

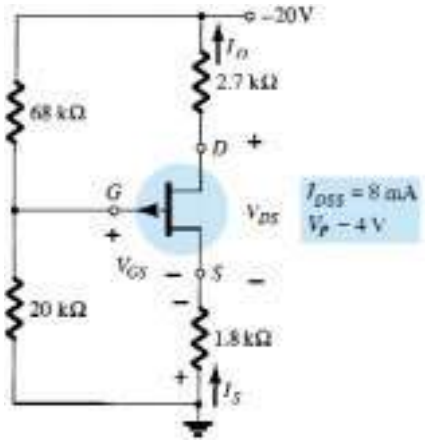

Figure 6.56 Example 6.18.

Solution

$$V_G = \frac{20\ \text{k}\Omega(-20\ \text{V})}{20\ \text{k}\Omega + 68\ \text{k}\Omega} = -4.55\ \text{V}$$

Applying Kirchhoff's voltage law gives

$$V_G - V_{GS} + I_D R_S = 0$$

and

$$V_{GS} = V_G + I_D R_S$$

Choosing $I_D = 0$ mA yields

$$V_{GS} = V_G = -4.55\ \text{V}$$

as appearing in Fig. 6.57.
Choosing $V_{GS} = 0$ V, we obtain

$$I_D = -\frac{V_G}{R_S} = -\frac{-4.55\ \text{V}}{1.8\ \text{k}\Omega} = 2.53\ \text{mA}$$

as also appearing in Fig. 6.57.
The resulting quiescent point from Fig. 6.57:

$$I_{DQ} = \mathbf{3.4\ mA}$$
$$V_{GSQ} = \mathbf{1.4\ V}$$

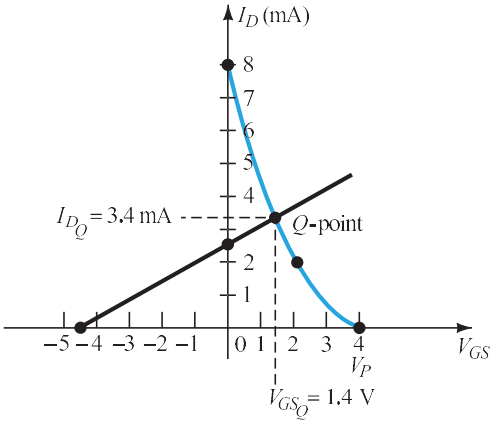

Figure 6.57 Determining the *Q*-point for the JFET configuration of Fig. 6.56.

For V_{DS}, Kirchhoff's voltage law will result in

$$-I_D R_S + V_{DS} - I_D R_D + V_{DD} = 0$$

and

$$\begin{aligned} V_{DS} &= -V_{DD} + I_D(R_D + R_S) \\ &= -20\text{ V} + (3.4\text{ mA})(2.7\text{ k}\Omega + 1.8\text{ k}\Omega) \\ &= -20\text{ V} + 15.3\text{ V} \\ &= \mathbf{-4.7\text{ V}} \end{aligned}$$

6.12 UNIVERSAL JFET BIAS CURVE

Since the dc solution of a FET configuration requires drawing the transfer curve for each analysis, a universal curve was developed that can be used for any level of I_{DSS} and V_P. The universal curve for an *n*-channel JFET or depletion-type MOSFET (for negative values of V_{GS_Q}) is provided in Fig. 6.58. Note that the horizontal axis is not that of V_{GS} but of a normalized level defined by $V_{GS}/|V_P|$, the $|V_P|$ indicating that only the magnitude of V_P is to be employed, not its sign. For the vertical axis, the scale is also a normalized level of I_D/I_{DSS}. The result is that when $I_D = I_{DSS}$, the ratio is 1, and when $V_{GS} = V_P$, the ratio $V_{GS}/|V_P|$ is -1. Note also that the scale for I_D/I_{DSS} is on the left rather than on the right as encountered for I_D in past exercises. The additional two scales on the right need an introduction. The vertical scale labeled *m* can in itself be used to find the solution to fixed-bias configurations. The other scale, labeled *M*, is employed along with the *m* scale to find the solution

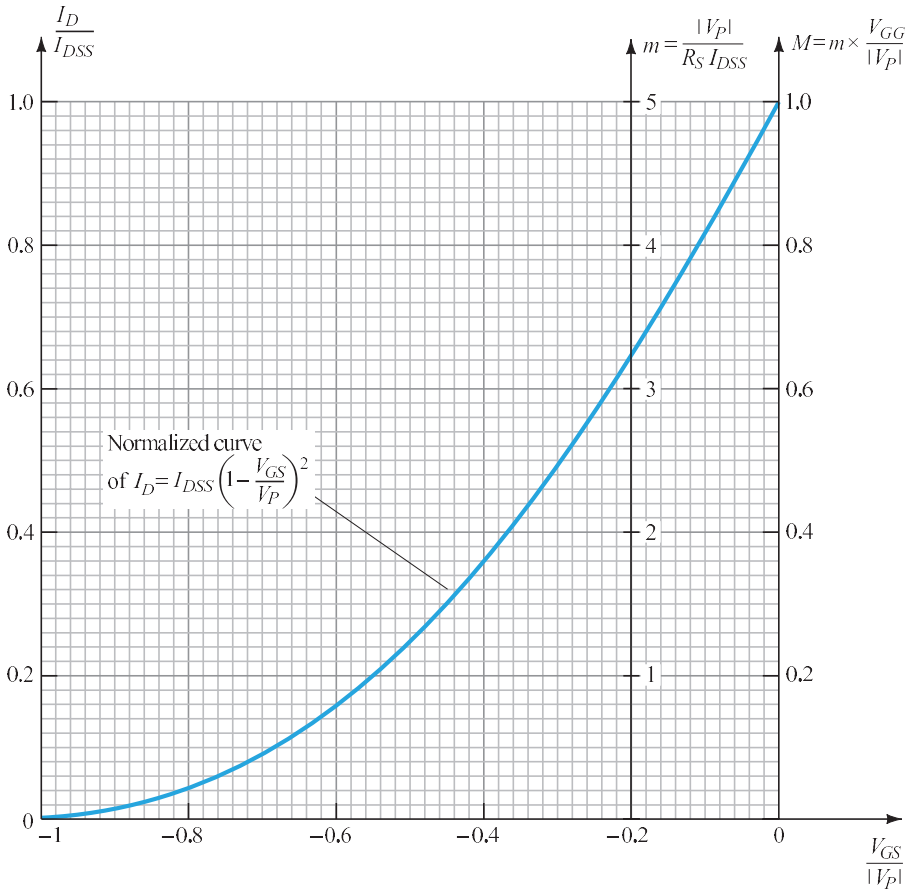

Figure 6.58 Universal JFET bias curve.

to voltage-divider configurations. The scaling for m and M come from a mathematical development involving the network equations and normalized scaling just introduced. The description to follow will not concentrate on why the m scale extends from 0 to 5 at $V_{GS}/|V_P| = -0.2$ and the M scale from 0 to 1 at $V_{GS}/|V_P| = 0$ but rather on how to use the resulting scales to obtain a solution for the configurations. The equations for m and M are the following, with V_G as defind by Eq. (6.15).

$$m = \frac{|V_P|}{I_{DSS}R_S} \tag{6.35}$$

$$M = m \times \frac{V_G}{|V_P|} \tag{6.36}$$

with $$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Keep in mind that the beauty of this approach is the elimination of the need to sketch the transfer curve for each analysis, that the superposition of the bias line is a great deal easier, and that the calculations are fewer. The use of the m and M axes is best described by examples employing the scales. Once the procedure is clearly understood, the analysis can be quite rapid, with a good measure of accuracy.

EXAMPLE 6.19

Determine the quiescent values of I_D and V_{GS} for the network of Fig. 6.59.

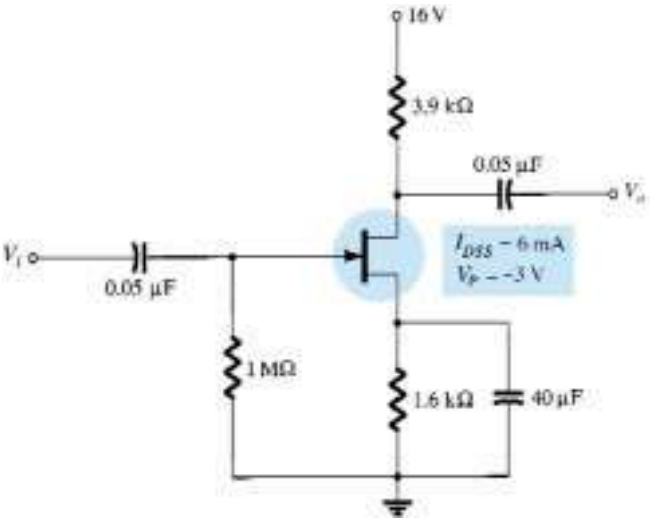

Figure 6.59 Example 6.19.

Solution

Calculating the value of m, we obtain

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-3\text{ V}|}{(6\text{ mA})(1.6\text{ k}\Omega)} = 0.31$$

The self-bias line defined by R_S is plotted by drawing a straight line from the origin through a point defined by $m = 0.31$, as shown in Fig. 6.60.
The resulting Q-point:

$$\frac{I_D}{I_{DSS}} = 0.18 \quad \text{and} \quad \frac{V_{GS}}{|V_P|} = -0.575$$

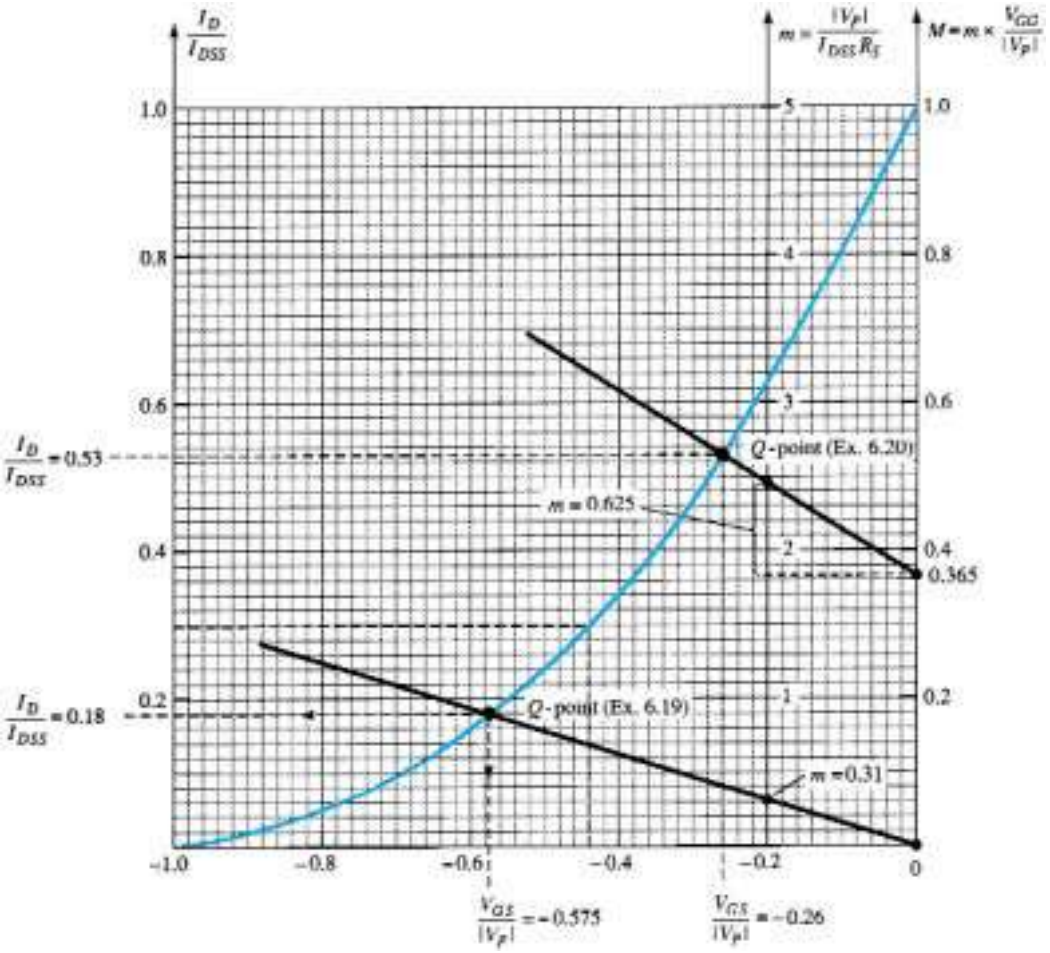

Figure 6.60 Universal curve for Examples 6.19 and 6.20.

The quiescent values of I_D and V_{GS} can then be determined as follows:

$$I_{D_Q} = 0.18I_{DSS} = 0.18(6\text{ mA}) = \mathbf{1.08\text{ mA}}$$

and

$$V_{GS_Q} = -0.575\,|V_P| = -0.575(3\text{ V}) = \mathbf{-1.73\text{ V}}$$

EXAMPLE 6.20

Determine the quiescent values of I_D and V_{GS} for the network of Fig. 6.61.

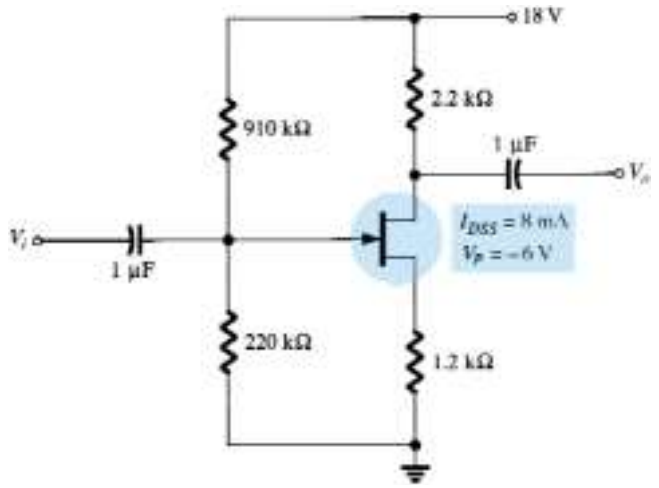

Figure 6.61 Example 6.20.

Solution

Calculating m gives

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-6\text{ V}|}{(8\text{ mA})(1.2\text{ k}\Omega)} = 0.625$$

Determining V_G yields

$$V_G = \frac{R_2V_{DD}}{R_1 + R_2} = \frac{(220\text{ k}\Omega)(18\text{ V})}{910\text{ k}\Omega + 220\text{ k}\Omega} = 3.5\text{ V}$$

Finding M, we have

$$M = m \times \frac{V_G}{|V_P|} = 0.625\left(\frac{3.5\text{ V}}{6\text{ V}}\right) = 0.365$$

Now that m and M are known, the bias line can be drawn on Fig. 6.60. In particular, note that even though the levels of I_{DSS} and V_P are different for the two networks, the same universal curve can be employed. First find M on the M axis as shown in Fig. 6.60. Then draw a horizontal line over to the m axis and, at the point of intersection, add the magnitude of m as shown in the figure. Using the resulting point on the m axis and the M intersection, draw the straight line to intersect with the transfer curve and define the Q-point:

That is, $\dfrac{I_D}{I_{DSS}} = 0.53$ and $\dfrac{V_{GS}}{|V_P|} = -0.26$

and $I_{D_Q} = 0.53I_{DSS} = 0.53(8\text{ mA}) = \mathbf{4.24\text{ mA}}$

with $V_{GS_Q} = -0.26|V_P| = -0.26(6\text{ V}) = \mathbf{-1.56\text{ V}}$

6.13 PSPICE WINDOWS

JFET Voltage-Divider Configuration

The results of Example 6.20 will now be verified using PSpice Windows. The network of Fig. 6.62 is constructed using computer methods described in the previous chapters. The J2N3819 JFET is obtained from the **EVAL.slb** library and, through **Edit-Model-Edit Instance Model (Text), Vto** is set to −6V and **Beta,** as defined by Beta = $I_{DSS}/|V_P|^2$ is set to 0.222 mA/V^2. After an **OK** followed by clicking the **Simulation** icon (the yellow background with the two waveforms) and clearing the **Message Viewer, PSpiceAD** screens will result in Fig. 6.62. The resulting drain cur-

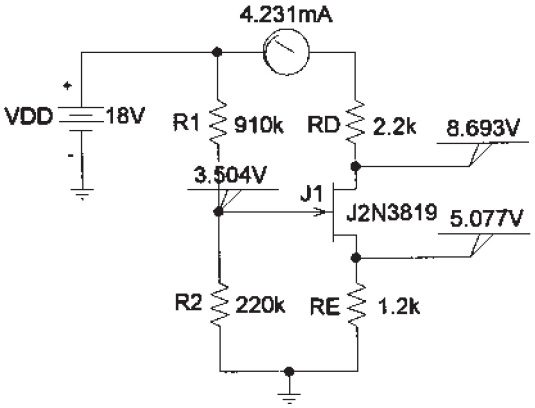

Figure 6.62 JFET voltage-divider configuration with PSpice Windows results for the dc levels.

rent is 4.231 mA compared to the calculated level of 4.24 mA, and V_{GS} is 3.504 V − 5.077 V = −1.573 V versus the calculated value of −1.56 V—both excellent comparisons.

Combination Network

Next, the results of Example 6.13 with both a transistor and JFET will be verified. For the transistor, the **Model** must be altered to have a **Bf**(beta) of 180 to match the example, and for the JFET, **Vto** must be set to −6V and **Beta** to 0.333 mA/V^2. The results appearing in Fig. 6.63 are again an excellent comparison with the hand-written solution. V_D is 11.44 V compared to 11.07 V, V_C is 7.138 V compared to 7.32 V, and V_{GS} is −3.758 V compared to −3.7 V.

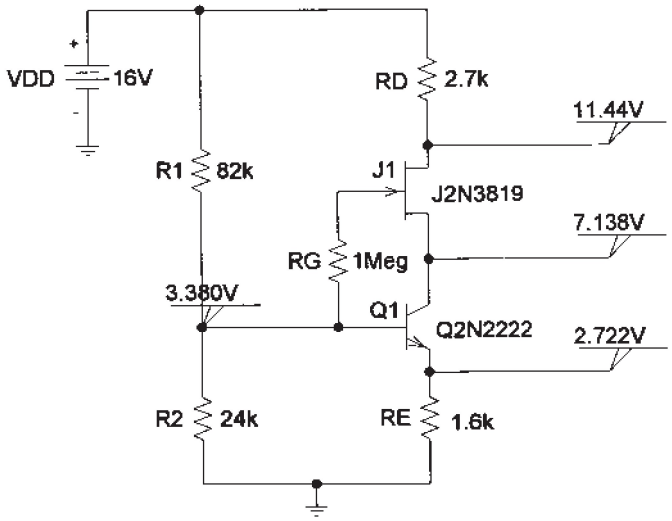

Figure 6.63 Verifying the hand-calculated solution of Example 6.13 using PSpice Windows.

Enhancement MOSFET

Next, the analysis procedure of Section 6.6 will be verified using the IRF150 enhancement-type *n*-channel MOSFET found in the **EVAL.slb** library. First, the device characteristics will be obtained by constructing the network of Fig. 6.64.

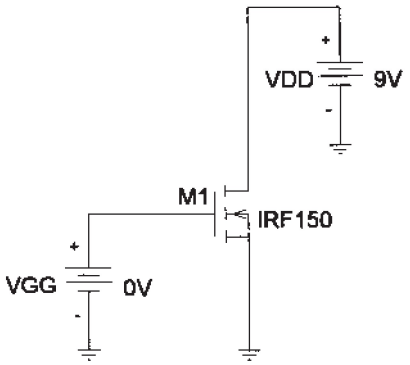

Figure 6.64 Network employed to obtain the characteristics of the IRF150 enhancement-type *n*-channel MOSFET.

Clicking on the **Setup Analysis** icon (with the blue bar at the top in the left-hand corner of the screen), **DC Sweep** is chosen to obtain the **DC Sweep** dialog box. **Voltage Source** is chosen as the **Swept Var. Type,** and **Linear** is chosen for the **Sweep Type.** Since only one curve will be obtained, there is no need for a **Nested Sweep.** The voltage-drain voltage VDD will remain fixed at a value of 9 V (about three times the threshold value (**Vto**) of 2.831 V), while the gate-to-source voltage V_{GS}, which in

this case is VGG, will be swept from 0 to 10 V. The **Name** therefore is VGG and the **Start Value** 0V, the **End Value** 10V, and the **Increment** 0.01V. After an **OK** followed by a **Close** of the **Analysis Setup,** the analysis can be performed through the **Analysis** icon. If **Automatically run Probe after simulation** is chosen under the **Probe Setup Options** of **Analysis,** the **OrCAD-MicroSim Probe** screen will result, with the horizontal axis appearing with VGG as the variable and range from 0 to 10 V. Next, the **Add Traces** dialog box can be obtained by clicking the **Traces** icon (red pointed pattern on an axis) and the **ID(M1)** chosen to obtain the drain current versus the gate-to-source voltage. Click **OK,** and the characteristics will appear on the screen. To expand the scale of the resulting plot to 20 V, simply choose **Plot** followed by **X-Axis Settings** and set the **User Defined** range to 0 to 20 V. After another **OK,** and the plot of Fig. 6.65 will result, revealing a rather high-current device. The labels **ID** and **VGS** were added using the **Text Label** icon with the letters A, B, and C. The hand-drawn load line will be described in the paragraph to follow.

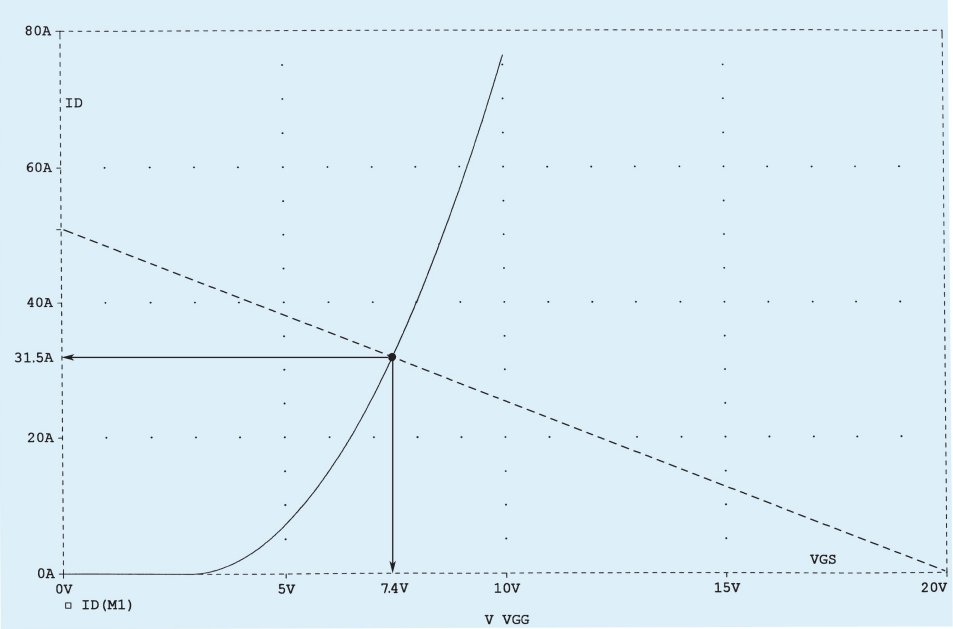

Figure 6.65 Characteristics of the IRF500 MOSFET of Figure 6.64 with a load line defined by the network of Figure 6.66.

The network of Fig. 6.66 was then established to provide a load line extending from I_D equal to 20 V/0.4 Ω = 50 A down to $V_{GS} = V_{GG} = 20$ V as shown in Fig. 6.65. A simulation resulted in the levels shown, which match the solution of Fig. 6.65.

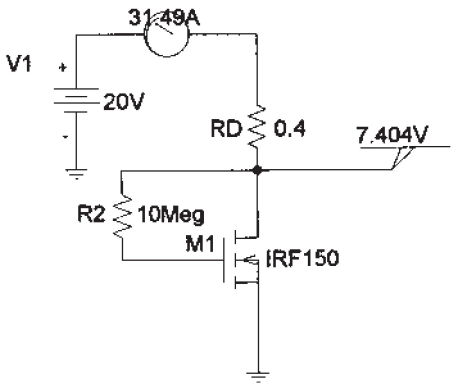

Figure 6.66 Feedback-biasing arrangement employing an IRF150 enhancement-type MOSFET.

1. For the fixed-bias configuration of Fig. 6.67:
(a) Sketch the transfer characteristics of the device.
(b) Superimpose the network equation on the same graph.
(c) Determine I_{D_Q} and V_{DS_Q}.
(d) Using Shockley's equation, solve for I_{D_Q} and then find V_{DS_Q}. Compare with the solutions of part (c).

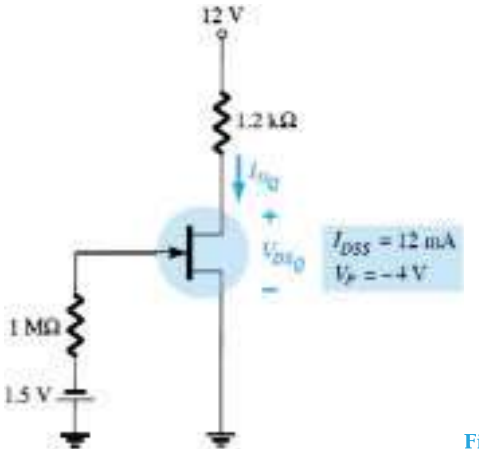

Figure 6.67 Problems 1, 35

2. For the fixed-bias configuration of Fig. 6.68, determine:
(a) I_{D_Q} and V_{GS_Q} using a purely mathematical approach.
(b) Repeat part (a) using a graphical approach and compare results.
(c) Find V_{DS}, V_D, V_G, and V_S using the results of part (a).

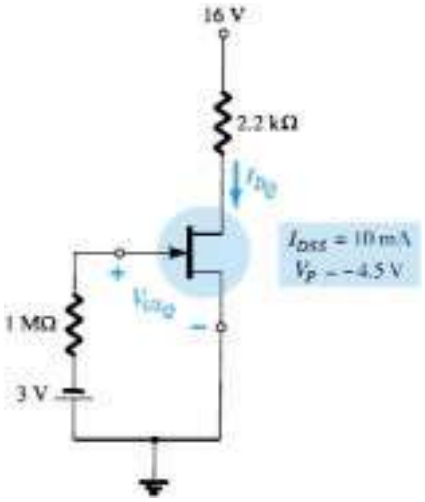

Figure 6.68 Problem 2

3. Given the measured value of V_D in Fig. 6.69, determine:
(a) I_D.
(b) V_{DS}.
(c) V_{GG}.

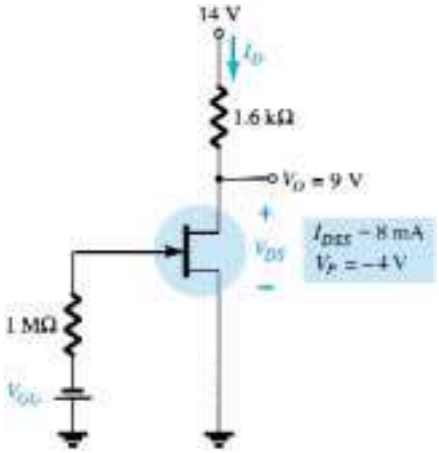

Figure 6.69 Problem 3

4. Determine V_D for the fixed-bias configuration of Fig. 6.70.
5. Determine V_D for the fixed-bias configuration of Fig. 6.71.

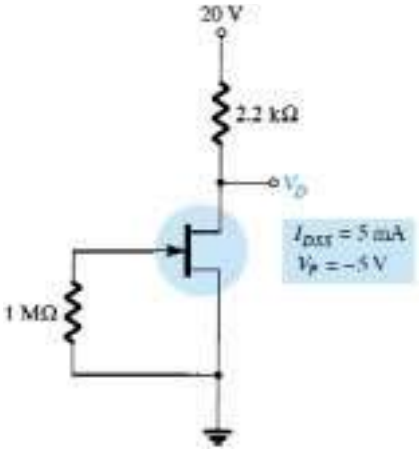

Figure 6.70 Problem 4

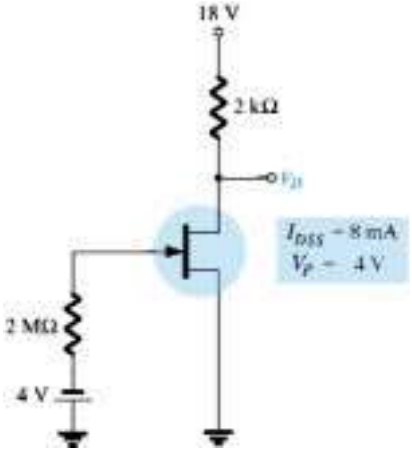

Figure 6.71 Problem 5

§ 6.3 Self-Bias Configuration

6. For the self-bias configuration of Fig. 6.72:
   (a) Sketch the transfer curve for the device.
   (b) Superimpose the network equation on the same graph.
   (c) Determine I_{DQ} and V_{GS_Q}.
   (d) Calculate V_{DS}, V_D, V_G, and V_S.

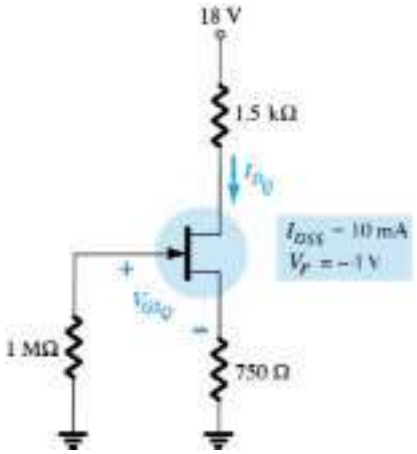

Figure 6.72 Problems 6, 7, 36

* 7. Determine I_{D_Q} for the network of Fig. 6.72 using a purely mathematical approach. That is, establish a quadratic equation for I_D and choose the solution compatible with the network characteristics. Compare to the solution obtained in Problem 6.

8. For the network of Fig. 6.73, determine:
   (a) V_{GS_Q} and I_{D_Q}.
   (b) V_{DS}, V_D, V_G, and V_S.

9. Given the measurement $V_S = 1.7$ V for the network of Fig. 6.74, determine:
   (a) I_{D_Q}.
   (b) V_{GS_Q}.
   (c) I_{DSS}.
   (d) V_D.
   (e) V_{DS}.

* **10.** For the network of Fig. 6.75, determine:
(a) I_D.
(b) V_{DS}.
(c) V_D.
(d) V_S.

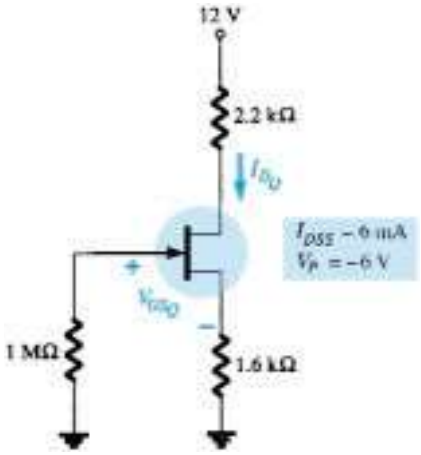

Figure 6.73 Problem 8

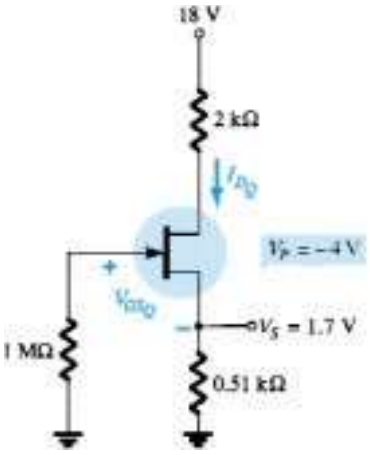

Figure 6.74 Problem 9

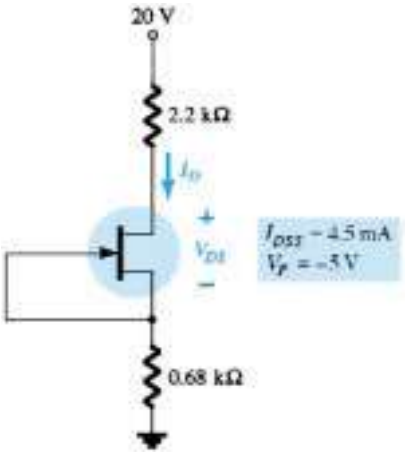

Figure 6.75 Problem 10

* **11.** Find V_S for the network of Fig. 6.76.

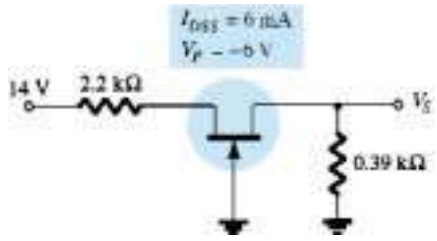

Figure 6.76 Problem 11

§ 6.4 Voltage-Divider Biasing

12. For the network of Fig. 6.77, determine:
(a) V_G.
(b) I_{D_Q} and V_{GS_Q}.
(c) V_D and V_S.
(d) V_{DS_Q}.

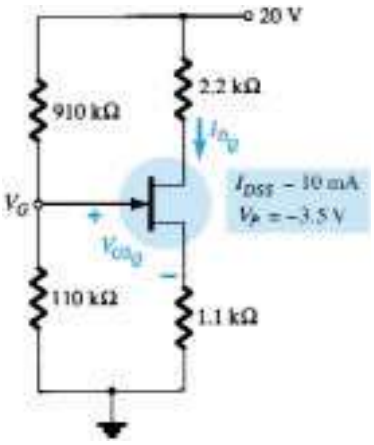

Figure 6.77 Problems 12, 13

13. (a) Repeat Problem 12 with $R_S = 0.51$ kΩ (about 50% of the value of 12). What is the effect of a smaller R_S on I_{D_Q} and V_{GS_Q}?
(b) What is the minimum possible value of R_S for the network of Fig. 6.77?

14. For the network of Fig. 6.78, $V_D = 9$ V. Determine:
    (a) I_D.
    (b) V_S and V_{DS}.
    (c) V_G and V_{GS}.
    (d) V_P.

* **15.** For the network of Fig. 6.79, determine:
    (a) I_{D_Q} and V_{GS_Q}.
    (b) V_{DS} and V_S.

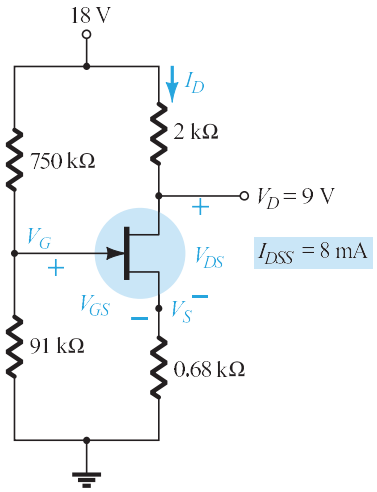

Figure 6.78 Problem 14

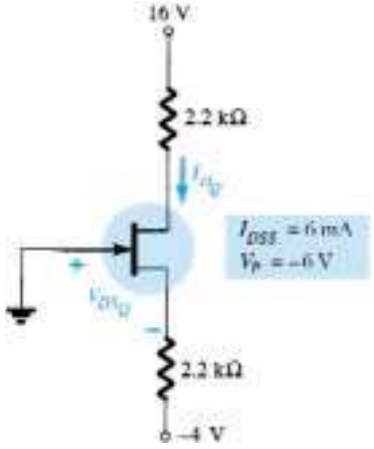

Figure 6.79 Problems 15, 37

* **16.** Given $V_{DS} = 4$ V for the network of Fig. 6.80, determine:
    (a) I_D.
    (b) V_D and V_S.
    (c) V_{GS}.

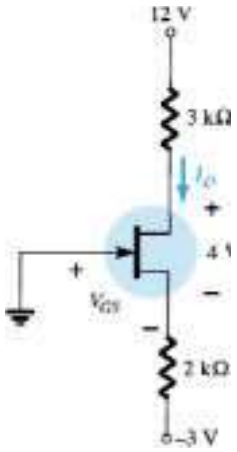

Figure 6.80 Problem 16

§ 6.5 Depletion-Type MOSFETs

17. For the self-bias configuration of Fig. 6.81, determine:
    (a) I_{D_Q} and V_{GS_Q}.
    (b) V_{DS} and V_D.

* **18.** For the network of Fig. 6.82, determine:
    (a) I_{D_Q} and V_{GS_Q}.
    (b) V_{DS} and V_S.

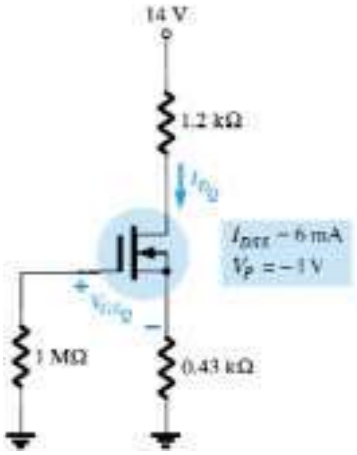

Figure 6.81 Problem 17

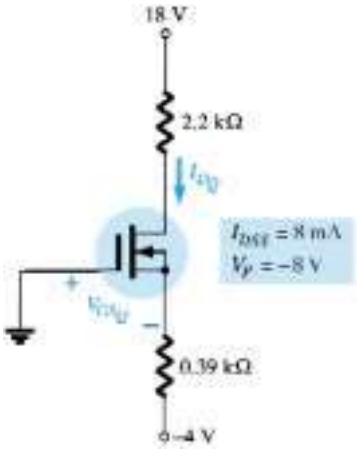

Figure 6.82 Problem 18

§ 6.6 Enhancement-Type MOSFETs

19. For the network of Fig. 6.83, determine:
(a) I_{D_Q}.
(b) V_{GS_Q} and V_{DS_Q}.
(c) V_D and V_S.
(d) V_{DS}.

20. For the voltage-divider configuration of Fig. 6.84, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_D and V_S.

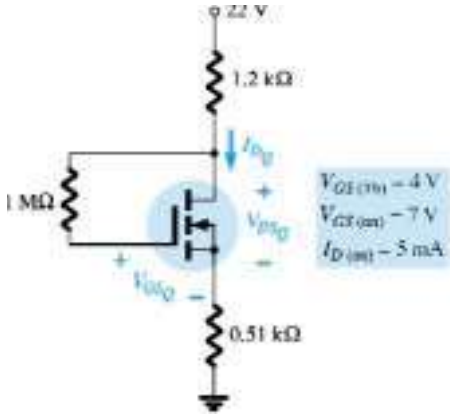

Figure 6.83 Problem 19

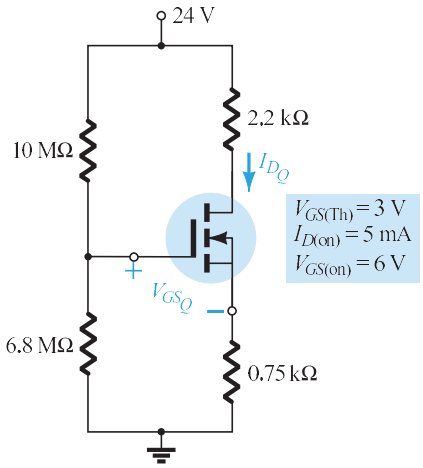

Figure 6.84 Problem 20

§ 6.8 Combination Networks

* **21.** For the network of Fig. 6.85, determine:
(a) V_G.
(b) V_{GS_Q} and I_{D_Q}.
(c) I_E.
(d) I_B.
(e) V_D.
(f) V_C.

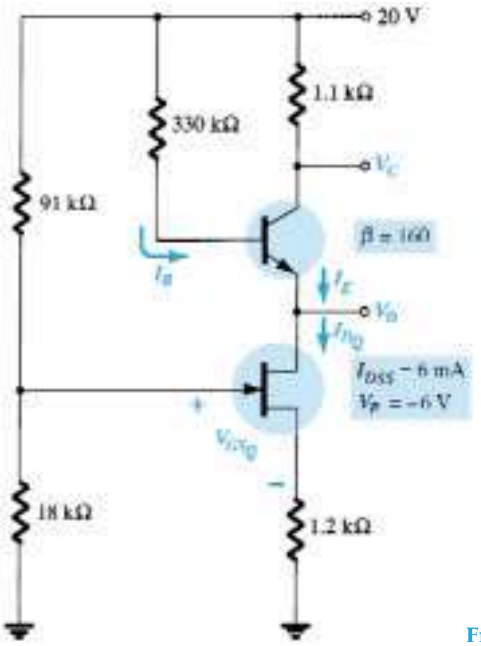

Figure 6.85 Problem 21

* **22.** For the combination network of Fig. 6.86, determine:
  (a) V_B and V_G.
  (b) V_E.
  (c) I_E, I_C, and I_D.
  (d) I_B.
  (e) V_C, V_S, and V_D.
  (f) V_{CE}.
  (g) V_{DS}.

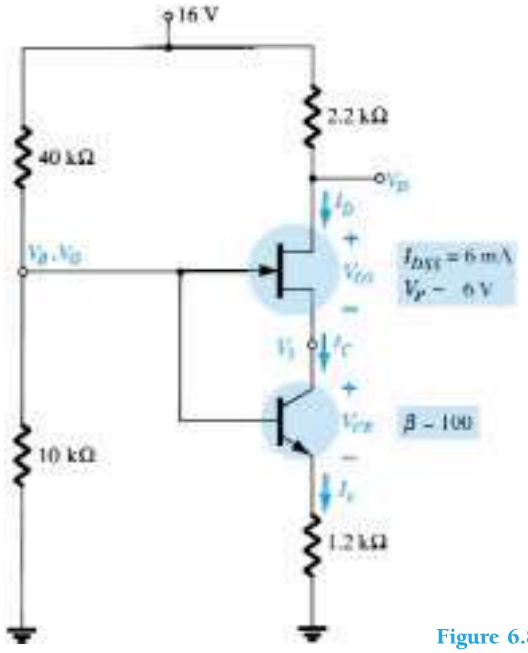

Figure 6.86 Problem 22

§ 6.9 Design

* **23.** Design a self-bias network using a JFET transistor with $I_{DSS} = 8$ mA and $V_P = -6$ V to have a Q-point at $I_{D_Q} = 4$ mA using a supply of 14 V. Assume that $R_D = 3R_S$ and use standard values.

* **24.** Design a voltage-divider bias network using a depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V to have a Q-point at $I_{D_Q} = 2.5$ mA using a supply of 24 V. In addition, set $V_G = 4$ V and use $R_D = 2.5R_S$ with $R_1 = 22$ MΩ. Use standard values.

25. Design a network such as appears in Fig. 6.39 using an enhancement-type MOSFET with $V_{GS(Th)} = 4$ V, $k = 0.5 \times 10^{-3}$A/V^2 to have a Q-point of $I_{D_Q} = 6$ mA. Use a supply of 16 V and standard values.

§ 6.10 Troubleshooting

* **26.** What do the readings for each configuration of Fig. 6.87 suggest about the operation of the network?

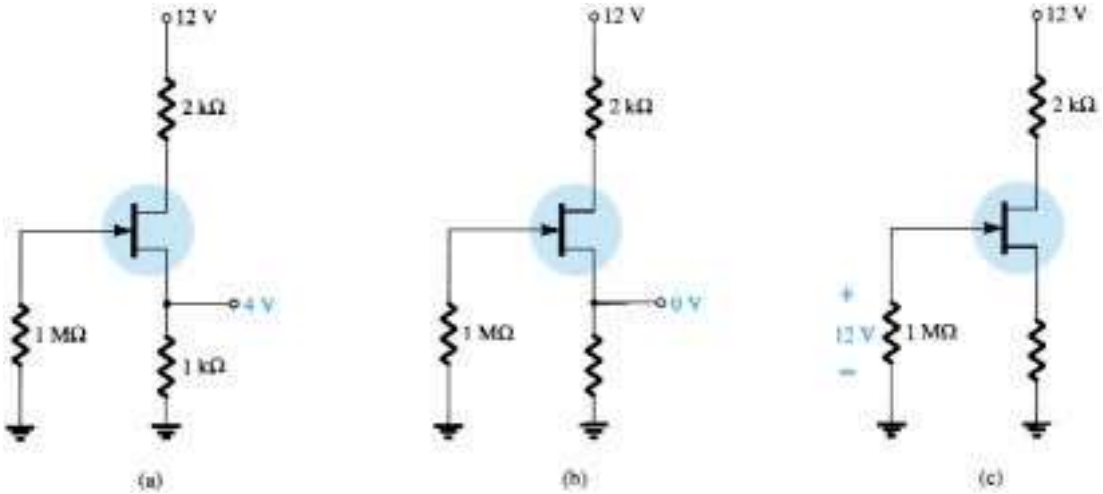

Figure 6.87 Problem 26

* **27.** Although the readings of Fig. 6.88 initially suggest that the network is behaving properly, determine a possible cause for the undesirable state of the network.

* **28.** The network of Fig. 6.89 is not operating properly. What is the specific cause for its failure?

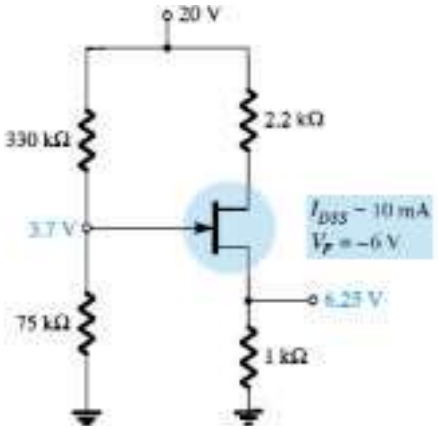

Figure 6.88 Problem 27

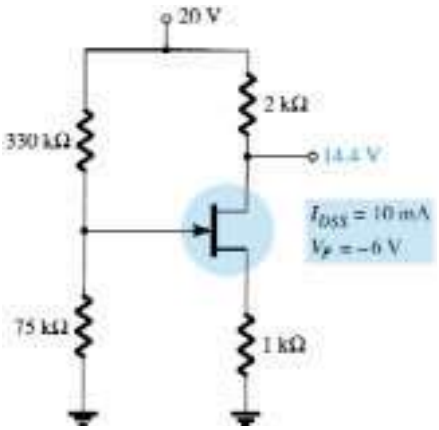

Figure 6.89 Problem 28

§ 6.11 *p*-Channel FETs

29. For the network of Fig. 6.90, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS}.
(c) V_D.

30. For the network of Fig. 6.91, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS}.
(c) V_D.

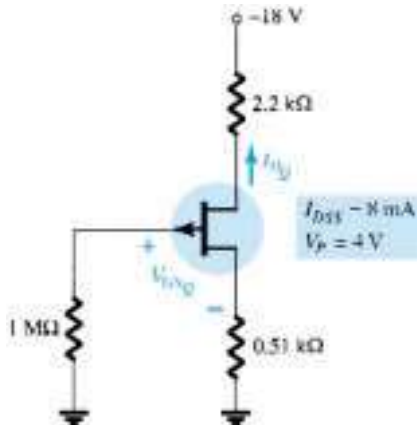

Figure 6.90 Problem 29

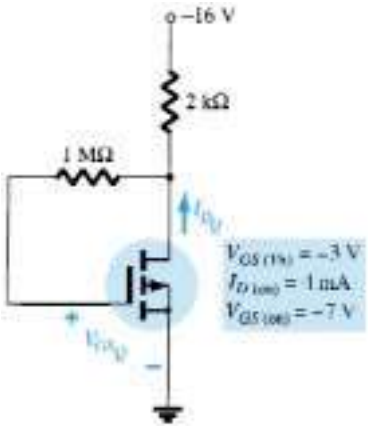

Figure 6.91 Problem 30

§ 6.12 Universal JFET Bias Curve

31. Repeat Problem 1 using the universal JFET bias curve.

32. Repeat Problem 6 using the universal JFET bias curve.

33. Repeat Problem 12 using the universal JFET bias curve.

34. Repeat Problem 15 using the universal JFET bias curve.

§ 6.13 PSpice Windows

35. Perform a PSpice Windows analysis of the network of Problem 1.

36. Perform a PSpice Windows analysis of the network of Problem 6.

37. Perform a PSpice Windows analysis of the network of Problem 15.

*Please Note: Asterisks indicate more difficult problems.