

4. Voltage-Feedback Bias Circuit:

Fig. 9-7a shows a voltage-feedback bias circuit.

Analysis:

- ◀ For the input (base-emitter circuit) loop as shown in Fig. 9-7b:

$$+V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I'_C = I_C + I_B = I_E \cong I_C = \beta I_B$$

$$+V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \quad [9.11a]$$

- ◀ For the output (collector-emitter circuit) loop as shown in Fig. 9-7c:

$$+I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

$$I'_C = I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad [9.11b]$$

Load-Line Analysis:

Continuing with the approximation $I'_C = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The levels of I_{BQ} will be defined by the chosen base configuration.

Design:

For an optimum design:

$$V_{CEQ} = \frac{1}{2} V_{CC}$$

$$I_{CQ} = \frac{1}{2} I_{C(sat)} = \frac{V_{CC}}{2(R_C + R_E)}$$

$$V_E = \frac{1}{10} V_{CC}$$

$$R_B \leq \beta(R_C + R_E)$$

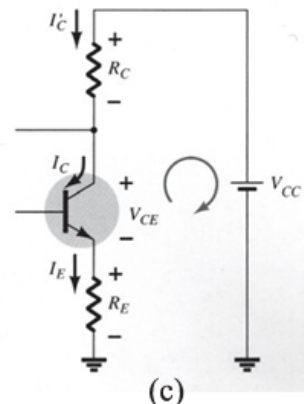
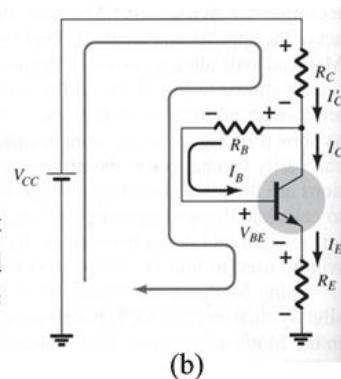
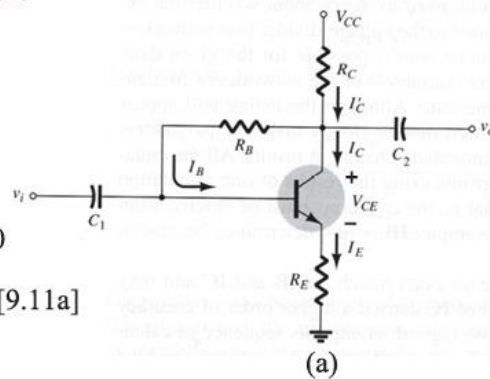


Fig. 9-7

Example 9-2: (Negative Supply)

Determine V_C and V_B for the circuit of Fig. 9-8.

Solution:

$$-I_B R_B - V_{BE} + V_{EE} = 0 \quad (\text{KVL})$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B} = \frac{9 - 0.7}{100k} = 83 \mu A$$

$$I_C = \beta I_B = (45)(83 \mu) = 3.735 \text{ mA}$$

$$V_C = -I_C R_C = -(3.735 \text{ m})(1.2k) = -4.48 \text{ V}$$

$$V_B = -I_B R_B = -(83 \mu)(100k) = -8.3 \text{ V}$$

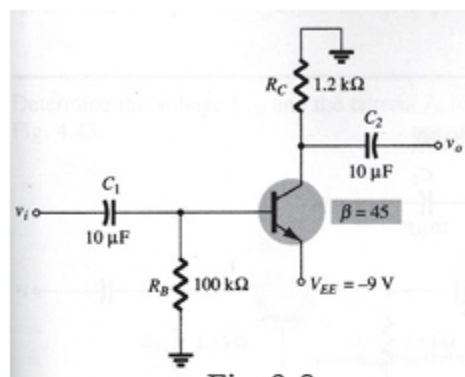


Fig. 9-8

Example 9-3: (Two Supplies)

Determine V_C and V_B for the circuit of Fig. 9-9a.

Solution:

From Fig. 9-9b:

$$R_{Th} = R_1 \parallel R_2 = 8.2k \parallel 2.2k = 1.73k\Omega$$

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20 + 20}{8.2k + 2.2k} = 3.85 \text{ mA}$$

$$E_{Th} = IR_2 - V_{EE} = (3.85 \text{ m})(2.2k) - 20 = -11.53 \text{ V}$$

From Fig. 9-9c:

$$-E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E + V_{EE} = 0 \quad (\text{KVL})$$

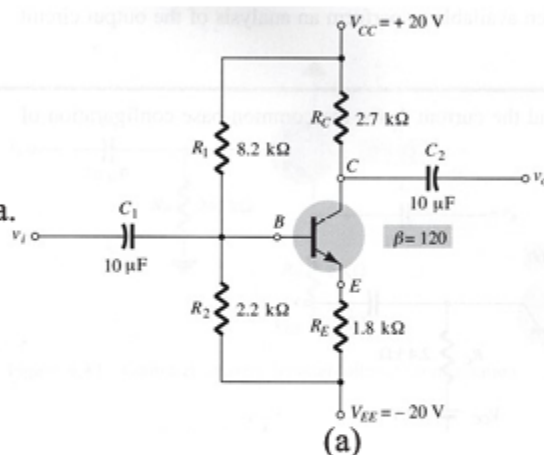
$$I_E = (\beta + 1)I_B$$

$$I_B = \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{20 - 11.53 - 0.7}{1.73k + (121)(1.8k)} = 35.39 \mu A$$

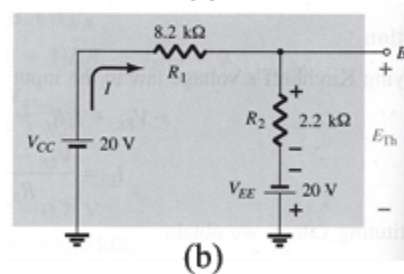
$$I_C = \beta I_B = (120)(35.39 \mu) = 4.25 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C = 20 - (4.25 \text{ m})(2.7k) = 8.53 \text{ V}$$

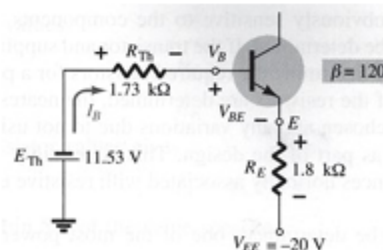
$$V_B = -E_{Th} - I_B R_{Th} = -(11.53) - (35.39 \mu)(1.73k) = -11.59 \text{ V}$$



(a)



(b)



(c)

Fig. 9-9

Example 9-4: (Common-Base)

Determine V_{CB} and I_B for the common-base configuration of Fig. 9-10.

Solution:

Applying KVL to the input circuit:

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{4 - 0.7}{1.2k} = 2.75mA$$

Applying KVL to the output circuit:

$$+V_{CB} + I_C R_C - V_{CC} = 0$$

$$V_{CB} = V_{CC} - I_C R_C$$

with $I_C \cong I_E$

$$V_{CB} = 10 - (2.75m)(2.4k) = 3.4V$$

$$I_B = \frac{I_C}{\beta} = \frac{2.75m}{60} = 45.8\mu A$$

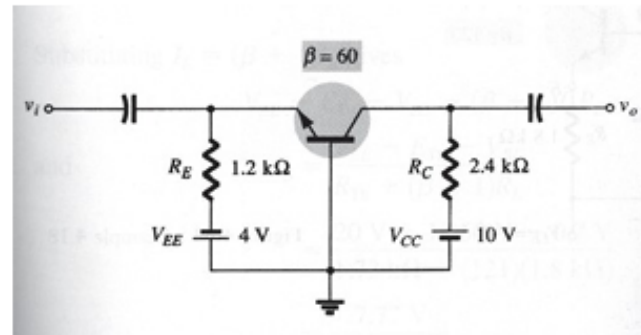


Fig. 9-10

Example 9-5: (Common-Collector)

Determine I_E and V_{CE} for the common-collector (emitter-follower) configuration of Fig. 9-11.

Solution:

Applying KVL to the input circuit:

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$I_E = (\beta + 1)I_B$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 - 0.7}{240k + (91)(2k)} = 45.73\mu A$$

$$I_E = (\beta + 1)I_B = (91)(45.73\mu) = 4.16mA$$

Applying KVL to the output circuit:

$$-V_{EE} + I_E R_E + V_{CE} = 0$$

$$V_{CE} = V_{EE} - I_E R_E = 20 - (4.16m)(2k) = 11.68V$$

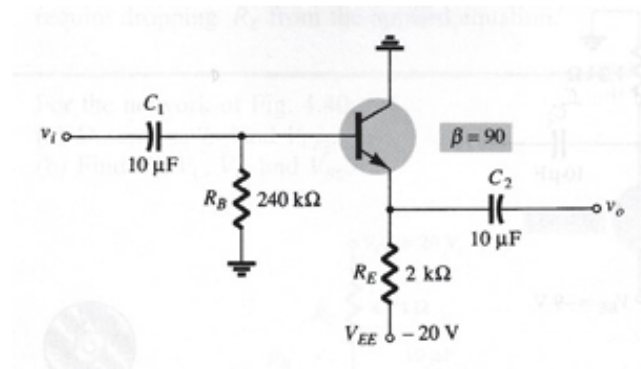


Fig. 9-11

Example 9-6: (PNP Transistor)

Determine V_{CE} for the voltage-divider bias configuration of Fig. 9-12.

Solution:

Testing: $\beta R_E \geq 10 R_2$

$$(120)(1.1k) \geq 10(10k)$$

$$132k\Omega \geq 100k\Omega \text{ (satisfied)}$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(10k)(-18)}{47k + 10k} = -3.16V$$

$$V_E = V_B - V_{BE} = -3.16 - (-0.7) = -2.46V$$

$$I_C = I_E = \frac{V_E}{R_E} = \frac{2.46}{1.1k} = 2.24mA$$

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0 \quad (\text{KVL})$$

$$V_{CE} = -V_{CC} + I_C(R_C + R_E) \\ = -18 + (2.24m)(2.4k + 1.1k) = -10.16V$$

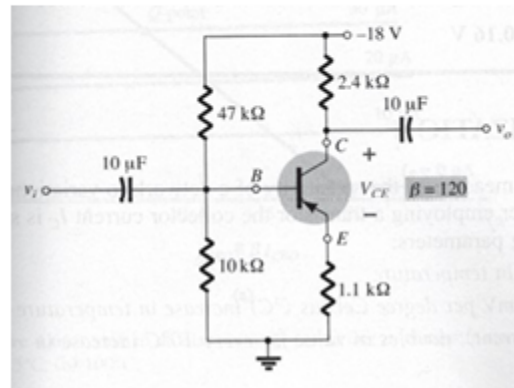


Fig. 9-12

Exercises:

- For the fixed-biased configuration of Fig. 9-2a with the following parameters: $V_{CC} = +12V$, $\beta = 50$, $R_B = 240k\Omega$, and $R_C = 2.2k\Omega$, determine: I_{BQ} , I_{CQ} , V_{CEQ} , V_B , V_C , and V_{BC} .
- Given the device characteristics of Fig. 9-13a, determine V_{CC} , R_B , and R_C for the fixed-bias configuration of Fig. 9-13b.

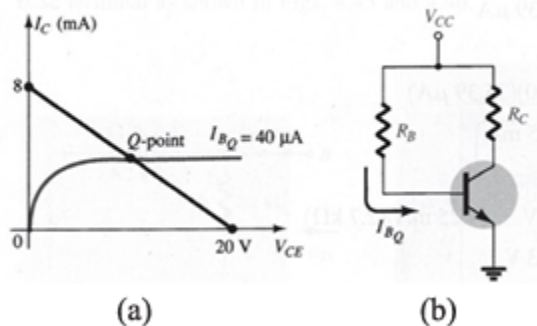


Fig. 9-13