Al-Mustaqbal University / College of Engineering & Technology
Department (Communication Technical Engineering)
Class (First)
Subject (ELECTRONIC CIRCUITS)/ Code/ UOMU028022)
(Lecturer (Prof.Dr.Haider J Abd)
2nd term – Lecture No. & Lecture Name (Lec 7: BJT switching Circuit)

Part 2:

$S(I_{CO}) = 3.8,$

$\Delta I_{CO} = 10\mu - 0.2\mu = 9.8\mu A.$

$$S(V_{BE}) = \frac{-\beta}{(\beta+1)R_E + R_{Th}} = \frac{-80}{(81)(1.5k) + 4.4k} = -0.635mS,$$

$\Delta V_{BE} = 0.5 - 0.7 = -0.2V.$

$\beta_2 = \beta_1(1 + 25/100) = 1.25\beta_1 = 1.25(80) = 100,$

$$S(\beta) = \frac{(I_{C_1}/\beta_1)(R_E + R_{Th})}{(\beta_2+1)R_E + R_{Th}} = \frac{(1m/80)(1.5k + 4.4k)}{(101)(1.5k) + 4.4k} = 0.473\mu A,$$

$\Delta\beta = 100 - 80 = 20.$

$$\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta$$
$$= (3.8)(9.8\mu) + (-0.635m)(-0.2) + (0.473\mu)(20) = 0.174mA.$$

Part 3:

Since I_{CO}, doubles in value for every 10°C increase in temperature.

Thus $N = \frac{\Delta T}{10} = \frac{75-25}{10} = 5$, $I_{CO}(75^oC) = 2^N \cdot I_{CO}(25^oC) = (2^5)(0.2\mu) = 6.4\mu A$.

$\Delta I_{CO} = 6.4\mu - 0.2\mu = 6.2\mu A.$

Since V_{BE}, decreases about 7.5 mV per 1°C increase in temperature.

Thus $\Delta T = 75 - 25 = 50^oC$, $V_{BE}(25^oC) = 0.7V$ =>

$V_{BE}(75^oC) = 0.7 - 50(7.5m) = 0.325V.$

$$\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE}$$
$$= (3.8)(6.2\mu) + (-0.635m)(-0.375) = 0.262mA.$$

Exercises:

1. Derive a mathematical expression to determine the stability factor $S(V_{CC}) = \Delta I_C/\Delta V_{CC}$ for the emitter-stabilized bias circuit.

2. Discuss and compare (by equations) between the relative levels of stability for the following biasing circuits:
   i. the fixed-bias circuit,
   ii. the emitter-stabilized bias circuit,
   iii. the voltage-divider bias circuit, and
   iv. the voltage-feedback circuit.

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BJT Switching Circuits

Basic Concepts:

The application of transistors is not limited solely to the amplification of signals. Through proper design it can be used as a switch for computer and control applications. The circuit of Fig. 11-1a can be employed as an ***inverter*** in computer logic circuitry. Note that the output voltage V_C is opposite to that applied to the base or input terminal. In addition, note the absence of a dc supply connected to the base circuit. The only dc source is connected to the collector or output side and for computer applications is typically equal to the magnitude of the "high" side of the applied signal-in this case 5V.

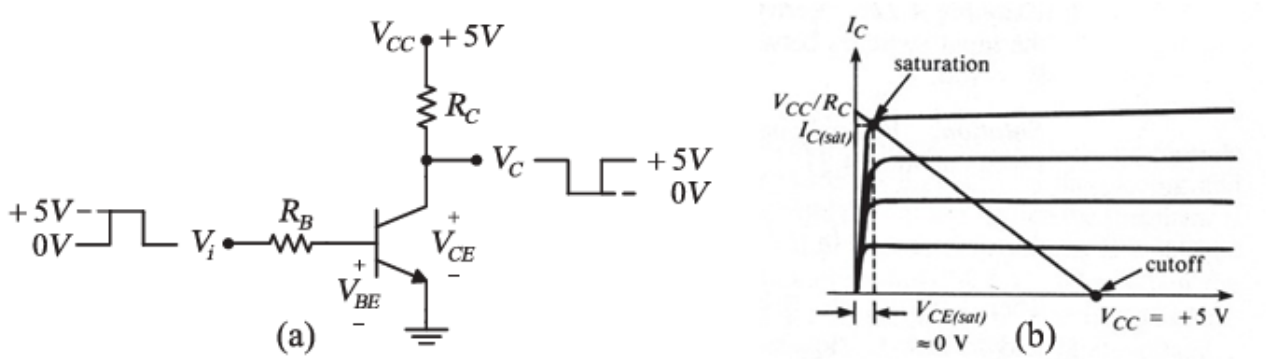

Fig. 11-1

Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Fig. 11-1b. For our purposes we will assume that $I_C = I_{CEO} \approx 0$ mA when $I_B = 0$ μA (an excellent approximation in light of improving construction techniques), as shown in Fig. 11-1b. In addition, we will assume that $V_{CE} = V_{CE(sat)} \approx 0$ V rather than the typical 0.1 to 0.3 V level.

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When $V_i = 5$ V, the transistor will be "on" and the design must ensure that the circuit is heavily saturated by a level of I_B greater than that associated with the I_B curve appearing near the saturation level.

The base current I_B for the circuit of Fig. 11-1a is determined by

$$I_B = \frac{V_i - V_{BE}}{R_B} \qquad [11.1]$$

The saturation level for collector current $I_{C(sat)}$ for the same circuit is defined by

$$I_{C(sat)} = \frac{V_{CC}}{R_C} \qquad [11.2]$$

The level of I_B in the active region just before saturation results can be approximated by the following equation:

$$I_{B(max)} \cong \frac{I_{C(sat)}}{\beta} \qquad [11.3]$$

For the saturation level we must therefore ensure that the following is satisfied:

$$I_B > I_{B(max)} \qquad [11.4]$$

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Example 11-1:

Verify that the circuit shown in Fig. 11-2 behaves like an inverter when the input switches between 0 V and +10 V. Assume that the transistor is silicon and that $\beta = 50$.

Solution:

It is only necessary to verify that the transistor is saturated when $V_i = +10$ V.

$$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{10 - 0.7}{220k} = 42.3\mu A.$$

$$I_{B(\max)} = \frac{I_{C(sat)}}{\beta} = \frac{V_{CC}}{\beta R_C} = \frac{10}{(50)(6.2k)} = 32.3\mu A.$$

Thus, we have $I_B > I_{B(\max)}$, therefore the transistor is saturated, and the circuit is inverter.

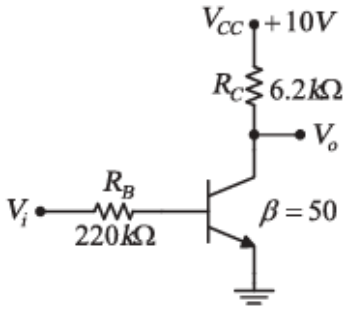

Fig. 11-2

Example 11-2:

Verify that the circuit shown in Fig. 11-3 is an inverter when the input switches between 0 V and -5 V. What minimum value of β is required? Assume that the transistor is silicon.

Solution:

When $V_i = 0V$, $V_B = \frac{(4)(5k)}{20k + 5k} = 0.8V$, hence the transistor is at cutoff, so that D_1 and D_2 are on and $V_o = -4 - 0.7 - 0.3 = -5V$.

When $V_i = -5V$, $R_{Th} = 5k \| 20k = 4k\Omega$,

$$E_{Th} = \frac{(+4)(5k)}{20k + 5k} + \frac{(-5)(20k)}{20k + 5k} = -3.2V,$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th}} = \frac{3.2 - 0.7}{4k} = 625\mu A.$$

We assume the transistor is at saturation, $V_o = 0V$, so that D_1 and D_2 are off and

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20}{1.6k} = 12.5mA,$$

$$I_{B(\max)} = I_{C(sat)} / \beta = 12.5mA/\beta.$$

For the transistor to be in saturation,

$$I_B > I_{B(\max)} \Rightarrow \beta > \frac{I_{C(sat)}}{I_B} = \frac{12.5m}{625\mu} = 20.$$

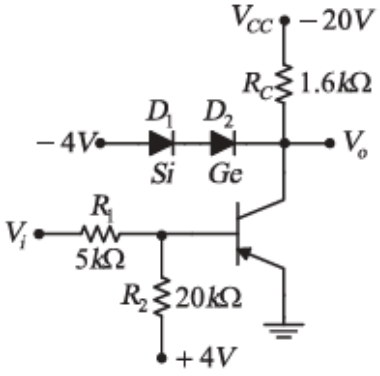

Fig. 11-3

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Exercise:

1. Design the transistor inverter of Fig. 11-4 to operate with a saturation current of 8 mA using a transistor with a beta of 100. Use a level of I_B equal to 120% of $I_{B(max)}$ and standard resistor values.

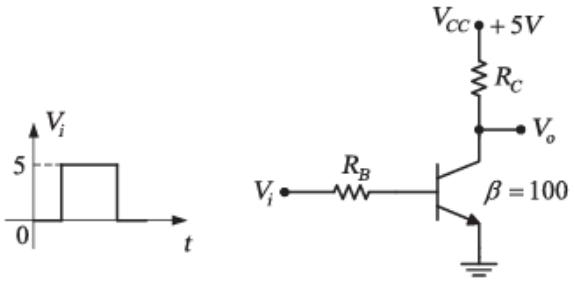

Fig. 11-4

2. Verify that the circuit shown in Fig. 11-5 is a positive NAND when the input switches between 0 V and +12 V. Neglect source impedance and junction saturation voltages and diode voltages in forward direction. Find the minimum value of β.

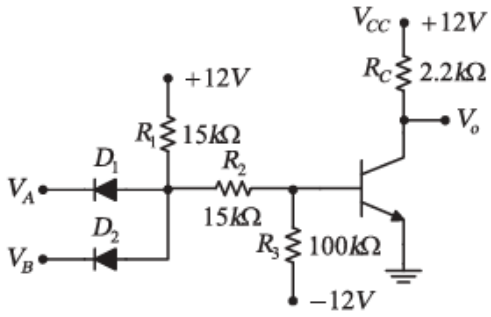

Fig. 11-5

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