Al-Mustaqbal University / College of Engineering & Technology
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Class (First)
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(Lecturer (Prof.Dr.Haider J Abd)
2nd term – Lecture No. & Lecture Name (Lec 8: Field Effect Transistor)

19.1 Types of Field Effect Transistors

A bipolar junction transistor (*BJT*) is a current controlled device *i.e.*, output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (*FET*), the output characteristics are controlled by input voltage (*i.e.*, electric field) and not by input current. This is probably the biggest difference between *BJT* and *FET*. There are two basic types of field effect transistors:

(*i*) Junction field effect transistor (*JFET*)

(*ii*) Metal oxide semiconductor field effect transistor (*MOSFET*)

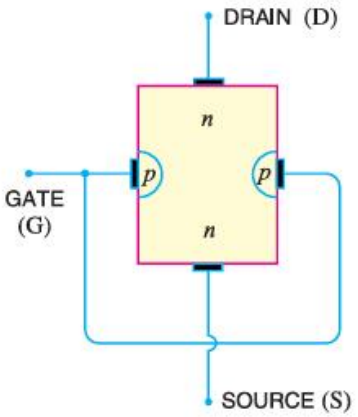
To begin with, we shall study about *JFET* and then improved form of *JFET*, namely; *MOSFET*.

19.2 Junction Field Effect Transistor (JFET)

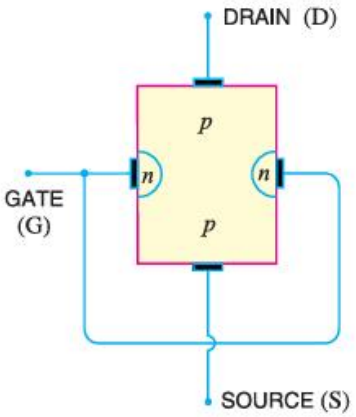
A junction field effect transistor *is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.*

The *JFET* was developed about the same time as the transistor but it came into general use only in the late 1960s. In a *JFET*, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The *JFET* has high input impedance and low noise level.

Constructional details. A *JFET* consists of a *p*-type or *n*-type silicon bar containing two *pn* junctions at the sides as shown in Fig.19.1. The bar forms the conducting channel for the charge carriers. If the bar is of *n*-type, it is called *n-channel JFET* as shown in Fig. 19.1 (*i*) and if the bar is of *p*-type, it is called a *p-channel JFET* as shown in Fig. 19.1 (*ii*). The two *pn* junctions forming diodes are connected *internally and a common terminal called *gate* is taken out. Other terminals are *source* and *drain* taken out from the bar as shown. Thus a *JFET* has essentially three terminals *viz.*, *gate* (*G*), *source* (*S*) and *drain* (*D*).



n-Channel JFET
(*i*)



p-Channel JFET
(*ii*)

JFET polarities. Fig. 19.2 (*i*) shows *n*-channel *JFET* polarities whereas Fig. 19.2 (*ii*) shows the *p*-channel *JFET* polarities. Note that in each case, the voltage between the gate and source is such that the gate is reverse biased. This is the normal way of *JFET* connection. The drain and source terminals are interchangeable *i.e.*, either end can be used as source and the other end as drain.

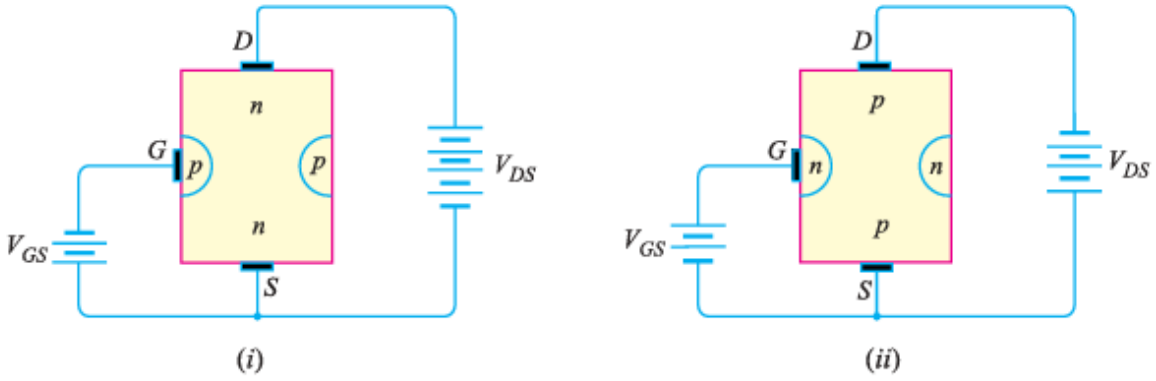


Fig. 19.2

The following points may be noted :

(*i*) The input circuit (*i.e.* gate to source) of a *JFET* is reverse biased. This means that the device has high input impedance.

(*ii*) The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.

(*iii*) In all *JFETs*, source current I_S is equal to the drain current *i.e.* $I_S = I_D$.

19.3 Principle and Working of JFET

Fig. 19.3 shows the circuit of *n*-channel *JFET* with normal polarities. Note that the gate is reverse biased.

Principle. The two *pn* junctions at the sides form two depletion layers. The current conduction by charge carriers (*i.e.* free electrons in this case) is through the channel between the two depletion layers and out of the drain. The width and hence *resistance of this channel can be controlled by changing the input voltage V_{GS}. The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease. *Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.* In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS}.

Working. The working of *JFET* is as under :

(*i*) When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero [See Fig. 19.3 (*i*)], the two *pn* junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

(*ii*) When a reverse voltage V_{GS} is applied between the gate and source [See Fig. 19.3 (*ii*)], the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of *n*-type bar. Consequently, the current from source to drain is decreased. On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.

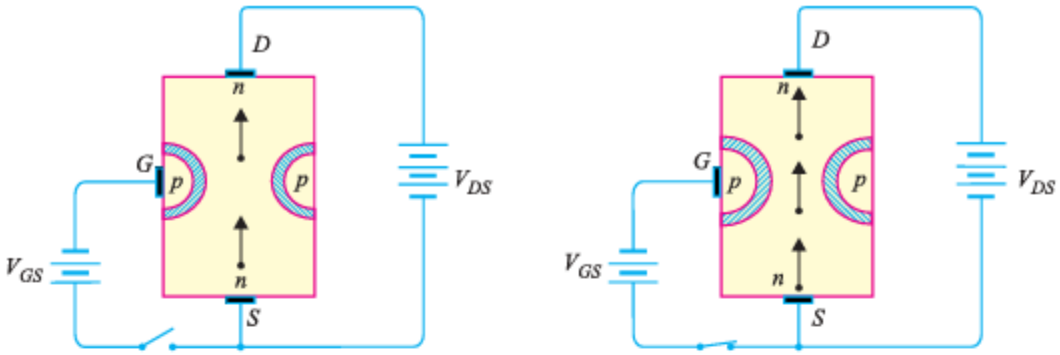
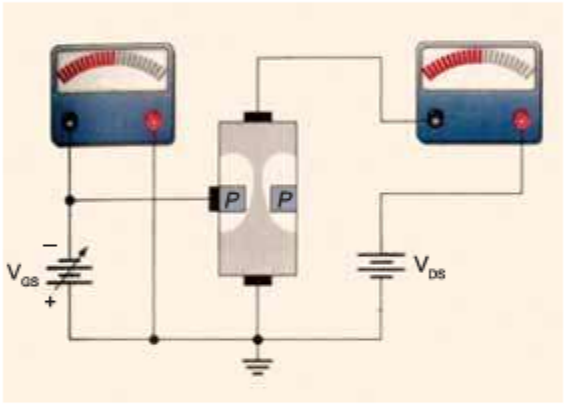


Fig. 19.3

It is clear from the above discussion that current from source to drain can be controlled by the application of potential (*i.e.* electric field) on the gate. For this reason, the device is called *field effect transistor*. It may be noted that a *p*-channel *JFET* operates in the same manner as an *n* -channel *JFET* except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

Note. If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layers touch each other and the channel is cut off. Under such conditions, the channel becomes a non-conductor.



JFET biased for Conduction

19.4 Schematic Symbol of JFET

Fig. 19.4 shows the schematic symbol of *JFET*. The vertical line in the symbol may be thought

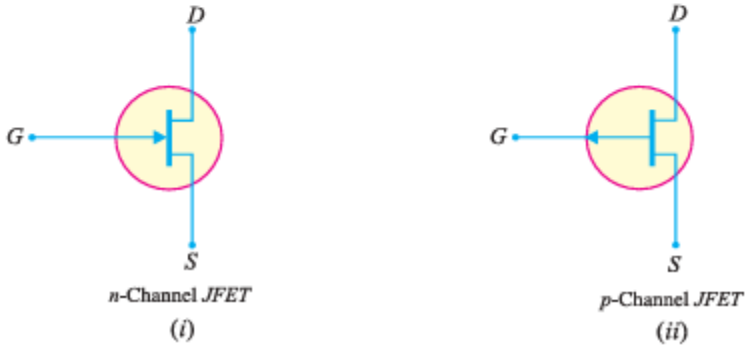
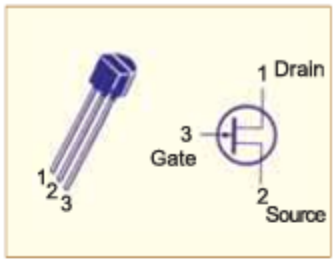


Fig. 19.4

as channel and source (S) and drain (D) connected to this line. If the channel is *n*-type, the arrow on the gate points towards the channel as shown in Fig. 19.4 (*i*). However, for *p*-type channel, the arrow on the gate points from channel to gate [See Fig. 19.4 (*ii*)].



19.5 Importance of JFET

A *JFET* acts like a voltage controlled device *i.e.* input voltage (V_{GS}) controls the output current. This is different from ordinary transistor (or bipolar transistor) where input current controls the output current. Thus *JFET* is a semiconductor device acting *like a vacuum tube. The need for *JFET* arose because as modern electronic equipment became increasingly transistorised, it became apparent that there were many functions in which bipolar transistors were unable to replace vacuum tubes. Owing to their extremely high input impedance, *JFET* devices are more like vacuum tubes than are the bipolar transistors and hence are able to take over many vacuum-tube functions. Thus, because of *JFET*, electronic equipment is closer today to being completely solid state.

The *JFET* devices have not only taken over the functions of vacuum tubes but they now also threaten to depose the bipolar transistors as the most widely used semiconductor devices. As an amplifier, the *JFET* has higher input impedance than that of a conventional transistor, generates less noise and has greater resistance to nuclear radiations.

19.6 Difference Between JFET and Bipolar Transistor

The *JFET* differs from an ordinary or bipolar transistor in the following ways :

(*i*) In a *JFET*, there is only one type of carrier, holes in *p*-type channel and electrons in *n*-type channel. For this reason, it is also called a *unipolar transistor*. However, in an ordinary transistor, both holes and electrons play part in conduction. Therefore, an ordinary transistor is sometimes called a *bipolar transistor*.

(*ii*) As the input circuit (*i.e.*, gate to source) of a *JFET* is reverse biased, therefore, the device has high input impedance. However, the input circuit of an ordinary transistor is forward biased and hence has low input impedance.

(*iii*) The primary functional difference between the *JFET* and the *BJT* is that no current (actually, a very, very small current) enters the gate of *JFET* (*i.e.* $I_G = 0$A). However, typical *BJT* base current might be a few μA while *JFET* gate current a thousand times smaller [See Fig. 19.5].

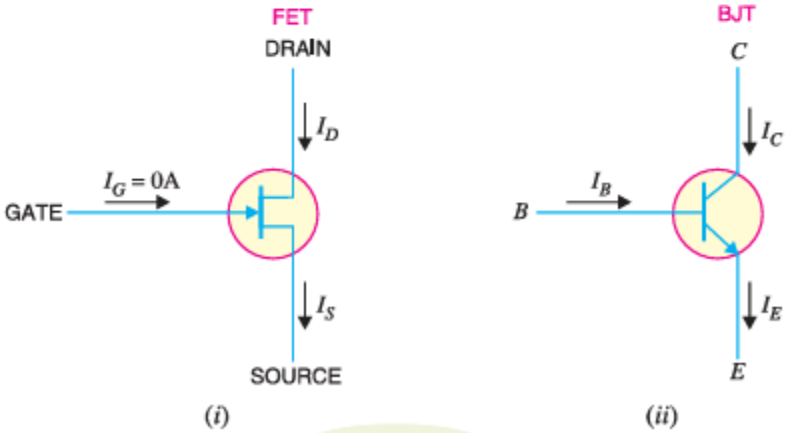


Fig. 19.5

* The gate, source and drain of a *JFET* correspond to grid, cathode and anode of a vacuum tube.

(iv) A bipolar transistor uses a current into its base to control a large current between collector and emitter whereas a *JFET* uses voltage on the 'gate' (= base) terminal to control the current between drain (= collector) and source (= emitter). Thus a bipolar transistor gain is characterised by current gain whereas the *JFET* gain is characterised as a transconductance *i.e.*, the ratio of change in output current (drain current) to the input (gate) voltage.

(v) In *JFET*, there are no junctions as in an ordinary transistor. The conduction is through an *n*- type or *p*-type semi-conductor material. For this reason, noise level in *JFET* is very small.

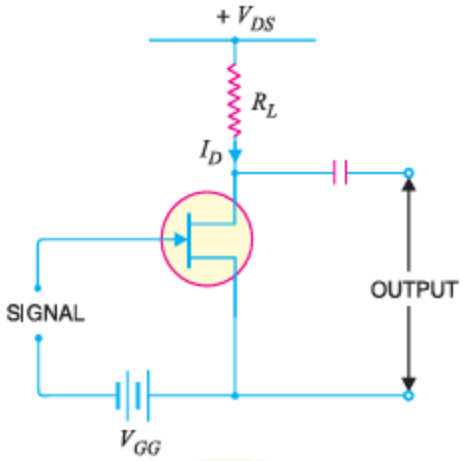


Fig. 19.6

19.7 JFET as an Amplifier

Fig. 19.6 shows *JFET* amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of *JFET*, the gate must be negative w.r.t. source *i.e.*, input circuit should always be reverse biased. This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit. In the present case, we are providing biasing by the battery V_{GG}.

A small change in the reverse bias on the gate produces a large change in drain current. This fact makes *JFET* capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current. During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases. The result is that a small change in voltage at the gate produces a large change in drain current. These large variations in drain current produce large output across the load R_L. In this way, *JFET* acts as an amplifier.

19.8 Output Characteristics of JFET

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a *JFET* at constant gate-source voltage (V_{GS}) is known as *output characteristics of JFET*. Fig. 19.7 shows the circuit for determining the output characteristics of *JFET*. Keeping V_{GS} fixed at some value, say 1V, the drian-source voltage is changed in steps. Corresponding to each value of V_{DS}, the drain current I_D is noted. A plot of these values gives the output characteristic of *JFET* at V_{GS} = 1V. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. 19.8 shows a family of output characteristics.

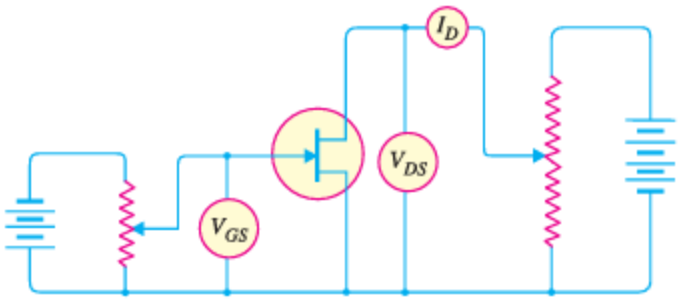


Fig. 19.7

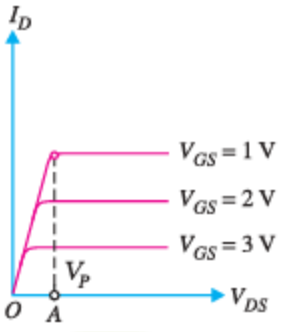


Fig. 19.8

The following points may be noted from the characteristics :

(*i*) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as *pinch off voltage*. Thus in Fig. 19.8, OA is the *pinch off voltage* V_P.

(*ii*) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch off voltage. Consequently, drain current remains constant.

(*iii*) The characteristics resemble that of a pentode valve.

19.9 Salient Features of JFET

The following are some salient features of *JFET*:

(*i*) A *JFET* is a three-terminal *voltage-controlled* semiconductor device *i.e.* input voltage controls the output characteristics of *JFET*.

(*ii*) The *JFET* is *always* operated with gate-source *pn* junction *reverse biased.

(*iii*) In a *JFET*, the gate current is zero *i.e.* $I_G = 0$A.

(*iv*) Since there is no gate current, $I_D = I_S$.

(*v*) The *JFET* must be operated between V_{GS} and $V_{GS\,(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

(*vi*) Because the two gates are at the same potential, both depletion layers widen or narrow down by an equal amount.

(*vii*) The *JFET* is not subjected to thermal runaway when the temperature of the device increases.

(*viii*) The drain current I_D is controlled by changing the channel width.

(*ix*) Since *JFET* has no gate current, there is no β rating of the device. We can find drain current I_D by using the eq. mentioned in Art. 19.11.

19.10 Important Terms

In the analysis of a *JFET* circuit, the following important terms are often used :

1. Shorted-gate drain current (I_{DSS})
2. Pinch off voltage (V_P)
3. Gate-source cut off voltage [$V_{GS(off)}$]

1. Shorted-gate drain current (I_{DSS}). *It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage.* It is sometimes called *zero-bias current*.

Fig 19.9 shows the *JFET* circuit with $V_{GS} = 0$ *i.e.*, source shorted-circuited to gate. This is normally called shorted-gate condition. Fig. 19.10 shows the graph between I_D and V_{DS} for the shorted gate condition. The drain current rises rapidly at first and then levels off at pinch off voltage V_P. The drain current has now reached the maximum value I_{DSS}. When V_{DS} is increased beyond V_P, the depletion layers expand at the top of the channel. The channel now acts as a current limiter and **holds drain current constant at I_{DSS}.

* Forward biasing gate-source *pn* junction may destroy the device.

** When drain voltage equals V_P, the channel becomes narrow and the depletion layers almost touch each other. The channel now acts as a current limiter and holds drain current at a constant value of I_{DSS}.