Lesson Seven

8085 Time Delay and Counters

Lesson Objectives:

- **To introduce the types of time delay.**
- **To write a program that generates specified time delay.**
- **To learn how to determine the time delay based on one register or pair of registers.**

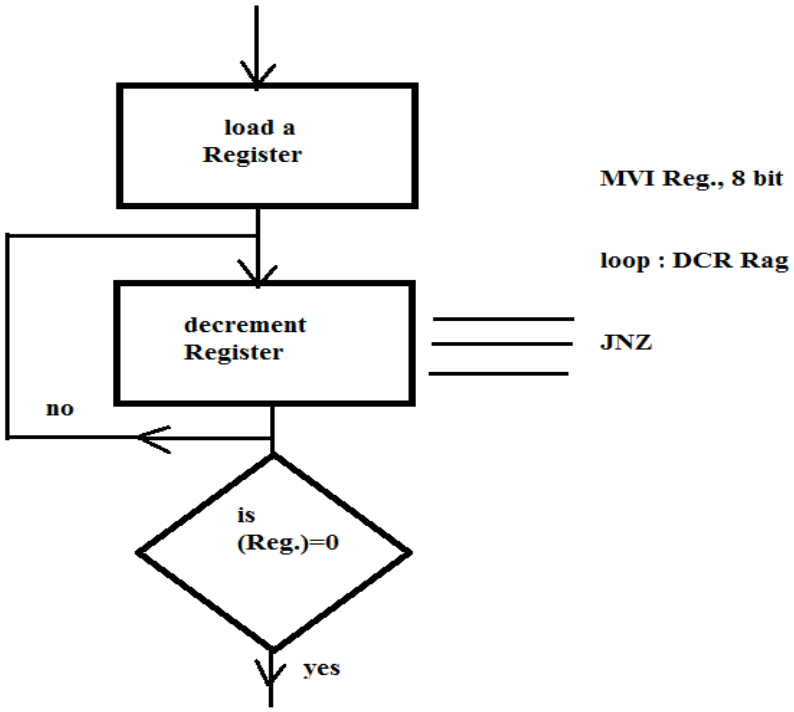
Pre Test:

- **What are the types of time delay can be produced by 8085µp.**
- **What is the maximum time delay generated by pair of register.**
- **Write a program to generate 5msec time delay**

Time Delay and Counters

Time delay: a register (or pair of registers) is loaded with a number depending on the time delay required, then the register is decremented until it equals to zero. Also, (NoP) instruction can be used to generate time delay equals to 4 T- states.

1- Time Delay With One Register



Ex.:

What is time delay generated by the following program if the clock frequency = 2MHz?

MVI C, FF ⟶ 7T
Loop: DCR C. ⟶ 4T
JNZ Loop ⟶ 10/7T

Total delay = time outside the loop + loop execution time
$T_D = T_O + T_L$
T_O= 7 * 1/2MHz = 3.5 µsec
$T_L = (\sum (N_{Tstates} * 1/f)) * N$, where N is the number loaded to the register
= ((4+10)* (1/2MHz))*255 Note FFH= 255_{10}
= 1785 µsec ≈**1.8 msec**

$T_{D\ approximate}$ = 3.5 µsec + 1785 µsec = 1788.5 µsec
$T_{D\ accurate}$ = 3.5 µsec + (1785- 1.5) µsec = 1787 µsec
Note: The max. time delay is generated by one register loaded with (FFH) and equals to 1787 µsec (~ 1.8 msec).

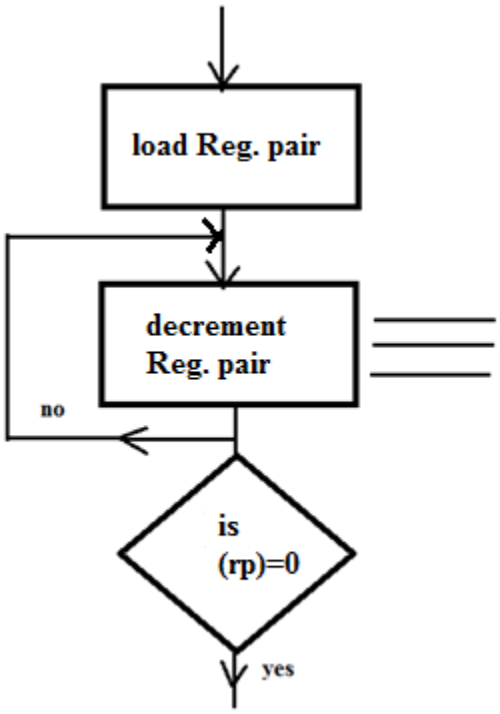
H.W. **What will be the time delay generated with one register if the number loaded to that register equals to :**
1- 78 H, 2- A3 H, 3- 5EH

EX.: **Write a program to generate time delay equals to (1 msec).**

MVI C, **?** ⟶ 7 T
*: DCR C ⟶ 4 T
JNZ * ⟶ 10 / 7 T

$T_D = T_O + T_L$= 1 msec
T_O= 3.5 µsec
T_L= 1000 µsec- 3.5 µsec= 996.5 µsec
996.5= N_{10}* 14*(1/2MHz), N_{10} =142.35 ~8 EH

2- ***Time Delay With Pair Register***



LXI rp, 16 bit 10 T
Loop: DCX rp 6T (Does not affect the zero flag)
MOV A, rp_L 4T
ORA rp_H 4T
JNZ Loop 10/7T

EX.:

What is the max. time delay can be generated with pair of register?

Solution:

The max. time delay can be generated when the pair of register is loaded by FFFFH ($=65535_{10}$)

```
     LXI B, FFFF      10T
*:   DCX B            6T
     MOV A, C         4T
     ORA  B           4T
     JNZ   *          10/7 T
```

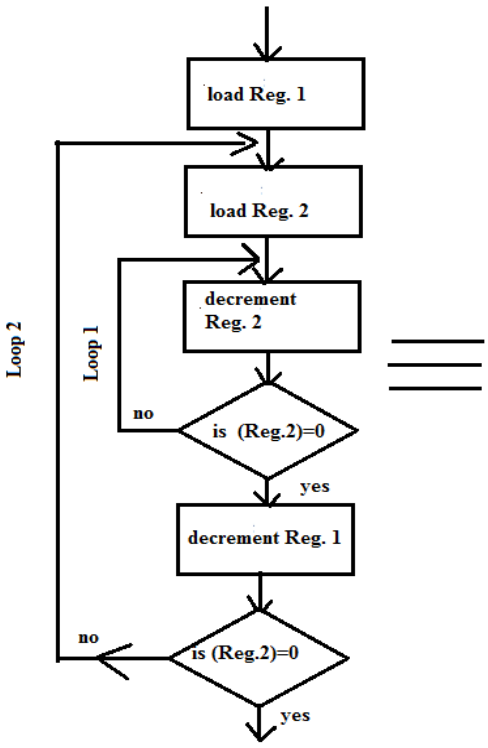
$T_D = T_O + T_L$

$T_D = 10 * (1/2) = 5\ \mu sec$

$T_L = (6+4+4+10)*(1/2) * 65535$

$= 786420\ \mu sec \simeq 786\ msec$

3- Time Delay Generated by Loop within Loop




```
          MVI Reg.1, 8 bit      7T
Loop 2:   MVI Reg.2, 8 bit      7T
Loop 1:   DCR Reg.2,            4T      } TL1      TL2
          JNZ  Loop 1           10/7T   }
          DCR Reg.1             4T
          JNZ  Loop 2           10/7T
```

EX.:

What is the time delay generated by following program?

```
        MVI  B, 38 H        7T  } T0
Loop 2: MVI  C, FF          7T
Loop 1: DCR  C              4T
        JNZ  Loop 1         10/7T
        DCR  B              4T
        JNZ  Loop 2         10/7T
```

T_{L1} T_{L2}

Time delay (T_D) = T_O+ T_L

T_O= 7*(1/2) = 3.5 µsec

T_L= T_{L2} = [T_{L1}+ ($\sum$ $(T)_{L2}$ *1/f)] * 56_{10} ($38H= 56_{10}$)

= [T_{L1}+ (7+4+10)* ½] * 56_{10}

= [T_{L1} + 10.5] * 56_{10}

T_{L1}= ($\sum$ (T_{L1})* 1/f)* 255_{10} ($FFH= 255_{10}$)

= (14 * ½) * 255_{10}

≃1.8 msec= 1783.5 µsec

T_L= (1783.5+ 10.5)* 56_{10} = 100.46 msec

T_D = 100460 µsec + 3.5 µsec≃101 msec

Note: performing time delay has the following disadvantages:

1- Calculating time delay is tedious.
2- µp is occupied waiting the delay loops.
3- Needs accuracy.

However time delay can be generated by using extra chip (e.g. 8254), but at the cost of complexity.

µp Applications With Delay

Ex. (1): **Design an up counter to continuously counting from 0 ⟶ 9_{10} with a delay =0.5 sec between each consecutive numbers, Display the number via o/p 33 H (f=2 MHz) .**

Sol.:

```
Again:  MVI   B, 00
        MOV   A, B
Next:   OUT   33H
        LXI   H, N?
Delay:  DCX   H       6
        MOV   A, L    4
                              } TD=0.5 sec
        ORA   H       4
        JNZ   Delay   10/7
        INR   B
        MOV   A, B
        CPI   OA
        JNZ   Next
        JMP   Again
```

T_D= (6+4+4+10) * ½ * N

N= 0.5 sec / 12

= 41666.6 $_{10}$ ≃ A2C2H (note that To is agnored)

Ex. (2):

Writ a program to generate a sequence waveform with a period of (500) µsec if f= 2 MHz. (used D_0 to output the wave through O/P port 00H).

```
        MVI   D, AA     7T
Next:   MOV   A, D      4T  ⟶
        RLC             4T  ⟶  To alternate D0 from 0 ⟶ 1 , AA ⟶ 55 ⟶ AA ⟶
        MOV   D, A      4T
        ANI   01        7T     Mask D1 ⟶ D7 and display only D0
        OUT   00        10T
        MVI   B, N?     7T
Delay:  DCR   B         4T     } Delay
        JNZ   Delay     10/7 T
        JMP   Next      10
```

$T_D = T_O + T_L$

T_O = (4+4+4+7+10+7+10) * 1/2M = 46* 1/ 2= 23 µsec

T_L = (4+ 10) * 1/ 2M * N= 12 * N µsec

500 µsec= 23 µsec+ (12* N) µsec

N= 39. 75_{10} ≃40_{10}= 28 H

Examples

H.W.
What is the time delay generated by pair of register if it is loaded by: - 00FF, 3E05, A32F?

H.W.
Write a program to generate a time delay equals to (5 msec)?

H.W.: **if Reg. (B) and (C) in the previous example are loaded with 23 H and 84 H respectively, what will be the time delay?**

Reference:

8085 µp architecture and programming_Gon