Lesson Two

8085 IO / M addressing, Machine Cycle & Bus Timing

Lesson Objectives:

- **To determine the machine cycles needed to execute the instructions.**
- **To Draw the bus timing diagram during the execution of the instruction**

Pre Test:

- **Determine the types of machine cycles executed by the 8085 µp.**
- **What is the status of control signals during memory read cycle.**
- **What is the function of ALE.**

8085 memory addressing, I/O addressing

8085 instructions can be classified in following addressing modes

- **Register Addressing mode**

Instructions which have their operands in registers only e.g. MOV, ADD, SUB, ANA, ORA, XRA etc.

- **Immediate Addressing mode**

Instructions in which operand immediately follows the op-code e.g. MVI, LXI, ADI, SUI, ANI, ORI etc.

- **Direct Addressing mode**

Instructions have their operands in memory and the 16-bit memory address is specified in the instruction e.g. LDA, STA, LHLD, SHLD etc.

- **Register Indirect Addressing mode**

Instructions have their operand in memory and the 16-bit memory address is specified in a register pair e.g. LDAX, STAX, PUSH, POP etc.

- **Implicit Addressing mode**

These instruction have their operand implied in the op-code itself e.g. CMA, CMC, STC etc.

8085 machine cycle & bus timing

1. Clock cycle

The speed of a computer processor, or CPU, is determined by the clock cycle, which is the amount of time between two pulses of an oscillator. Generally speaking, the higher number of pulses per second, the faster the computer processor will be able to process information. The clock speed is measured in Hz, typically either megahertz (MHz) or gigahertz (GHz). For example, a 3GHz processor performs 3,000,000,000 clock cycles per second.

Computer processors can execute one or more instructions per clock cycle, depending on the type of processor. Early computer processors and slower processors can only execute one instruction per clock cycle, but faster,

more advanced processors can execute multiple instructions per clock cycle, processing data more efficiently. Each clock cycle is called as T-states.

2. Instruction cycle

The sequence of operations that the CPU has to carry out while execution is called instruction cycle.

1:- Read an Instruction

2:- Decode the instruction

3:- Find the address of operand

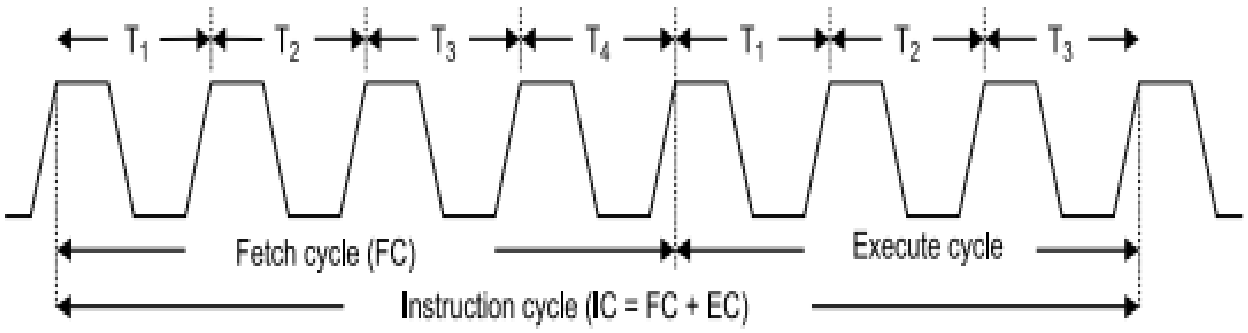
4:- retrieve an operand

5:- perform desired operation

6:- find the address of destination

7:- store the result into the destination

TimingDiagram:



Where, Instruction cycle= Fetch Cycle(FC) (and decode the opcode) + Execute cycle(EC).

Performing each cycle needs performing one or more of the machine cycle.

3. Machine cycle:

The steps performed by the computer processor for each machine language instruction. The four common machine cycles are:-

A. Opcode Fetch - Retrieve an instruction code from the memory.

B. Memory Read (MR) - Retrieve the operand from the memory.

C. Memory Write (MW) - Send the result to the memory Store.

D. Input_Output Read (I/O R) - Read the operand from the Input port.

E. Input_Output Write (I/O W) - Send the operand from the Input port.

Timing Diagram

Representation of Various Control signals generated during Execution of an Instruction. Following Buses and Control Signals must be shown in a Timing Diagram:

Higher Order Address Bus.

Lower Address/Data bus

ALE

RD

WR

IO/M

Opcode fetch:

The microprocessor requires instructions to perform any particular action. In order to perform these actions microprocessor utilizes Opcode which is a part of an instruction which provides detail (i.e. which operation µp needs to perform) to microprocessor.

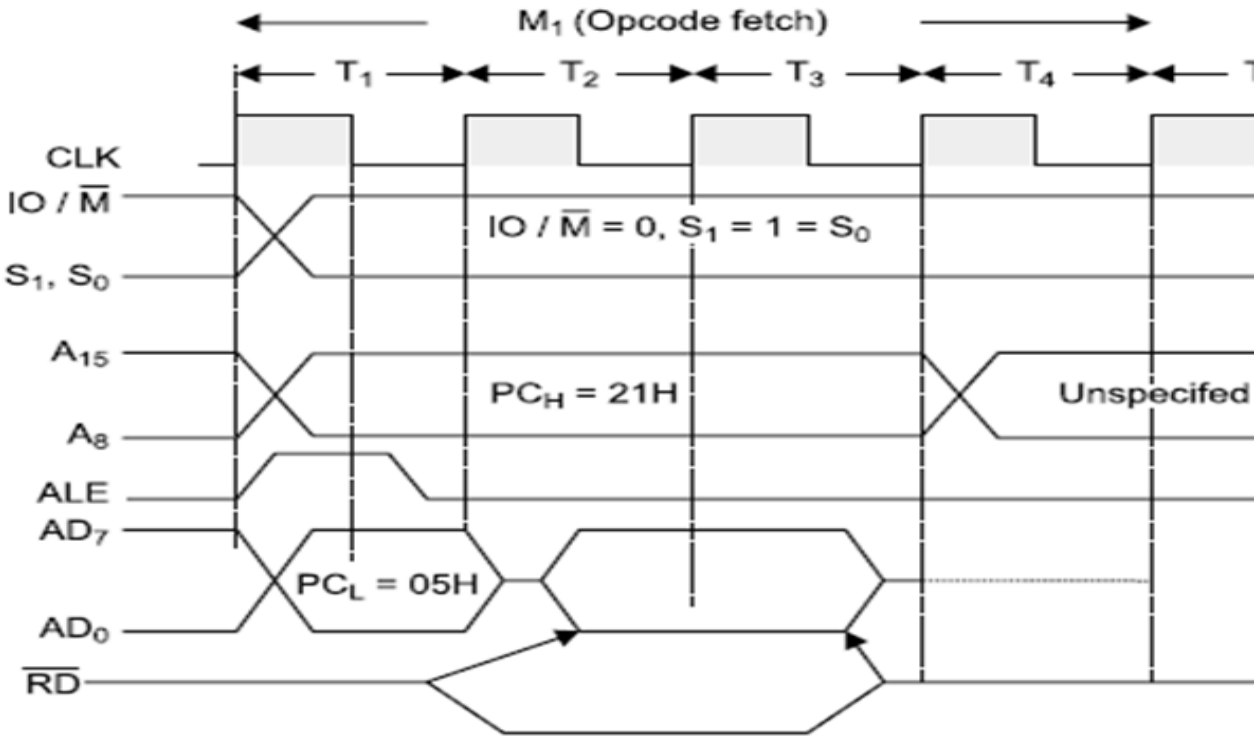


Figure (2): Opcode fetch timing diagram

Operation steps:

1- During T1 state, $IO/\overline{M}$, S_0, S_1 signals are used to instruct microprocessor to fetch opcode. Thus when $IO/\overline{M}$=0, S0=S1= 1, it indicates opcode fetch operation. During this operation 8085 transmits 16-bit address and also uses ALE signal for address latching. A8-A15 contains higher byte of address and lower byte of address A0-A7 is selected from AD0-AD7.

2- At T2 & T3 state, microprocessor uses read signal and make data ready from that memory location to read opcode from memory. Address is removed from AD0-AD7 and data D0-D7 appears on AD0-AD7.

Microprocessor reads opcode and stores it into instruction register to decode it further.

3- During T4 microprocessor performs internal operation like decoding opcode and providing necessary actions.

Read and write timing diagram for memory and I/O Operation

Memory Read:

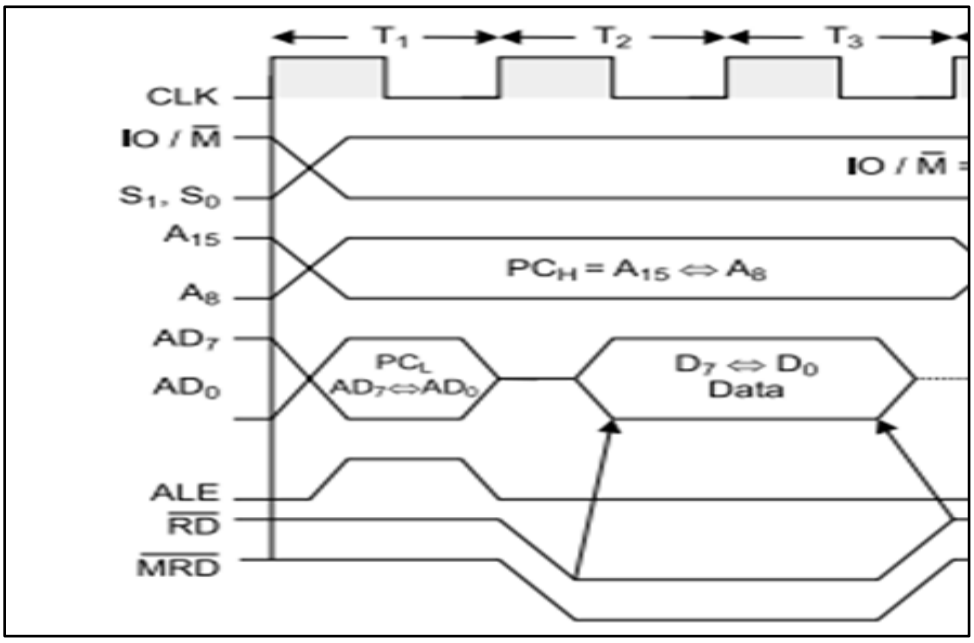


Figure (3): Memory read timing diagram

Operation steps:

1- It is used to fetch one byte from the memory.

2- It requires 3 T-States.

3- It can be used to fetch operand or data from the memory.

4- During T1, A8-A15 contains higher byte of address. At the same time ALE is high. Therefore Lower byte of address A0-A7 is selected from AD0-AD7.

5- Since it is memory ready operation, $IO/\overline{M}$ goes low.

6- During T2 & T3, ALE goes low, $\overline{RD}$ goes low. Address is removed from AD0-AD7 and data D0-D7 appears on AD0-AD7.

Memory Write:

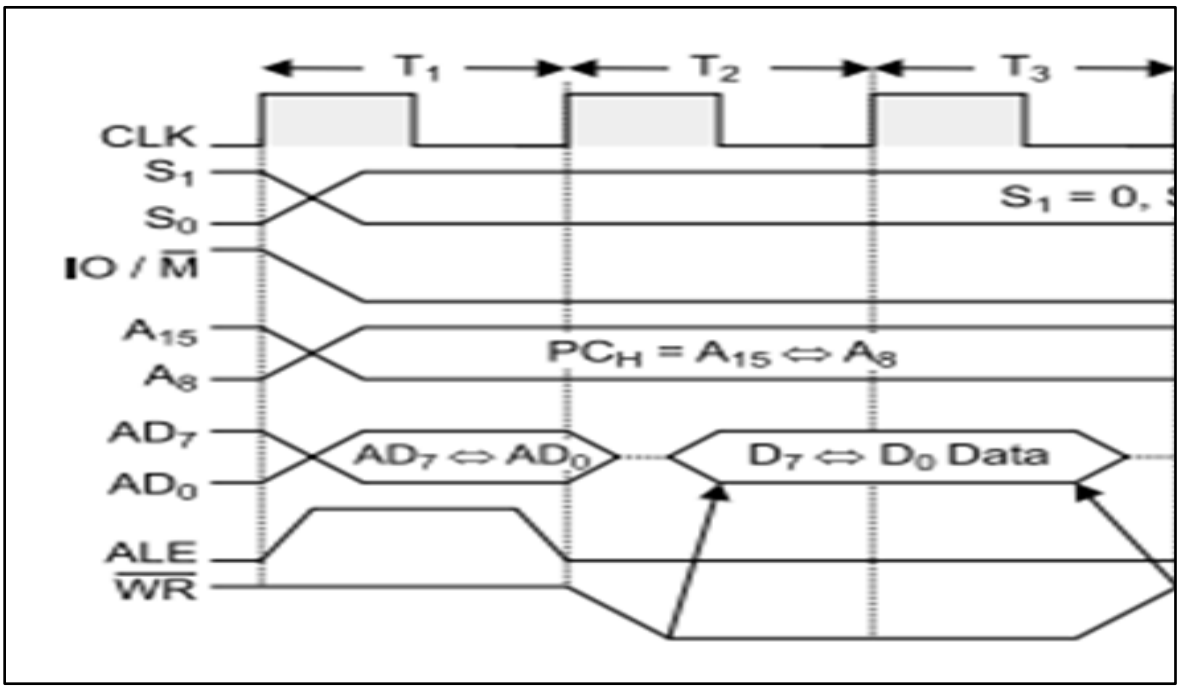


Figure (4): Memory write timing diagram

Operation:

1- It is used to send one byte to memory.

2- It requires 3 T-States.

3- During T1, ALE is high and contains lower address A0-A7 from AD0-AD7.

4- A8-A15 contains higher byte of address.

5- As it is memory operation, $IO/\overline{M}$ goes low.

6- During T2 & T3, ALE goes low, $\overline{WR}$ goes low and Address is removed from AD0-AD7 and then data appears on AD0-AD7.

I/O Read:

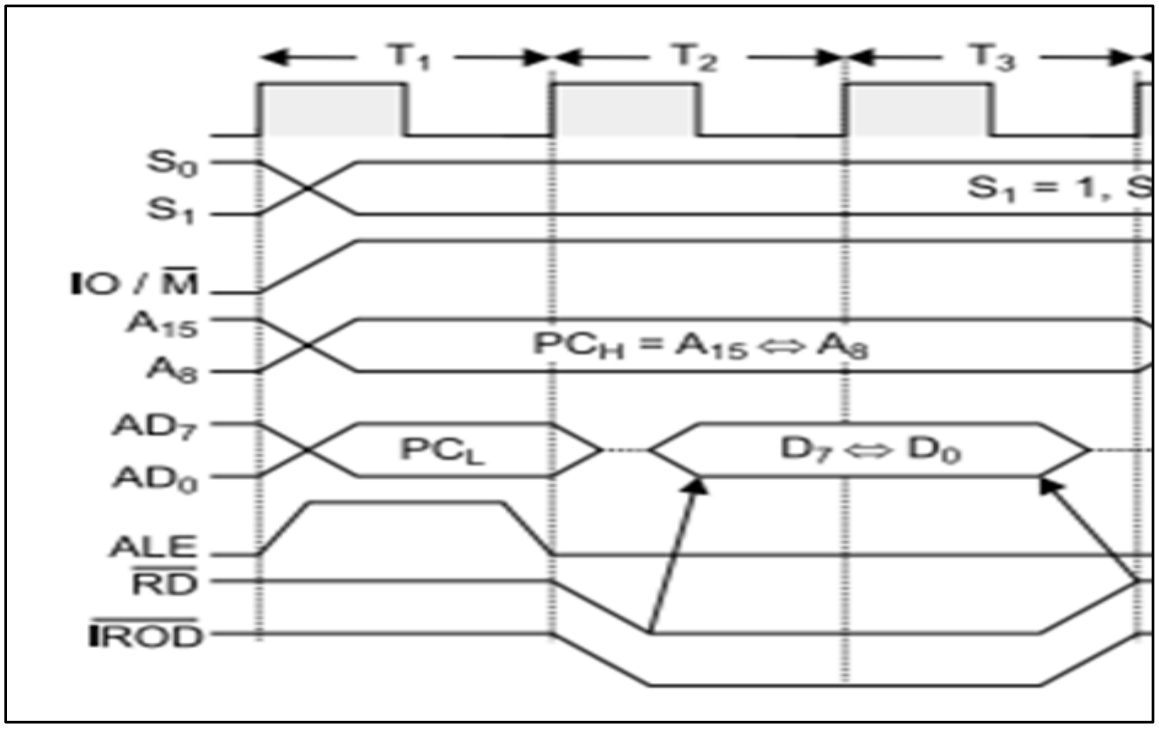


Figure (5): I/O Read timing diagram

Operation:

1- It is used to fetch one byte from an IO port.

2- It requires 3 T-States.

3- During T1, The Lower Byte of IO address is duplicated into higher order address bus A8-A15.

4- ALE is high and AD0-AD7 contains address of IO device.

5- $IO/\overline{M}$ goes high as it is an IO operation.

6- During T2 & T3, ALE goes low, $\overline{RD}$ goes low and data appears on AD0-AD7 as input from IO device.

IO Write:

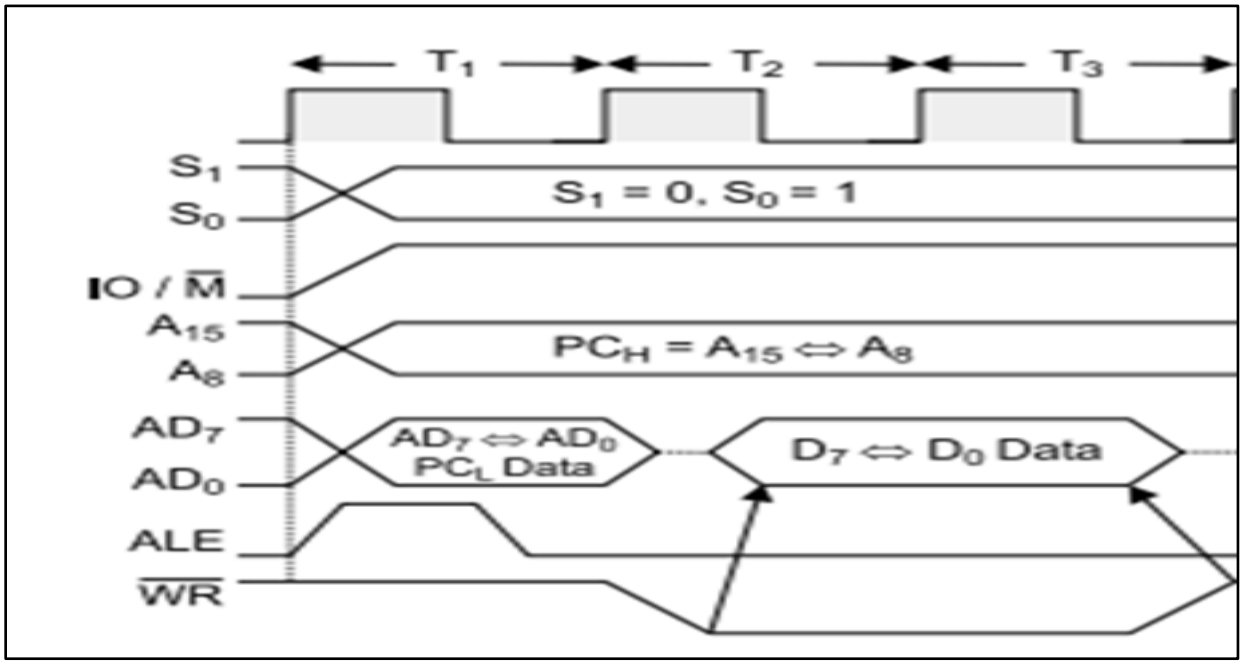


Figure (6): I/O Write timing diagram

Operation:

1- It is used to writ one byte to the IO device.

2- It requires 3 T-States.

3- During T1, the lower byte of address is duplicated into higher order address bus A8-A15.

4- ALE is high and A0-A7 address is selected from AD0-AD7.

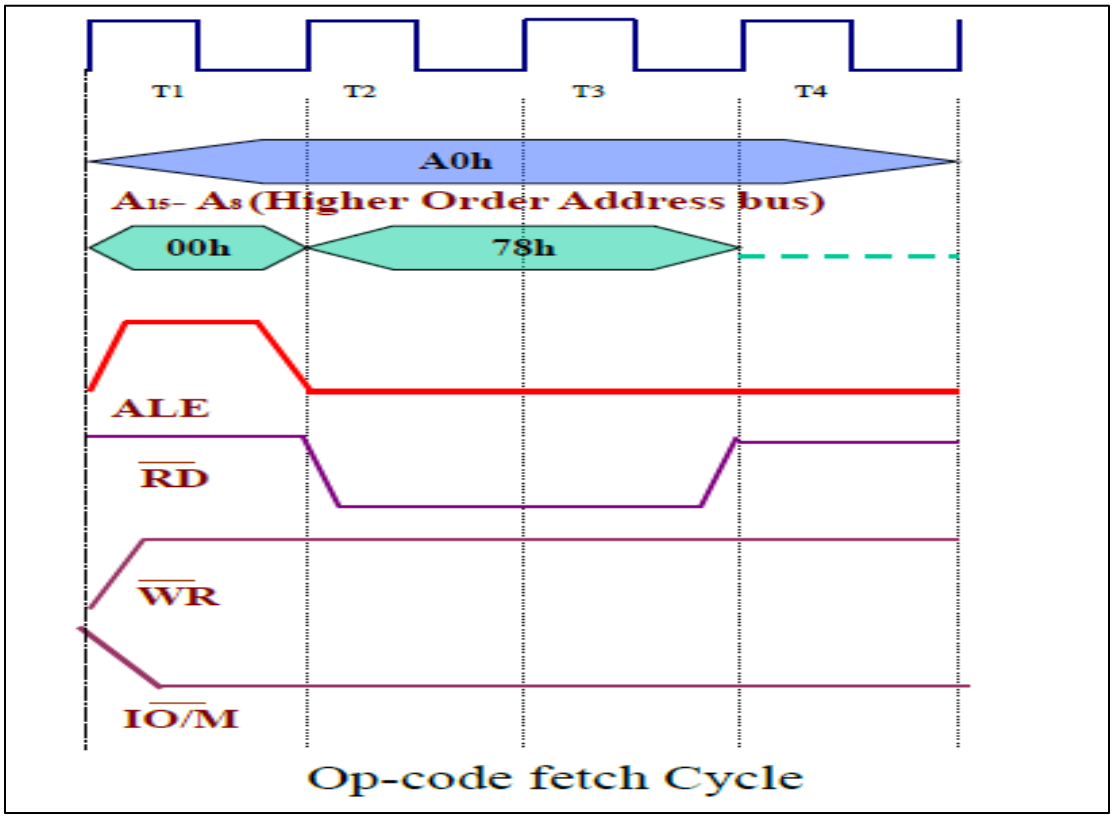
5- As it is an IO operation $IO/\overline{M}$ goes high.

6- During T2 & T3, ALE goes low, $\overline{WR}$ goes low and data appears on AD0-AD7 to write data to the IO device.

Examples

1. A000 MOV A,B 78

(1 Byte instruction, 1 machine cycle == opcode fetch == 4T state)



This 1 byte instruction and needs 1 machine cycle (opcode fetch). During T1, the content of the program counter (PC) is placed on the A8-A16 and AD1-AD7 as ALE goes high. During T2 & T3 of op code fetch cycle (M1), the op code of the instruction is loaded in the instruction register (IR). The T4-state of this cycle M1 is for decoding and the contents of B is copied in A.

2. A000 MOV A,M 7E

This 1 byte instruction which needs 2 machine cycle (opcode fetch and MR). During T1, the content of the program counter (PC) is placed on the A8-A16 and AD1-AD7 as ALE goes high. During T2 & T3 of op code fetch cycle (M1), the op code of the instruction is loaded in the instruction register (IR). The T4-state of this cycle M1 is for decoding. . During the T1-state of second machine cycle M2, the contents of H-L pair are

placed on the address and address data bus. As usual during this state ALE sends a high pulse. During T2 and T3 states of machine cycle M2, contents of memory location are transferred (copied) to the specified register

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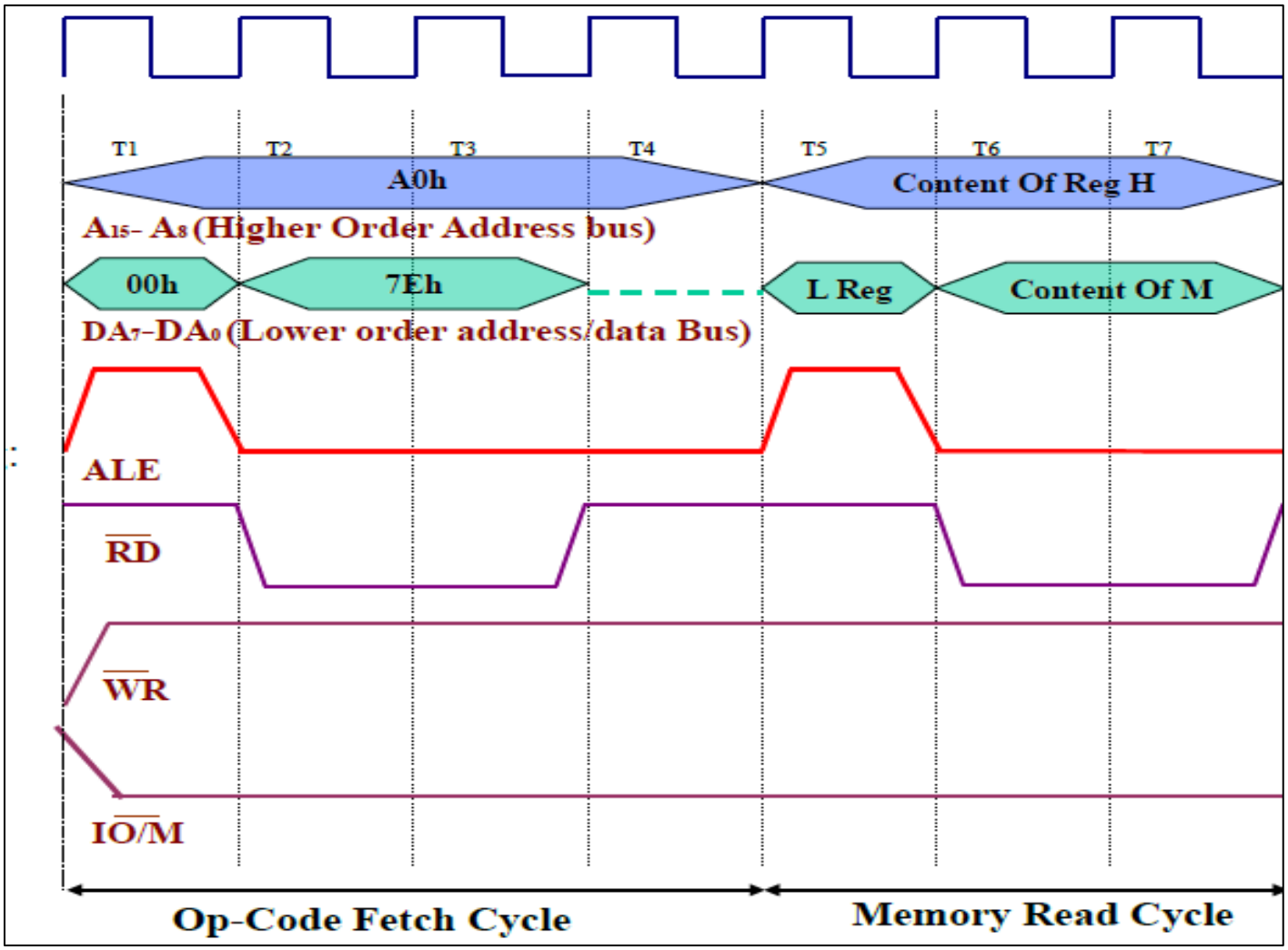


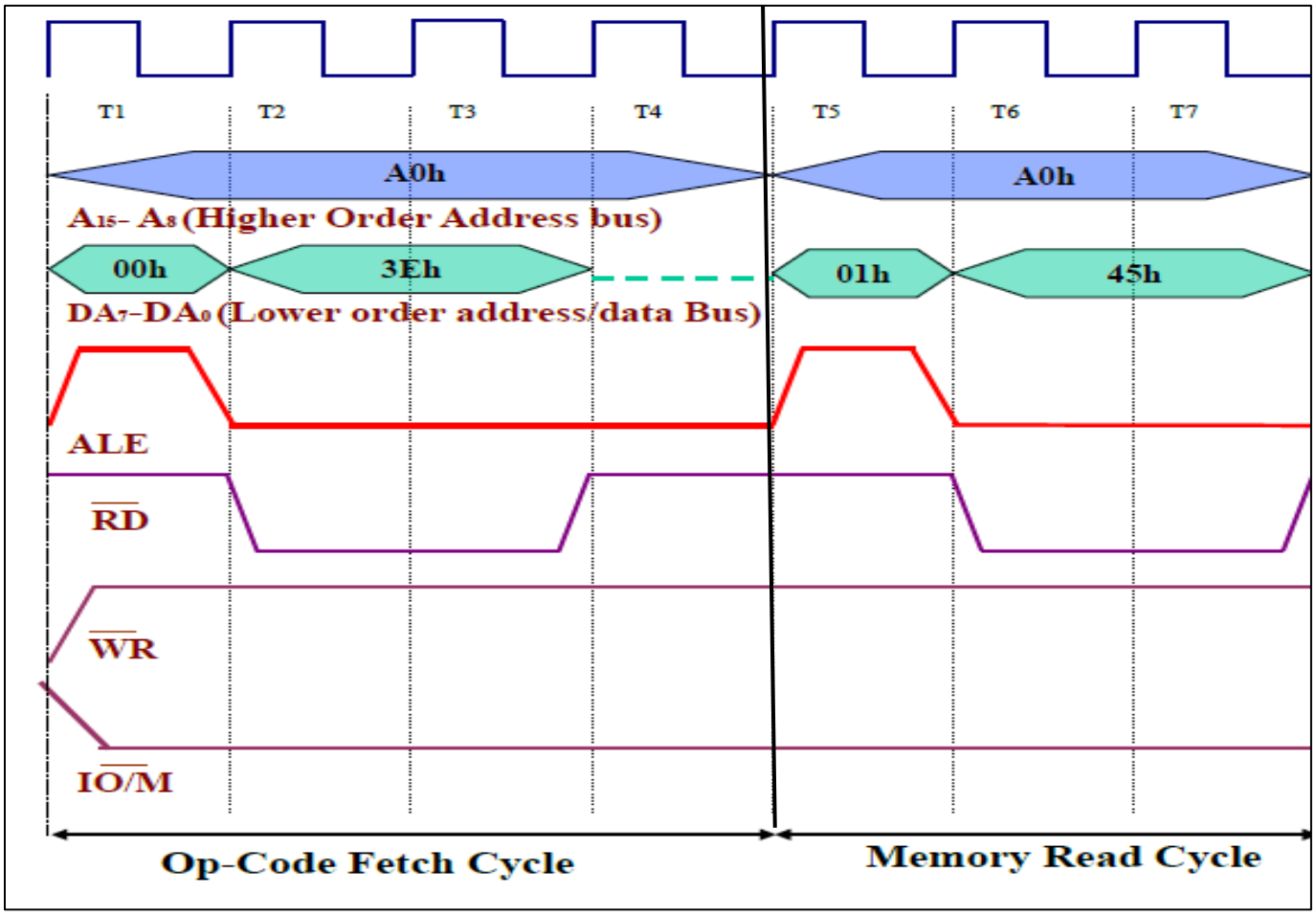
3. MVI A, 77 (2byte instruction , 2 machine cycle== (opcode fetch +1 MR) == 7T state

A000 3E

A001 77

This is an immediate move instruction. It is two byte instruction; one byte is used for the op code of the instruction and the other byte is used for the data. During T1, the content of the program counter (PC) is placed on the A8-A16 and AD1-AD7 as ALE goes high. During T2 & T3 of op code fetch cycle (M1), the op code of

the instruction is loaded in the instruction register (IR). The T4-state of this cycle M1 is for decoding. In the second machine cycle M2, the contents of the program counter (PC) is placed on the A8-A16 and AD1-AD7 during its T1 state. This is the address of the second byte. During T2 of M2 cycle, the PC is incremented. At the same time memory is accessed and immediate read data is loaded to the specified register during T3-state of M2 machine cycle. This instruction takes two machine cycles with 7 T-states.

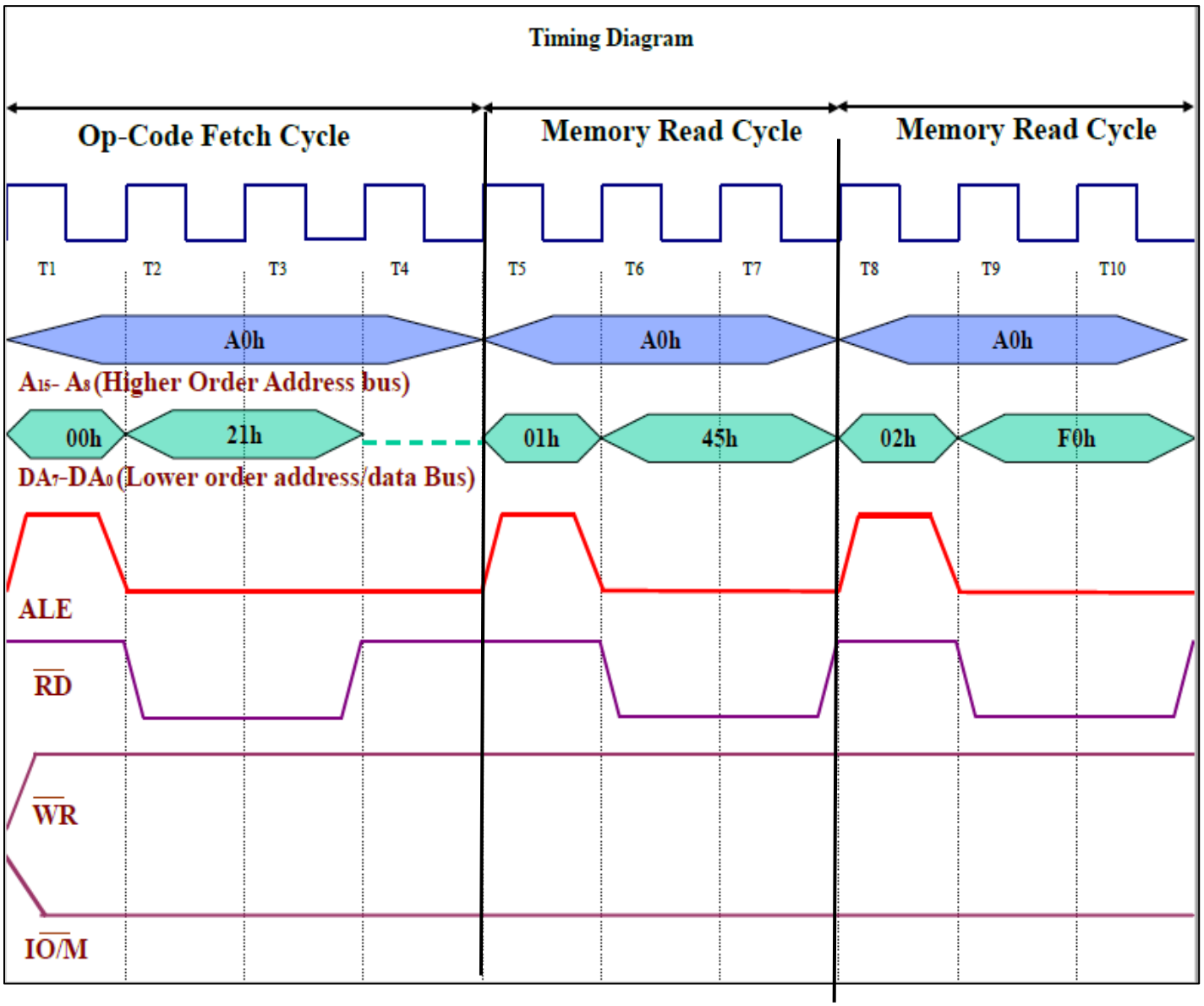


4. A000 LXI H, F045 21

A0001 45

A002 F0

This a three bytes instruction, which needs 3 machine cycle (opcode fetch + MR+MR). Each machine cycle is performed as previously discussed.



H.W.: For the following program , complete the table to determine the total instruction cycle time and the program processing time, if F= 2MHz. Draw the trimming diagram for each instruction.

M.L.	Instruction	Machine cycle	T state	RD WR	S0 S1 IO/M	Time (μsec)
2000	MOV B,A					
2001	MVI A, FF					
2003	LXI H, 2060					
2006	MOV M,B					

Exercises:

EX.1

6. The function of ALE is----------

7. RD signal will be ----------during MEMR cycle, while IO/M will be---------- .

8. OPcode fetch needs ---------- T states.

9. The demultiplexing between address and data bus will occurs at -------- T states.

10. The time required to execute CMA is--------.

EX.2

Draw the bus timing diagram during the execution of SHLD, ADI 88, OUT 20.

Reference:

8085 μp architecture and programming_Gonkar