Lesson Four

8085 Memory map

Lesson Objectives:

- **To determine the addresses range for each memory chip**
- **To draw the memory map**
- **To design a system the fulfills the requirements.**

Pre Test:

- **Define the memory map**
- **Illustrate the Basic concept in memory interfacing.**
- **How many address lines needed to address 2048 bytes of memory.**

Memory map

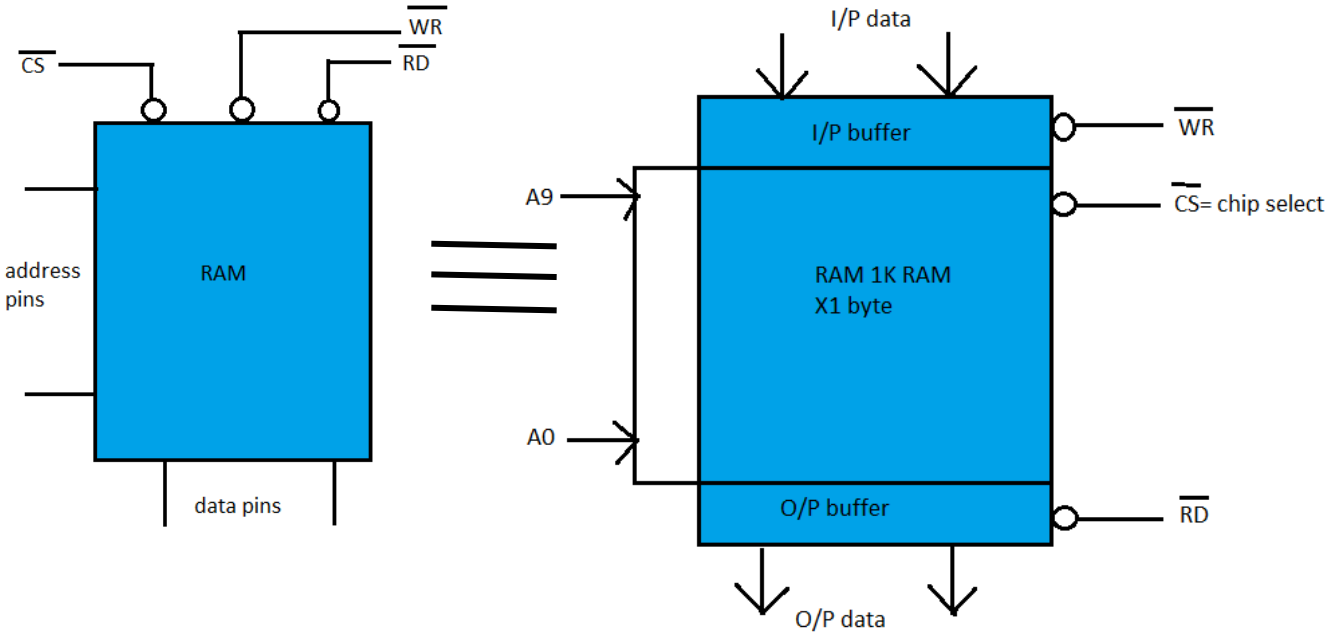
It is a pictorial representation in which memory devices are located in the entire range of addresses

Memory addresses: provide the location of various memory devices in the system.

- The interfacing logic defines the range of memory addresses of each memory device.

Memory interfacing:

- Typical memory chip



Basic concept in memory interfacing:

1. Select the chip (higher order address to activate **cs**)
2. Identify the memory location (low order address to enable the F/F)
3. Enable the I/P buffer (using WR) OR O/P buffer (using RD)

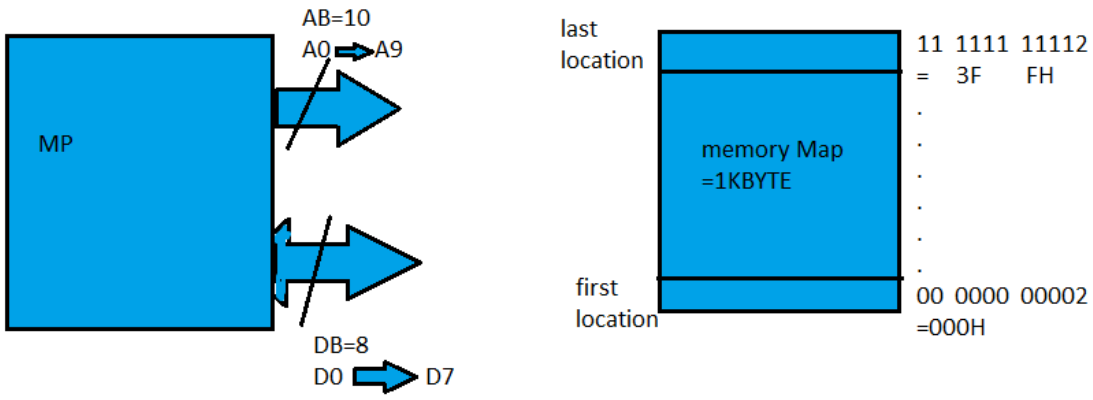
To interface the memory with MP:

1. Connect the low order of AB to the address pins of memory chip.

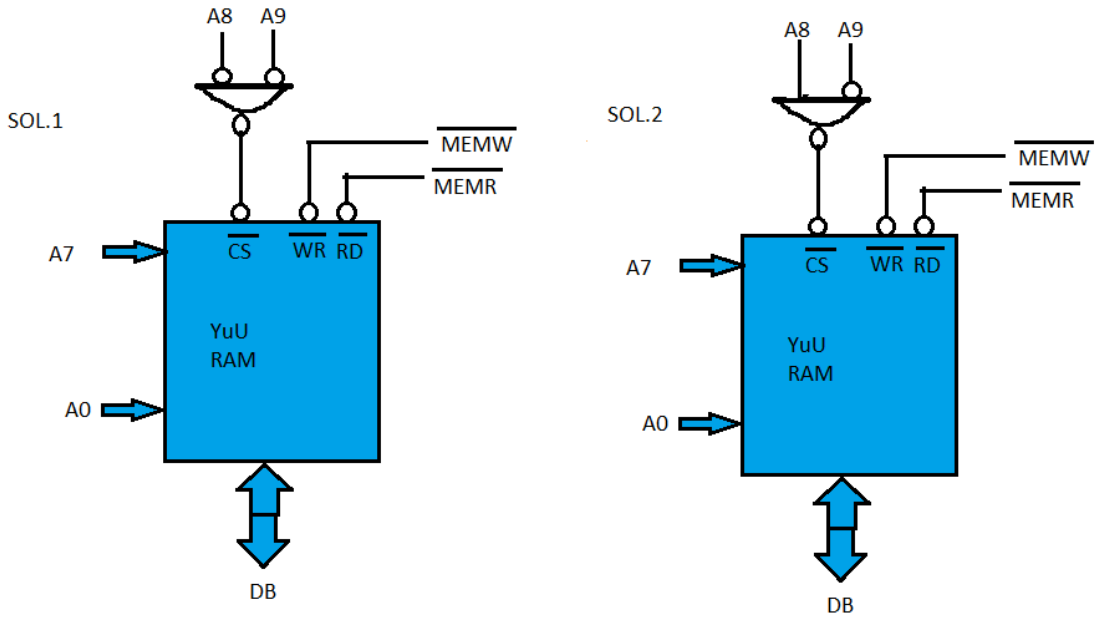
2. Decode the higher AB to generate unique address to the memory chip which activate the **CS**

3. Generate the control signals MEMR & MEMW by combining **RD** , **WR** with IO/M

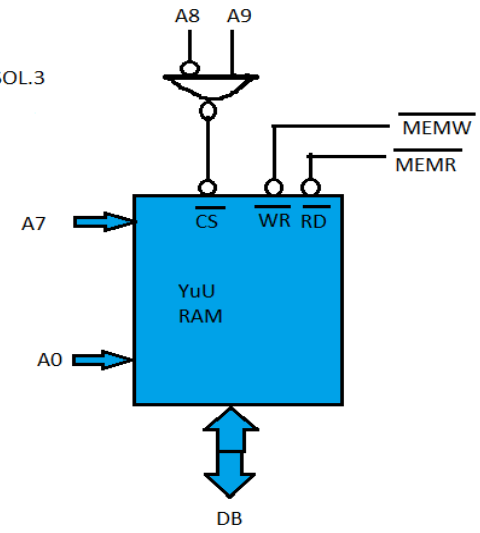
Ex(1) :Design a cct. That connect ¼ k of RAM chip to a µP with AB= 10 bits , DB=8 bits. Draw the memory map.



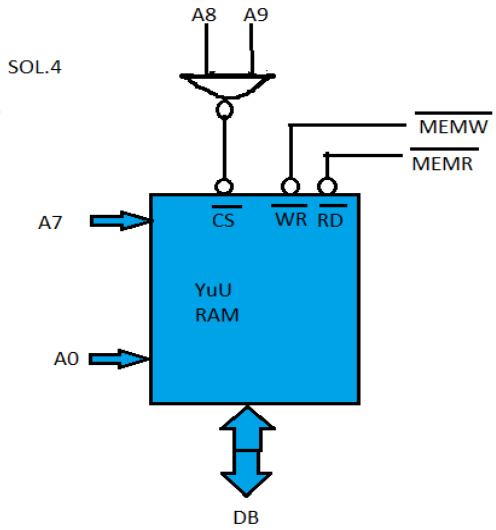
SOL.



SOL.3

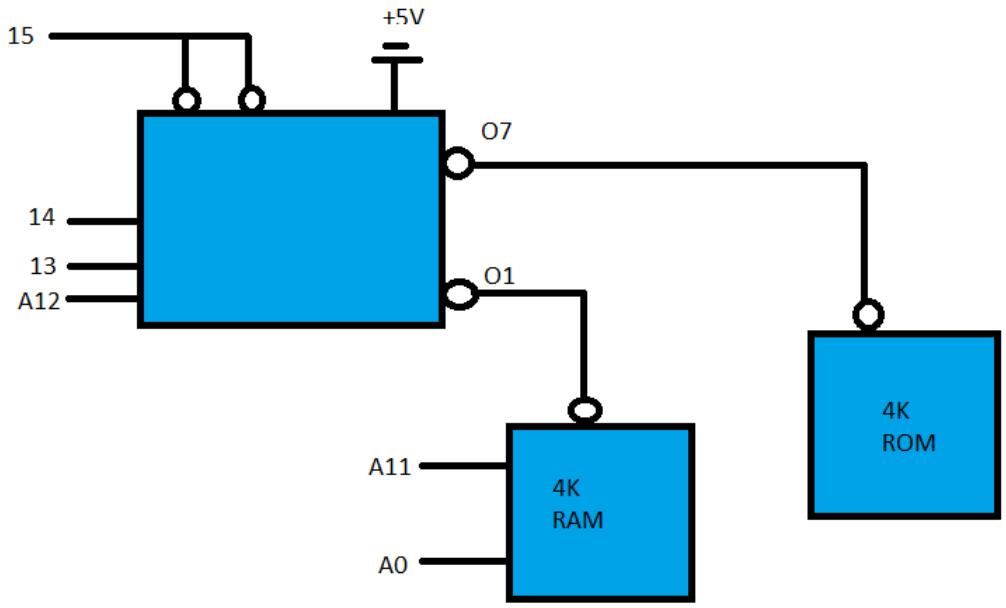


SOL.4



						High order						Low order				
						A_9	A_8	A_7	A6	A_5	A_4	A_3	A_2	A_1	A_0	
Sol1	O	O	O	H	=	0	0	0	0	0	0	0	0	0	0	1st
	O	F	F	H	=	0	0	1	1	1	1	1	1	1	1	Last location
Sol2	1	O	O	H	=	0	1	0	0	0	0	0	0	0	0	
	1	F	F	H	=	0	1	1	1	1	1	1	1	1	1	
Sol3	2	O	O	H	=	1	0	0	0	0	0	0	0	0	0	
	2	F	F	H	=	1	0	1	1	1	1	1	1	1	1	
Sol4	3	O	O		=	1	1	0	0	0	0	0	0	0	0	
	3	F	F		=	1	1	1	1	1	1	1	1	1	1	

Ex: What will be the range of address & foldback space if exist for each memory chip.



1. Replace 4 K RAM by 1 K SRAM

   $A_{11}A_{10}$= XX

2. Replace 4 K ROM by 512 ROM

   $A_{11}A_{10}A_9$ = XXX

3. Replace A_{12} by A_{15}
4. Connect E1 & E2 to ground
5. Exchange CS of RAM to O_5
6. Connect E_3 to A_{15}
7. Connect 4K ⟶ 2K with linear decode

Ex (2): For the same cct in Ex1, find the range of addresses, fold back space & type of decoding for each memory chip if:

A) Connect E_3 to Vcc

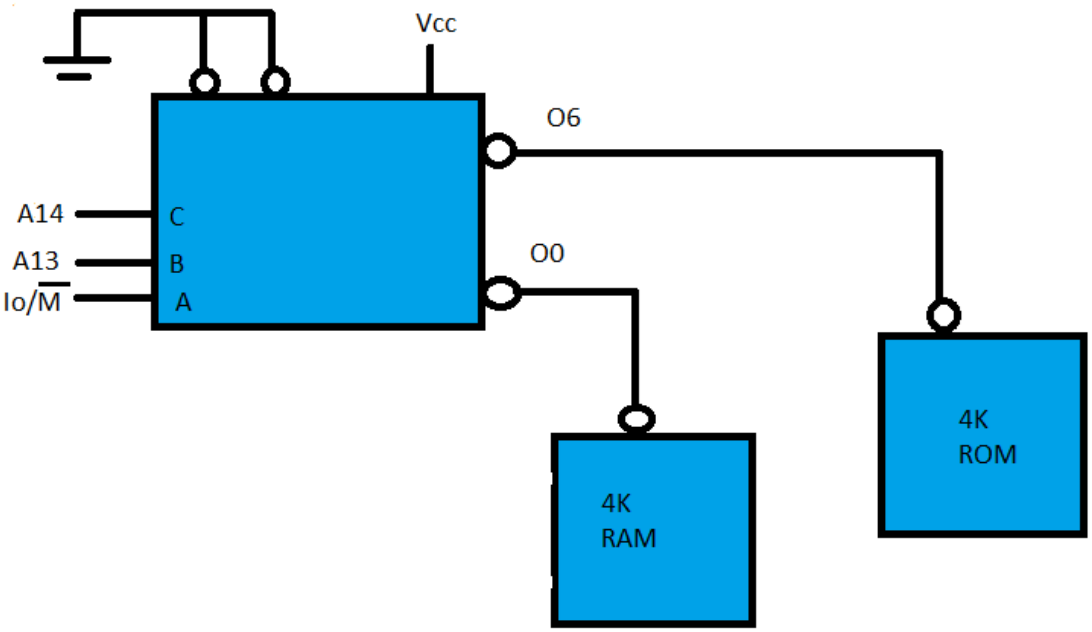
B) Can we connect I0/M to E3 and RD , WR pins of each chip to RD & WR signal?

C) Replace RAM by 2K RAM

D) Replace ROM by 1 K EPROM

E) Connect A to Vcc and eliminate A_{12}.

F) For the same ROM of addresses in Ex1, modify the cct while connecting E3 to A15. So that RAM the range of ram addresses equals to C000 ~~CFFF~~



Reference:

8085 µp architecture and programming_Gonkar