جامعة المستقبل

نحو جامعة مستدامة

Al-Mustaqbal University - College of engineering
Department of computer engineering

Second stage

Lecture Week 10
"Shift-registers (bidirectional , shift register counter)"

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2025

Objectives Overview

By the end of this lecture, students will be able to

- Understand the Structure and Operation.
- Describe how data shifts left or right based on control signals.
- Differentiate Shift Directions. Identify use cases for left-shift, right-shift, and bidirectional shifting.
- Demonstrate the effect of shift direction on data flow.
- Apply in Digital Systems, Design and implement bidirectional shift registers using flip-flops or simulation tools.
- Analyze their role in applications such as data conversion, communication systems, and arithmetic operations.

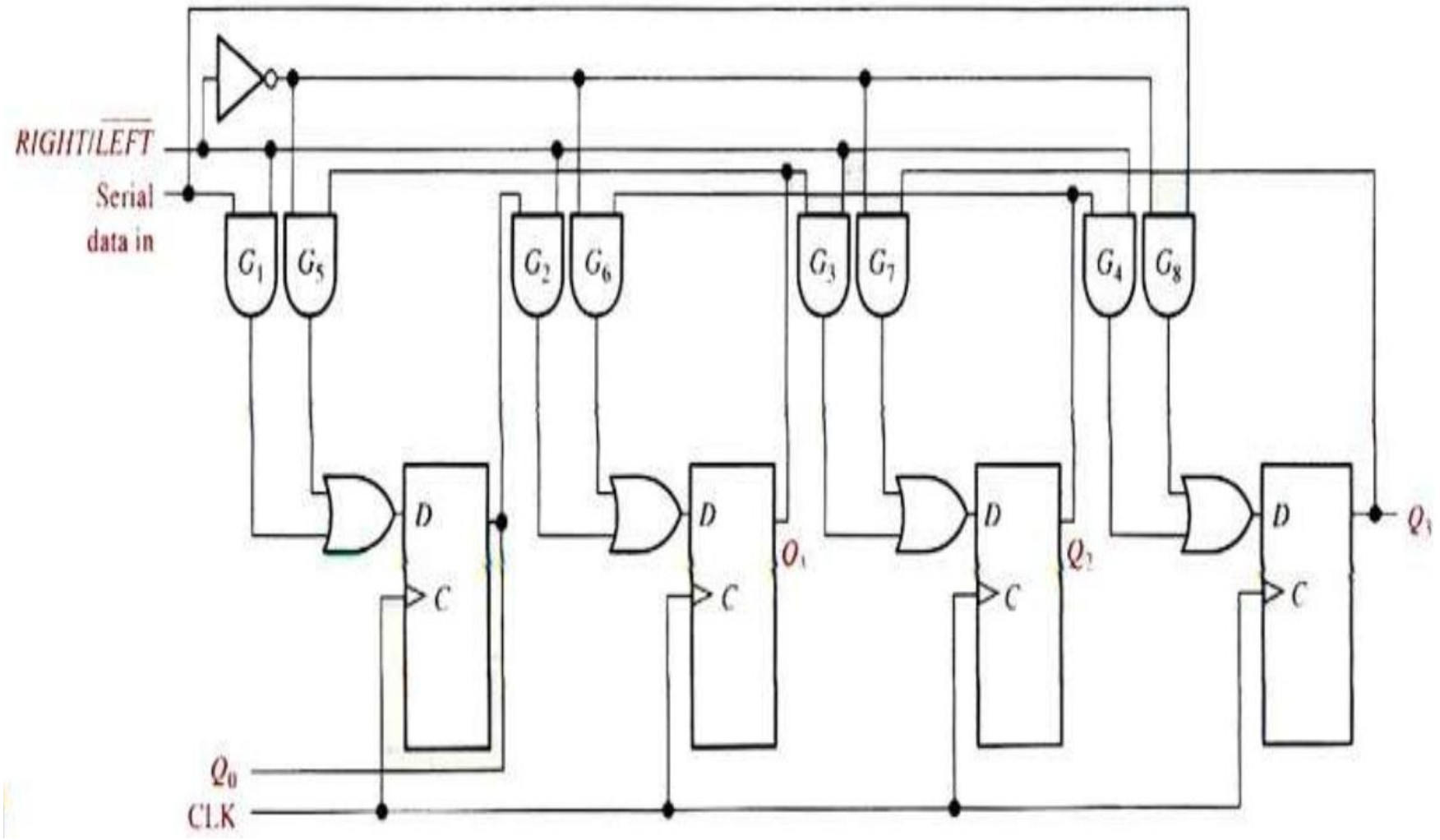
Digital Circuits - bidirectional Shift Registers

1. Bidirectional shift registers
2. Shift Register Counters
3. Shift Register Applications
4. Logic Symbols with Dependency Notation

Bidirectional shift registers

A bidirectional shift register is one in which the data can be shifted either left or right. A HIGH on the RIGHT/LEFT' control input allows data bits inside the register to be shifted to the right, and a LOW enables data bits inside the register to be shifted to the left. When the RIGHT/LEFT' control input is HIGH, gates G1 through G4 are enabled, and the state of the Q output of each flip-flop is passed through the D input of the following flip-flop. When a clock pulse occurs, the data bits are shifted one place to the right. When the RIGHT/LEFT' control input is LOW, gates G5 through G8 are enabled, and the Q output of each flip-flop is passed through to the D input of the preceding Flip-flop. When a clock pulse occurs, the data bits are then shifted one place to the left.

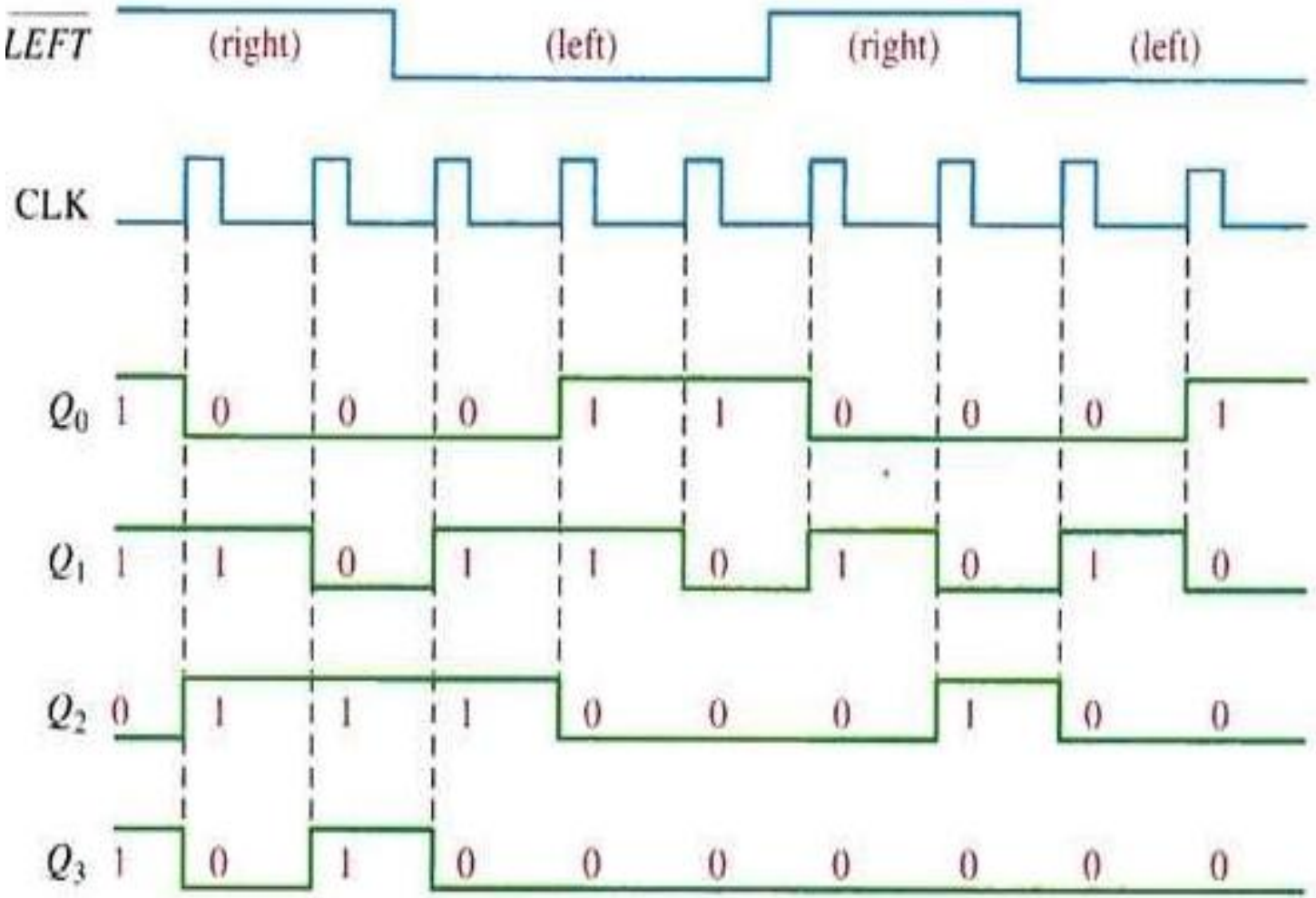
Four-bit bidirectional shift register



Example 1

1011=> Q0=1, Q1=1, Q2=0, Q3=1

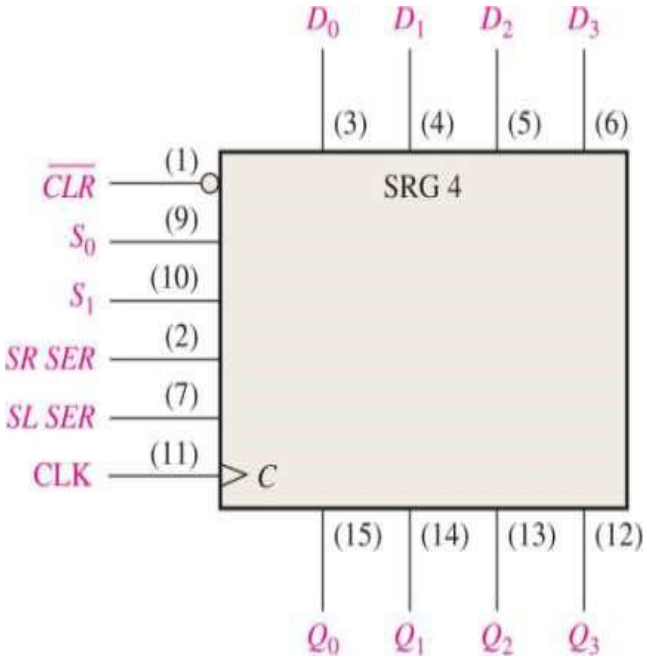
Right/



Example 2

The 74HC194 4-bit bidirectional universal shift register.

A universal shift register has both serial and parallel input and output capability.



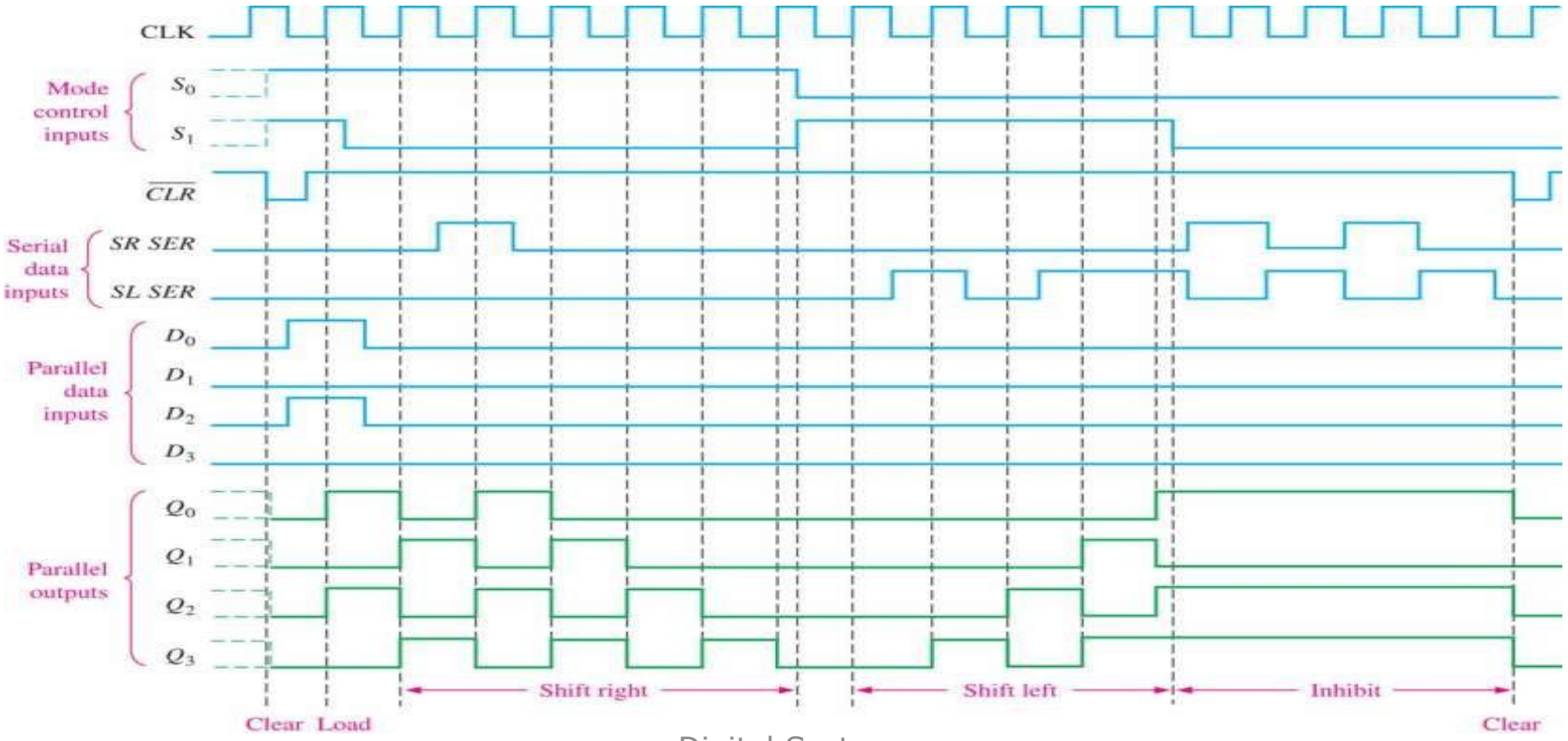
S0	S1	mode
1	1	load
1	0	Shift right
0	1	Shift left
0	0	Inhibit (NC)

74HC194 shift register

Synchronous parallel loading with the positive transition of the clock and a HIGH to the S0 and S1 inputs. Clear is asynchronous input

SR SER: shift right serial input **SL SER: shift left serial input**

Sample timing diagram



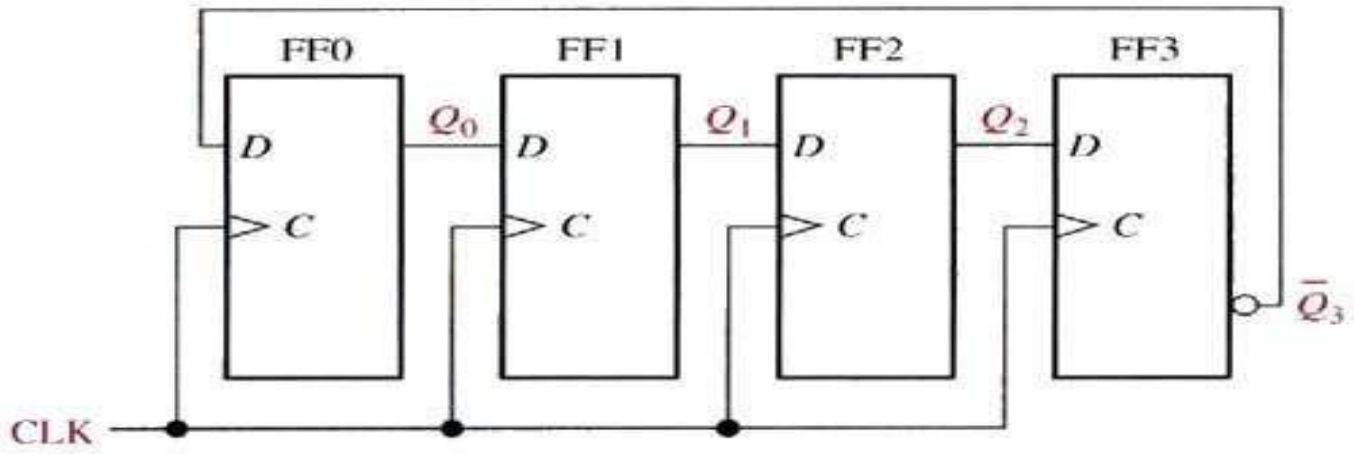
A shift register counter is basically a shift register with the serial output connected back to the serial input to produce special sequence. These devices are often classified as counters because they exhibit a specified sequence of states. Two of the most common types of shift register counters, the Johnson counter and the ring counter.

The Johnson Counter: -

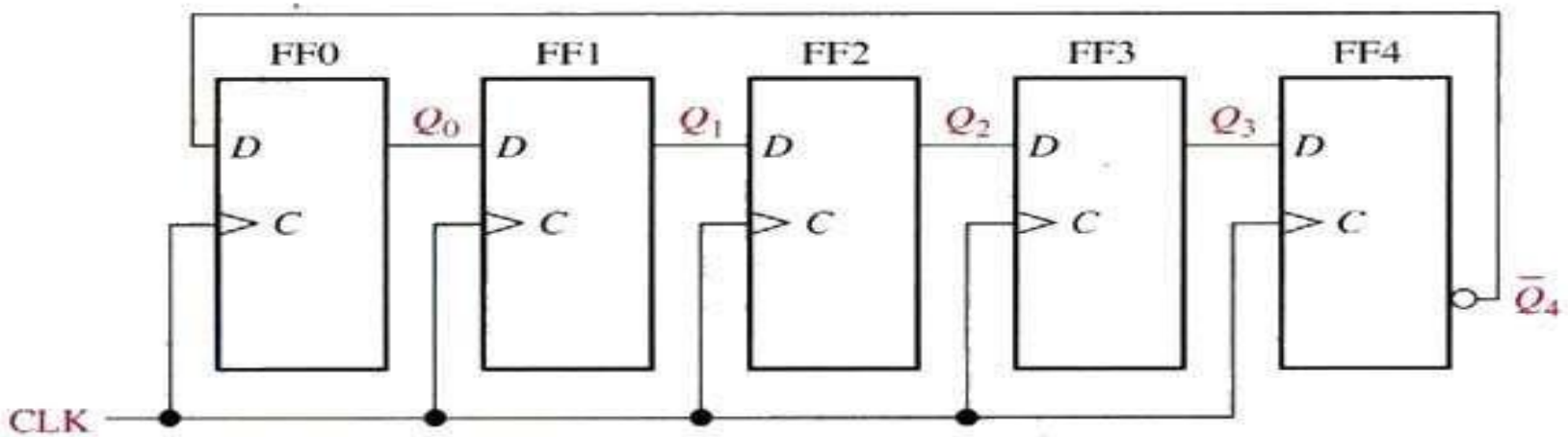
The complement of the output of the last flip-flop is connected Back to the D input of the first flip-flop. This feedback arrangement produces a characteristic sequence of states. In general, a Johnson counter will produce a modulus of 2n, where n is the number of stages in the counter.

CLOCK PULSE	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Four and Five – bit Johnson counter



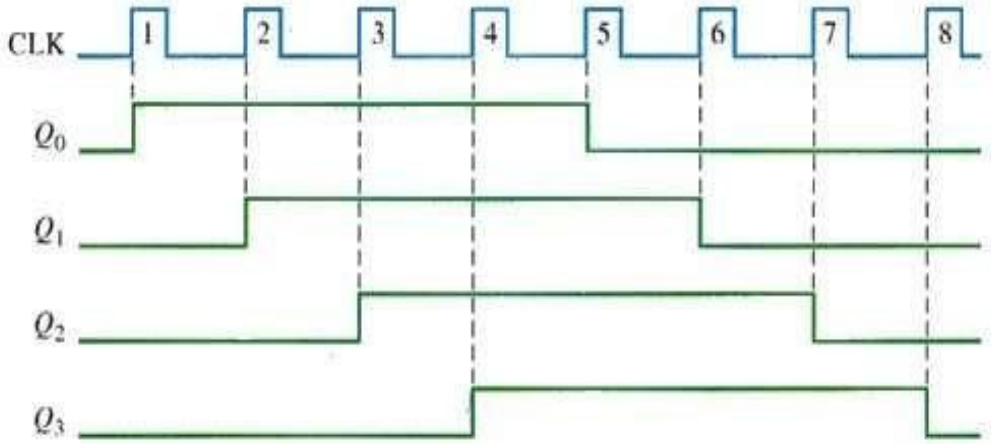
(a) Four-bit Johnson counter



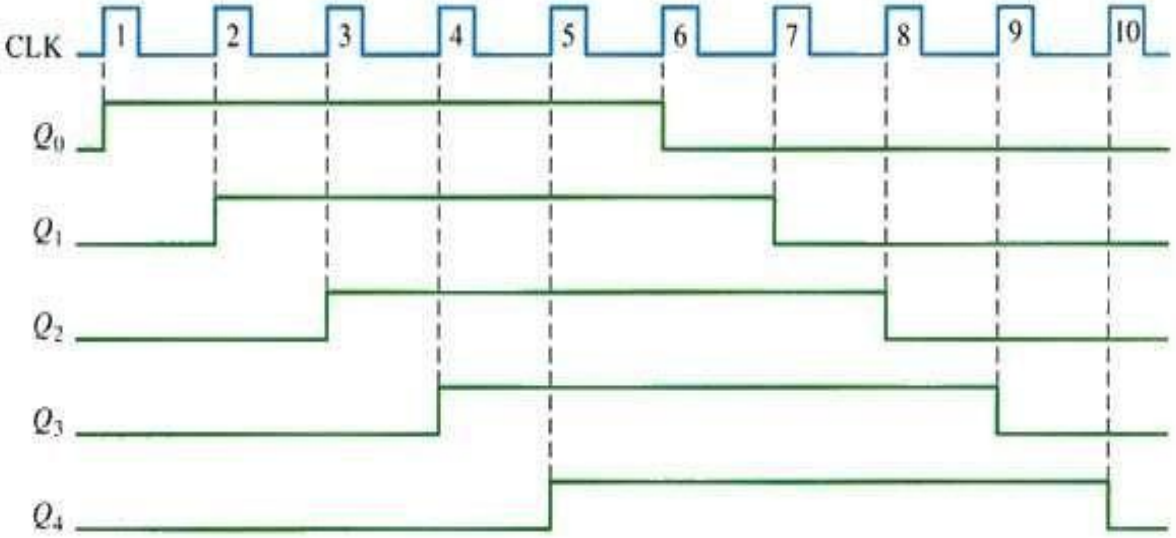
(b) Five-bit Johnson counter

Timing sequence for Johnson counter

Timing sequence for a 4-bit Johnson counter.



Timing sequence for a 5-bit Johnson counter.



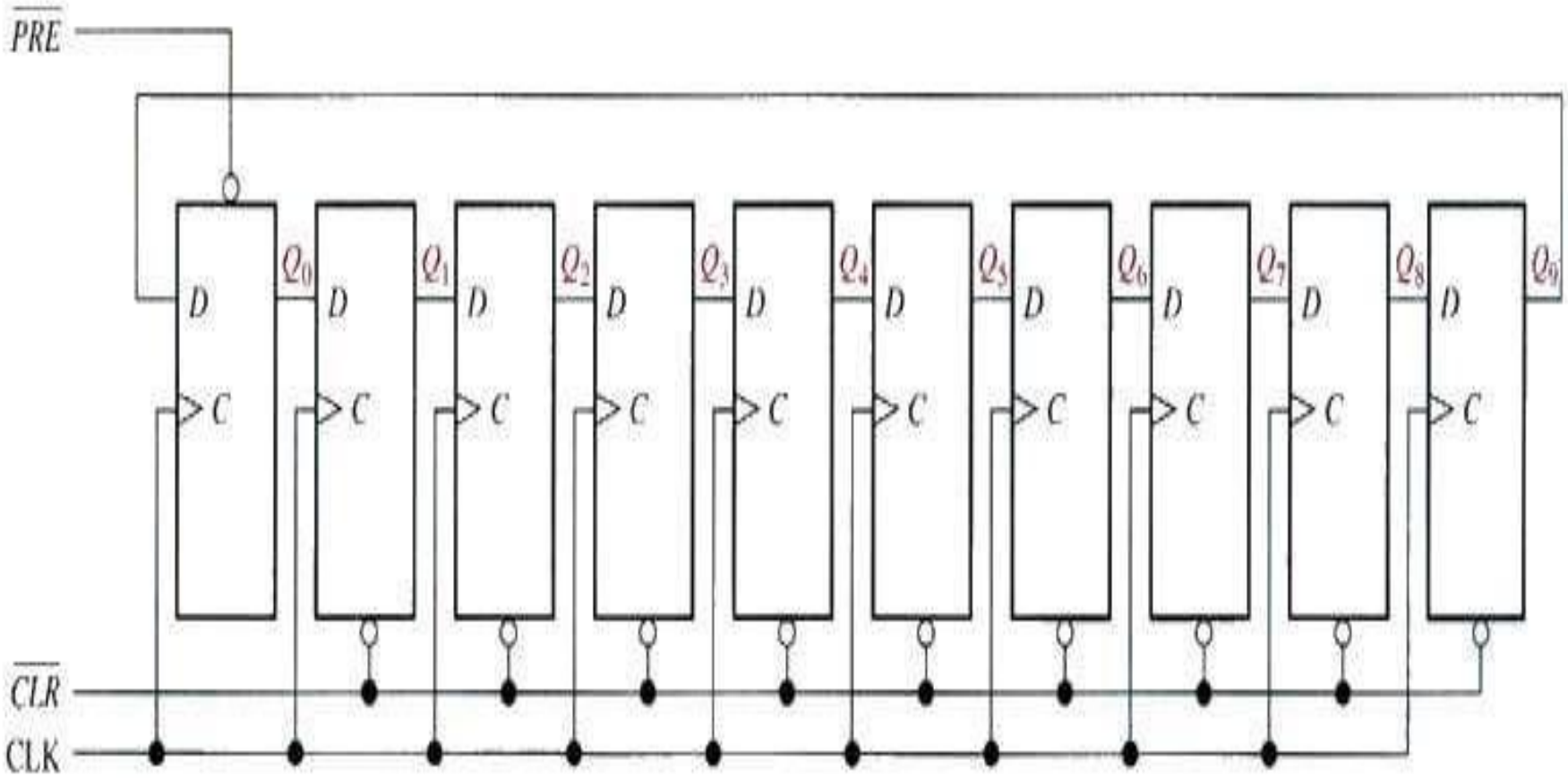
Ring Counter

The ring counter utilizes one flip-flop for each state in its sequence. It has the advantage that decoding gates are not required. In the case of a 10-bit ring counter. There is a unique output for each decimal digit. The sequence for the ring counter . Initially, a 1 is present into the first flip-flop and the rest of the flip-flop are cleared. The ten outputs of the counter indicates directly the decimal count of the clock pulse, for instance, a 1 on Q0 represents a zero, a 1 on Q1 represents a one, a 1 Q2 represents a two, a 1 on Q2 represents a three, and so on. You should verify that the 1 is always retained in the counter and simply shifts “around the ring” advancing one stage for each clock pulse

CLOCK PULSE	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

A 10-bit ring counter

Q9 is fed back to the D input of the first stage.

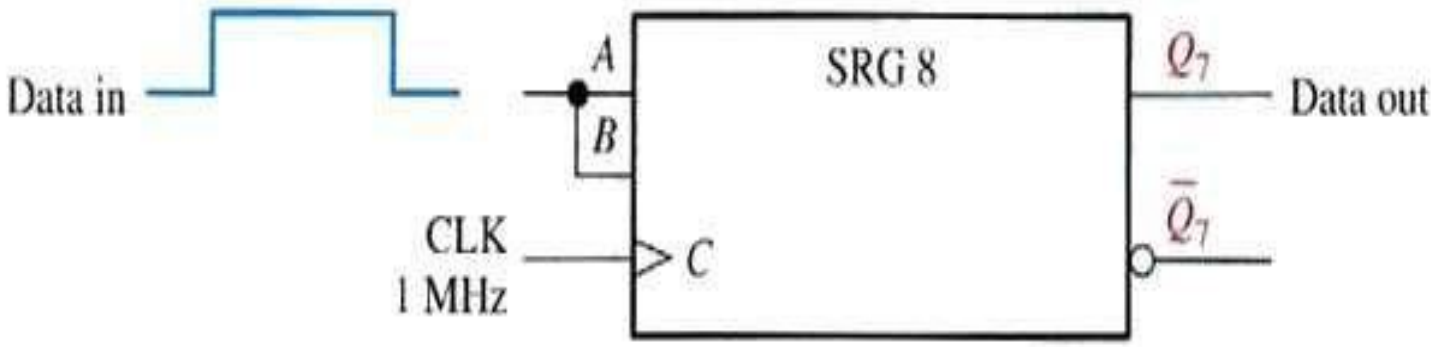


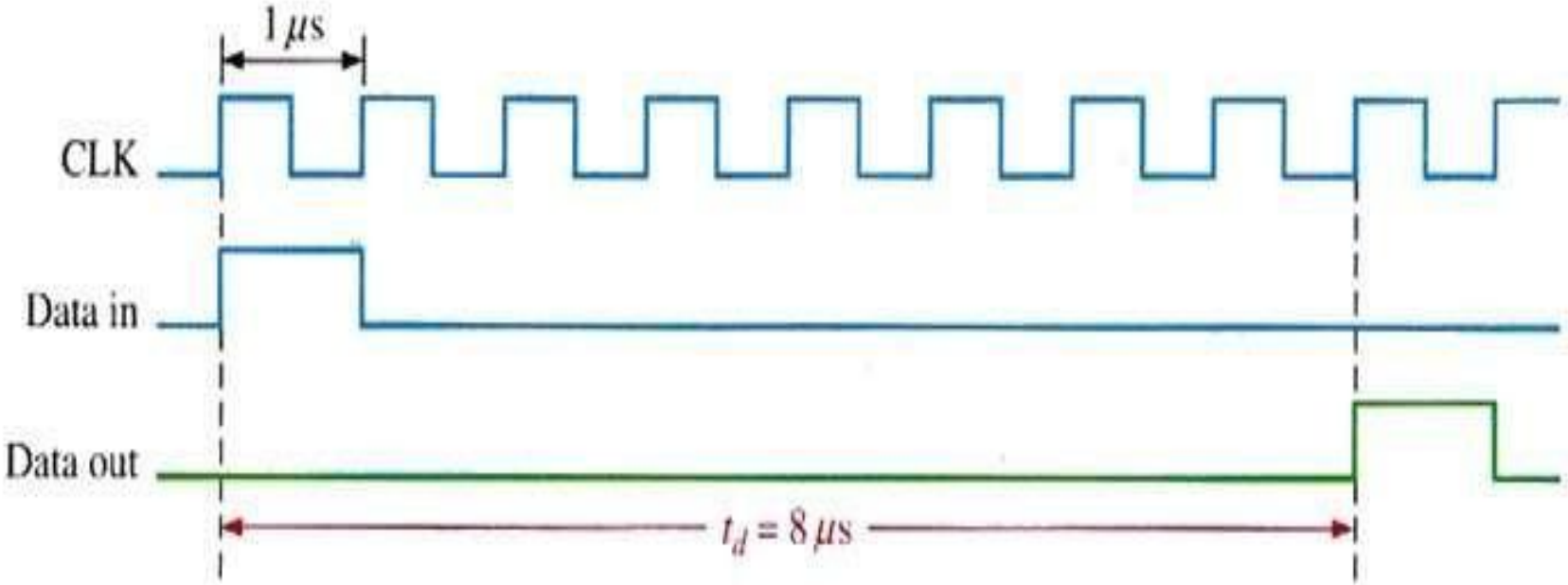
Time Delay

The serial in/serial out shift register can be used to provide a time delay from input to output that is a function of both the number of stages (n) in the register and the clock frequency. When a data pulse is applied to the serial input is shown in the following figure (A and B connected together), it enters the first stage on the triggering edge of the clock pulse. It is then shifted from stage to stage on each successive clock pulse until it appears on the serial output n clock periods later.

This time-delay operation in which an 8-bit serial in/serial out shift register is used with a clock frequency of 1MHz to achieve a time delay (td) of 8 μs (8 x 1 μs).

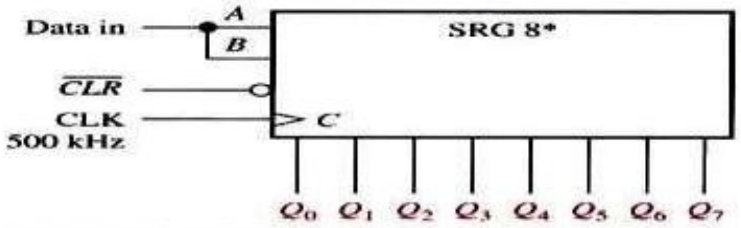
Example 1


Data in
A
B
SRG 8
Q_7
Data out
CLK
1 MHz
C
$\overline{Q}_7$


1 μs
CLK
Data in
Data out
$t_d = 8\,\mu s$

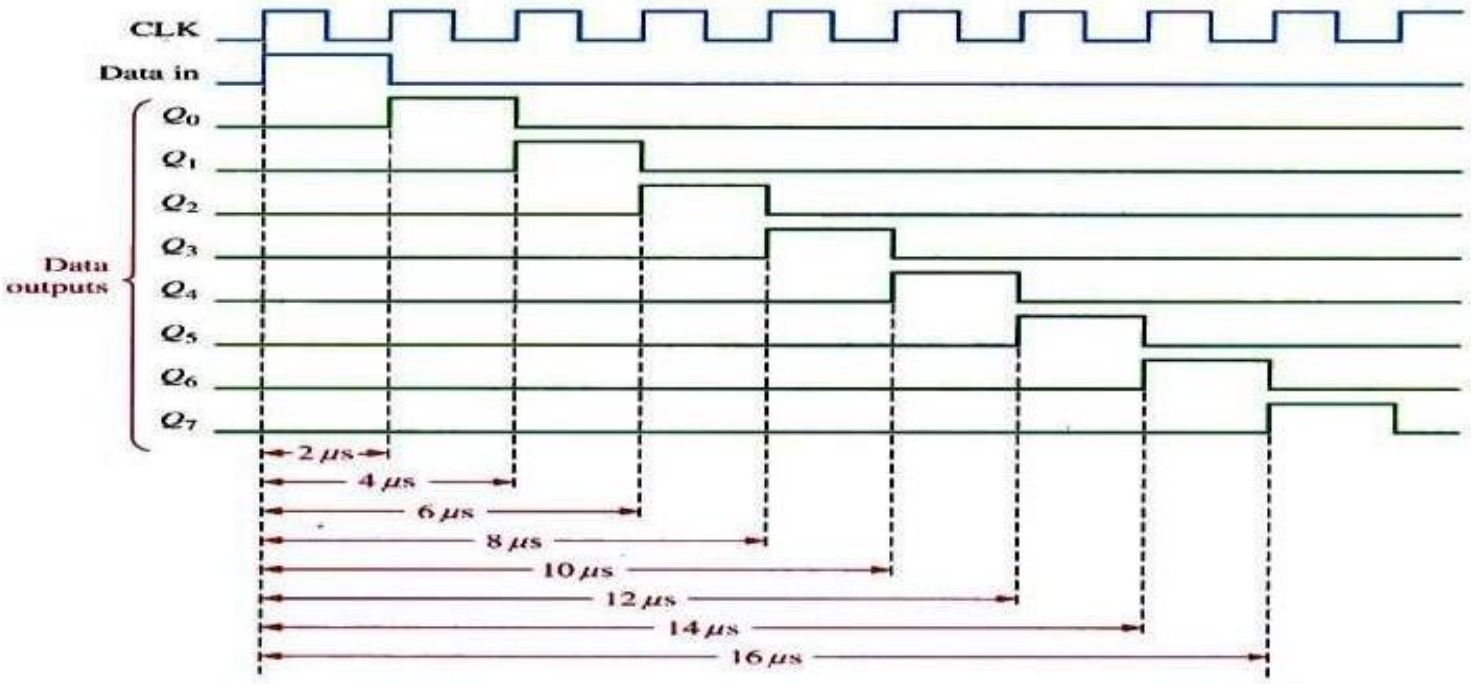
Example 2

Determine the amount of time delay between the serial input and each output



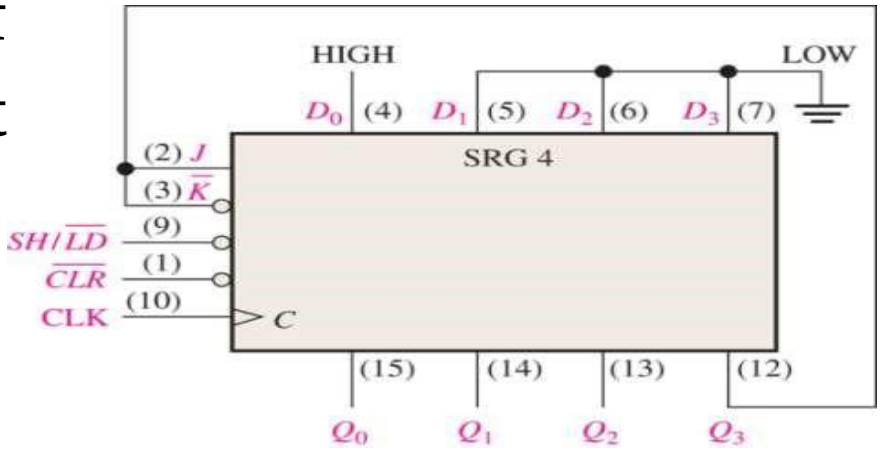
* Data shifts from Q_0 toward Q_7.

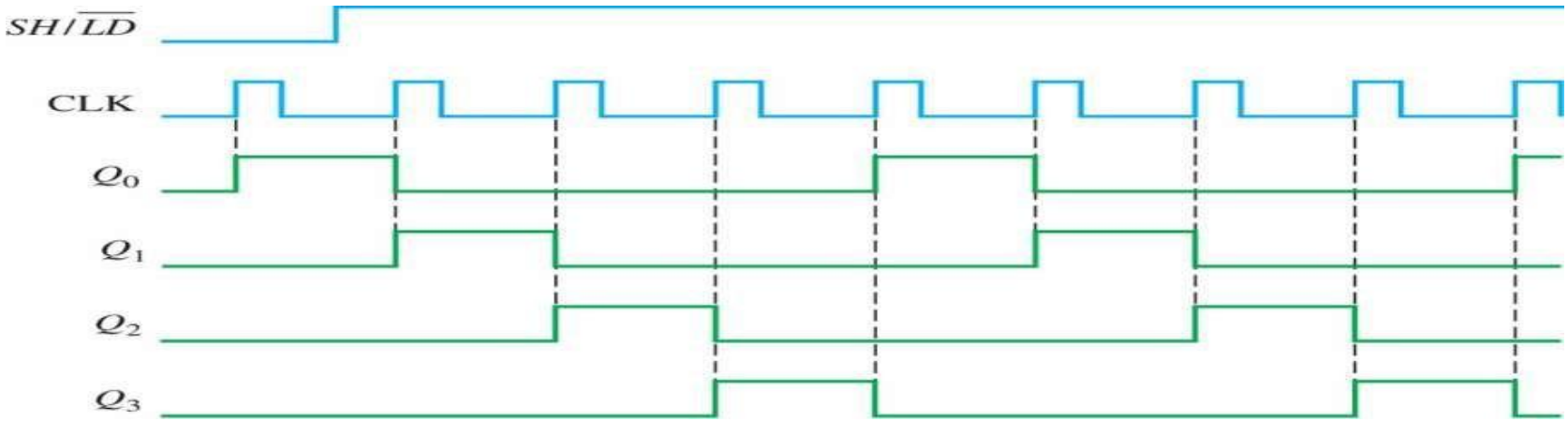
Solution The clock period is 2 μs. Thus, the time delay can be increased or decreased in 2 μs increments from a minimum of 2 μs to a maximum of 16 μs.



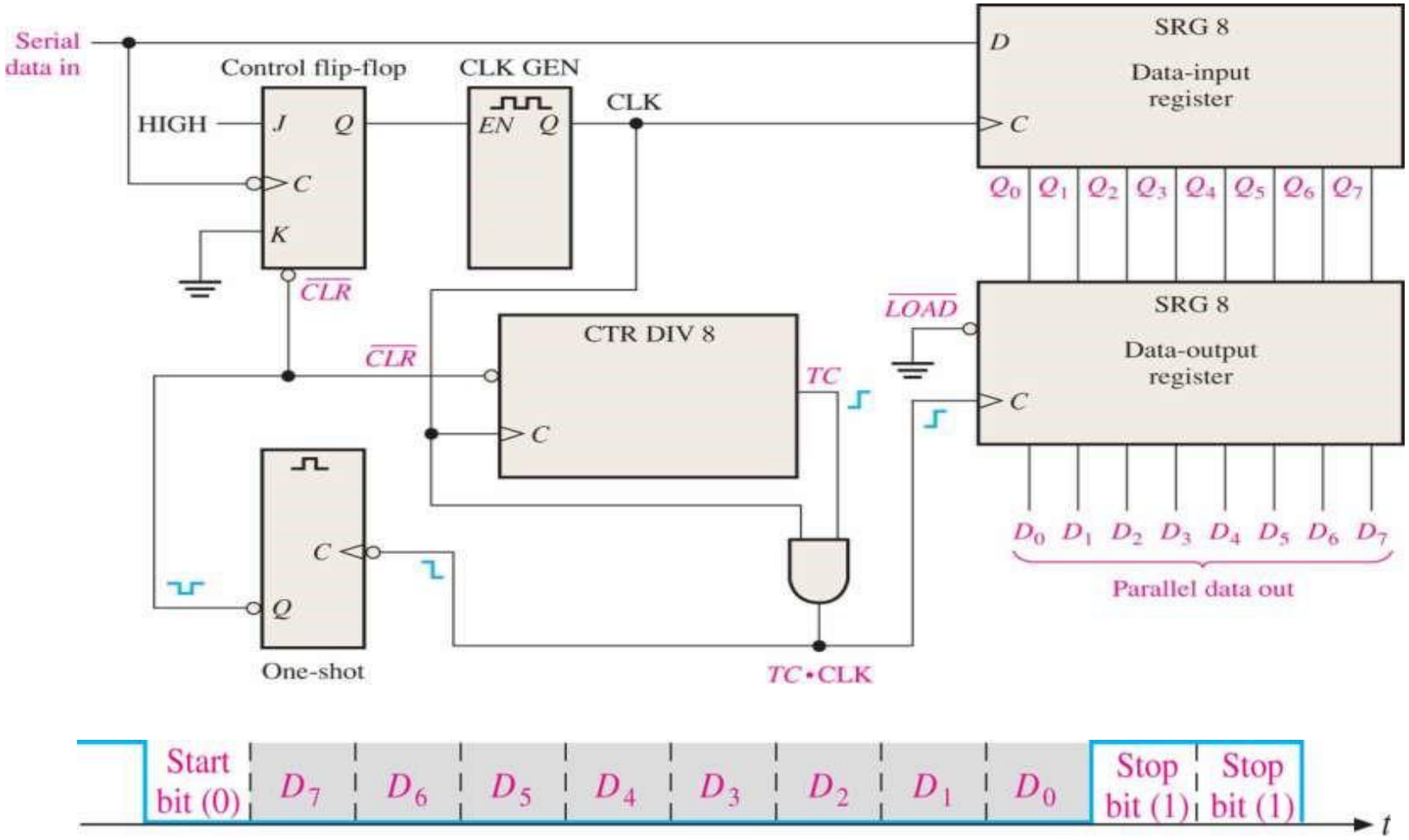
A ring counter using the 74HC195 shift register

Timing diagram showing two complete cycles of the ring counter when it is initially preset to 1000.

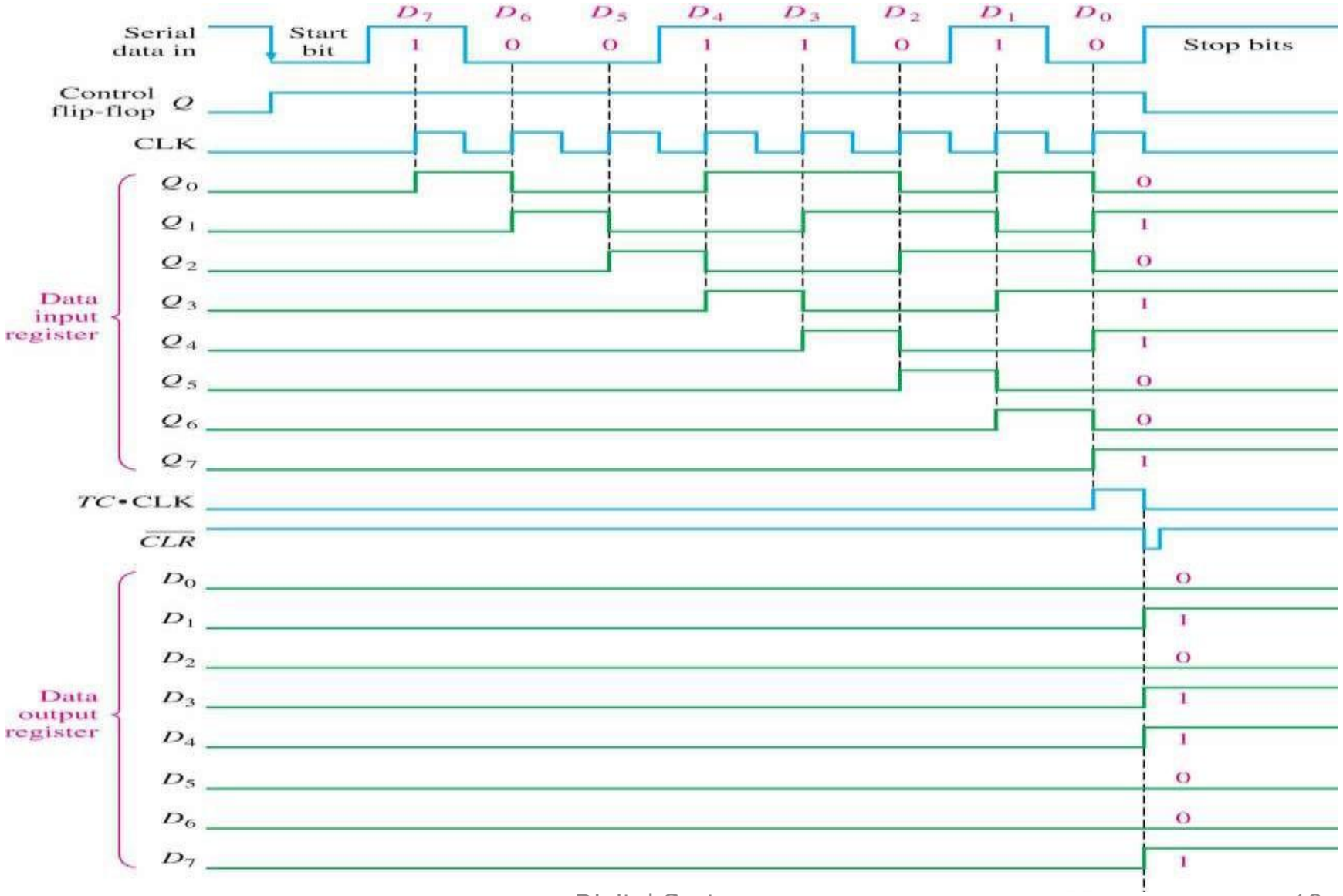




Serial to parallel Data Converter



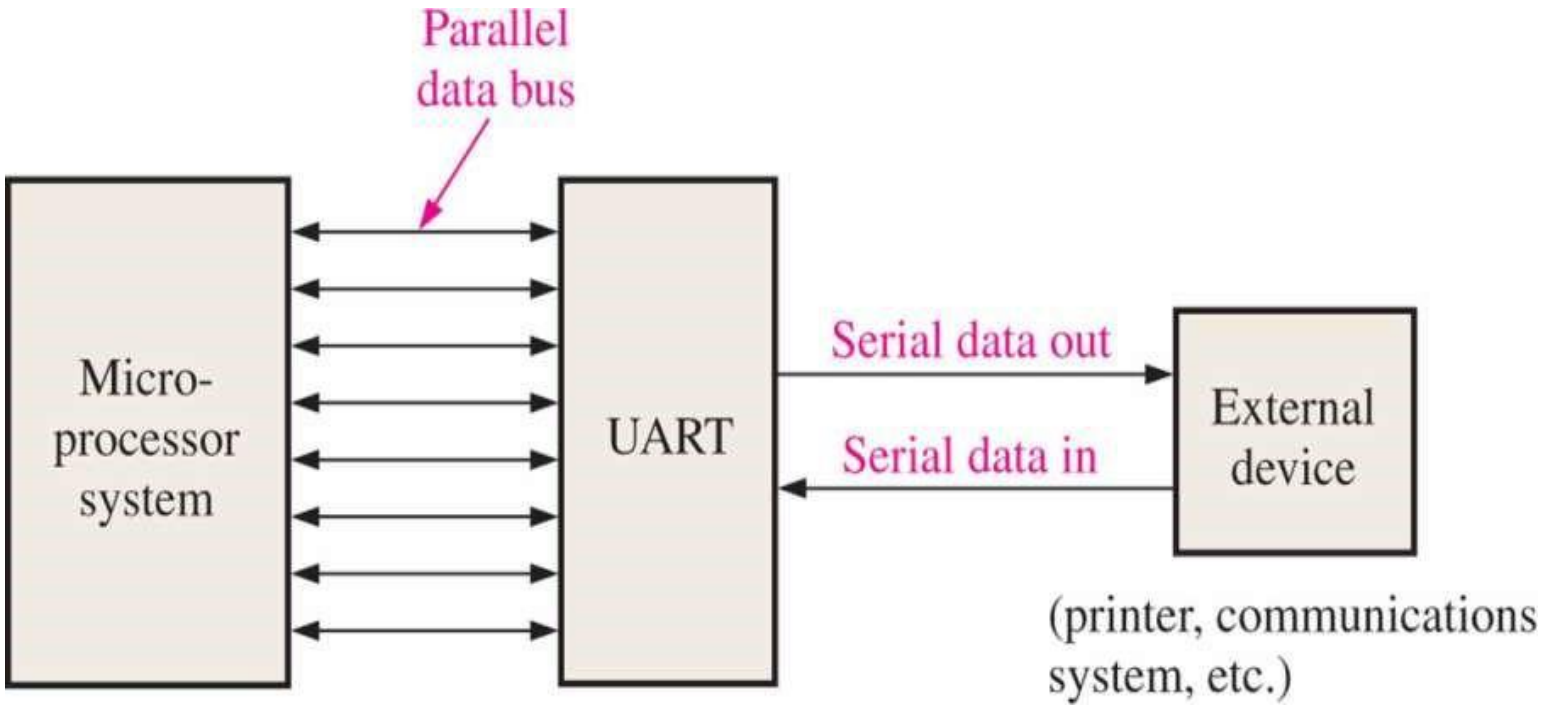
Data input and output: Timing



(UART)

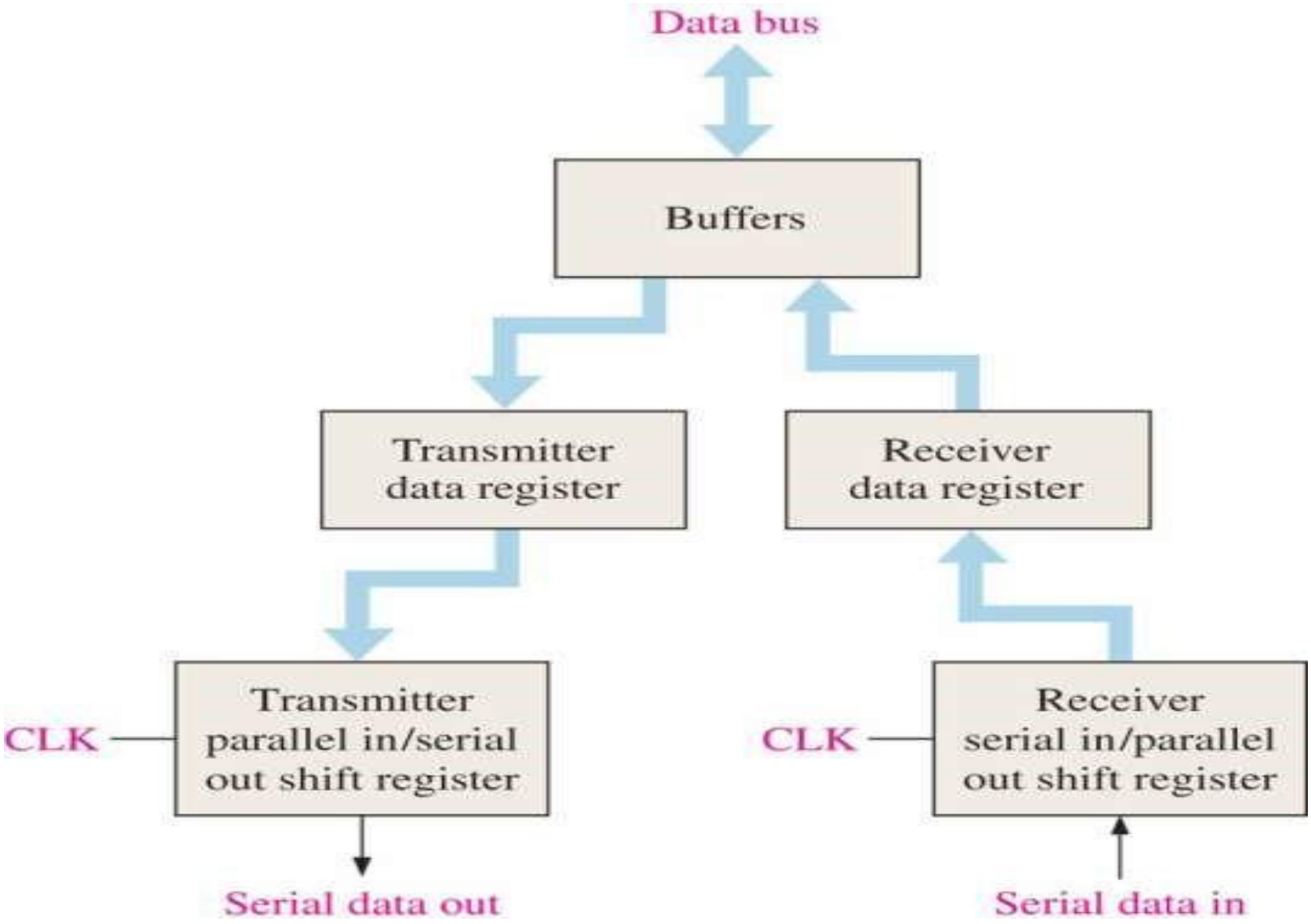
A UART (Universal Asynchronous Receiver Transmitter) is a serial-to parallel converter and a parallel to serial converter.

UARTs are commonly used in small systems where one device must communicate with another. Parallel data is converted to asynchronous serial form and transmitted. The serial data format is:



Basic UART block diagram.

Keyboard Encoding

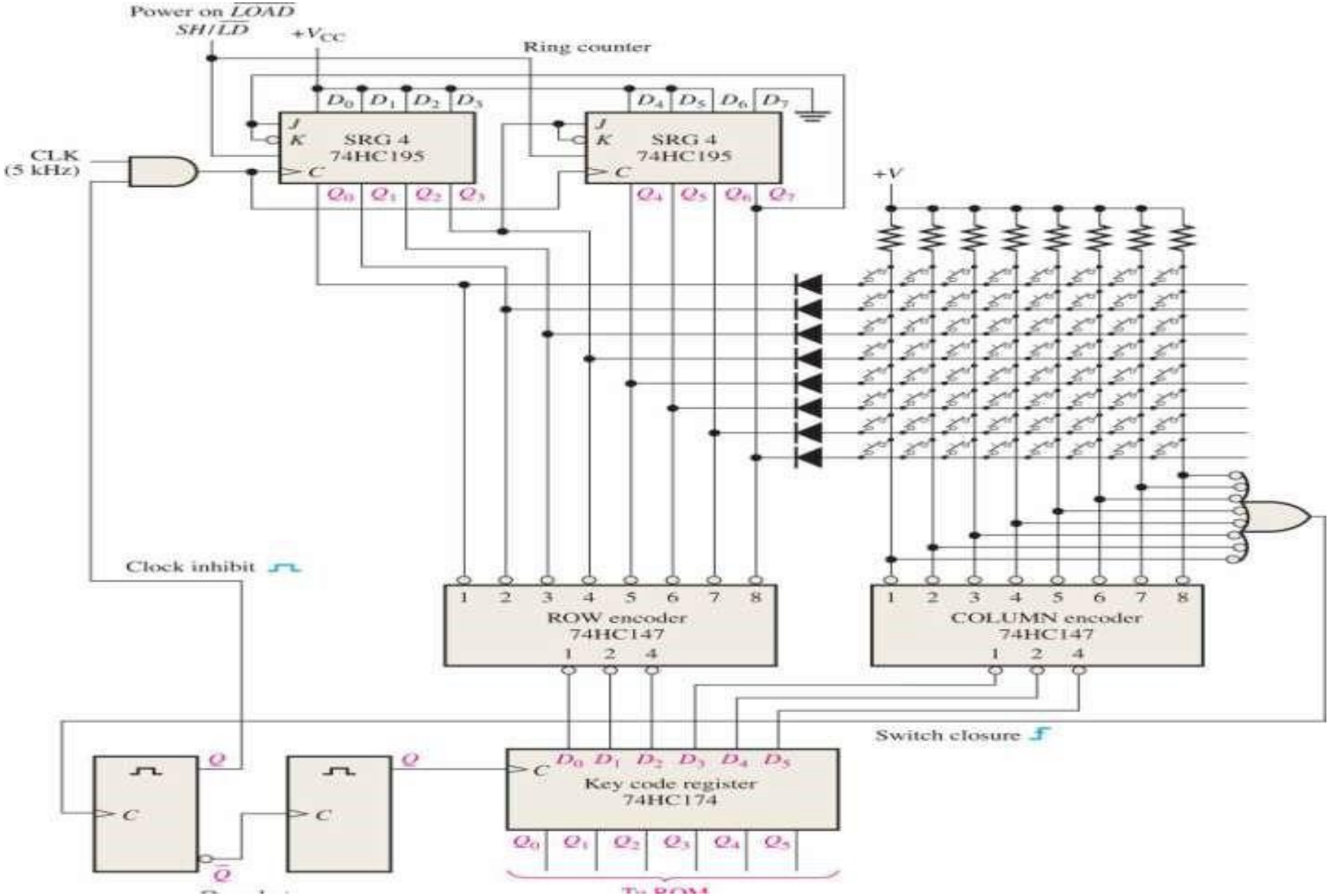


keyboard encoder

The keyboard encoder is an example of where a ring counter is used in a small system to encode a key press.

Two 74HC195 shift registers are connected as an 8-bit ring counter preloaded with a single 0. As the 0 circulate in the ring counter, it “scans” the keyboard looking for any row that has a key closure. When one is found, a corresponding column line is connected to that row line. The combination of the unique column and row lines identifies the key. The schematic is shown on the following slide…

Block diagram - keyboard encoder



(3 mins) Individual activity

https://docs.google.com/forms/d/e/1FAIpQLSf02f3_j_haRc7Wi1C4oxHAkf2nBKzHbAt-TRn01exlB75eDQ/viewform?usp=header

How does a bidirectional shift register differ from a unidirectional one?

Then Submit your answer using the QR code or the link above.

Summary Counter decoding

Shift Registers are sequential logic circuits used to store and shift data. They consist of flip-flops connected in series, where data is shifted in or out with each clock pulse.

1. Bidirectional Shift Register:

- Allows data to be shifted **left or right**.
- Has control input to determine shift direction.
- Useful in arithmetic operations and data movement.

2. Shift Register Counter:

- Also called a **ring counter** or **Johnson counter** depending on configuration.
- Uses shift register principles to create a counter sequence.
- Commonly used in timing circuits, sequencing, and control systems.

THANK YOU ☺

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END LESSON 10: SHIFT-REGISTERS (BIDIRECTIONAL , SHIFT REGISTER COUNTER)