جامعة المستقبل

نحو جامعة مستدامة

Al-Mustaqbal University - College of engineering
Department of computer engineering

Second stage

"Introduction of Digital Systems Module"

By DR. Mohammed Kadhim Rahma

2025

Welcome

Dr. Mohammed Rahma
A Lecturer at the College of Engineering (Al-Mustaqbal University)
Email: mohammed.Rahma@uomus.edu.iq
Please use module title in the email subject when contacting.

Academic journey:

Bachelor's degree Computer Engineering
MSc Computer systems and Networks,
Ph.D Computer Systems and components/Cyber security

Research: digital signature, Cyber security , cryptography, Encryption , project management, Networking.

Module Information

معلومات المادة الدراسية			
Module Title	**Digital Systems**		**Module Delivery**
Module Type	**Core**		• ✓ Theory • Lecture • ✓ Lab • Tutorial • Practical • Seminar
Module Code	**UOMU022021**		
ECTS Credits	**6**		
SWL (hr/sem)	**150**		
Module Level	**1**	**Semester of Delivery**	**2**
Administering Department	**Computer Engineering**	**College**	**EETC-College of Engineering and Technology**
Module Leader	**Dr. Mohammed Rahma**	**e-mail**	**mohammed.Rahma@uomus.edu.iq**
Module Leader's Acad. Title	**Lecturer**	**Module Leader's Qualification**	**PhD**
Scientific Committee Approval Date	**01/02/2025**	**Version Number**	**1.0**

Relation with other Modules

العلاقة مع المواد الدراسية الأخرى		
UOMU022011 Digital Fundamentals	**Semester**	**1**

Module Aims - أهداف المادة الدراسية

1. To understand the flip flop operation.
2. To understand the latches operation.
3. This course deals with the designing of logic systems.
4. To understand the principles of counter circuits.
5. To understand the shift registers.
6. To have a skill to design ADC and DAC.

Module Learning Outcomes

مخرجات التعلم للمادة الدراسية

1. Discuss the flip-flops.
2. Recognize the differences between flip-flops and latches.
3. List the applications of flip-flops.
4. Summarize what is meant by the logic systems.
5. Explain the counter circuits and discuss the difference between synchronous and asynchronous counter.
6. Discuss the types of asynchronous counter circuits.
7. Discuss the types of synchronous circuit.
8. Identify the shift registers.
9. Discuss the operations of each types of shift registers.
10. Discuss the shift register counter.
11. Explain the principles of ADC and DAC.
12. Explain the design for each type of ADC and DAC.

Learning and Teaching Strategies

استراتيجيات التعلم والتعليم

Type something like: The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students.

Module Evaluation

تقييم المادة الدراسية					
		Time / Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	1	10% (10)	4	LO #1-3
	Assignments	2	10% (10)	4, 10	LO #1 ,3- 8
	Projects / Lab.	10	10% (10)	Continuous	LO #1-14
	Report	10	10% (10)	Continuous	LO #1-14
Summative assessment	Midterm Exam	2 hr	10% (10)	9	LO #1-9
	Final Exam	4hr	50% (50)	15	All
Total assessment			100% (100 Marks)		

مصادر التعلم والتدريس
Learning and Teaching Resources

المتوفرة في مكتبة الجامعة / Available in the Library	
Required Text	Digital Fundamentals by Floyed
Recommended Text	Digital circuit analysis and design with Simulink modeling by Steven T. Karris

Grading Scheme

مخطط الدرجات			
Group	Grade	التقدير	Marks (%)
Success Group (50 - 100)	A-Excellent	امتياز	90-100
	B-Very Good	جيد جدا	80-89
	C-Good	جيد	70-79
	D-Satisfactory	متوسط	60-69
	E-Sufficient	مقبول	50-59
Fail Group (0 – 49)	FX–Fail	راسب (قيد المعالجة)	(45-49)
	F–Fail	راسب	(0-44)

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.

المنهاج
الاسبوعي النظري

Delivery Plan (Weekly Syllabus)

Week	Material Covered
Week 1	Flip-flops and laches (SR, JKD, D, T)
Week 2	Flip-Flops(edge triggered, master-slave)
Week 3	Flip-flops (conversion from one type to another, applications)
Week 4	Asynchronous counter
Week 5	Synchronous counter
Week 6	Decade, up-down counter
Week 7	Cascade counter, Counter decoding
Week 8	Shift-registers (SISO, SIPO,PISO,PIPO)
Week 9	Midterm exam
Week 10	Shift-registers (bidirectional , shift register counter)
Week 11	Multivibrators (definition , Classification , 555 timer)
Week 12	Digital-to-Analog Converter (DAC)
Week 13	Analog-to-Digital Converter (ADC)
Week 14	**Preparatory week before the final Exam**
Week 15	**final Exam**

Google Classroom

Please join the Google Classroom for Digital Systems Modules to access course materials, assignments, and updates.

https://classroom.google.com/c/NzgzNTI0MDM1OTMy?cjc=5t4nvf7h

Use the following class code to join:[ask your lecturer of module].

To join:

1. Go to classroom.google.com.
2. Then Click on the "+" sign and select **Join Class**.
3. Then Enter the class code provided above.
4. You can also join by scanning the QR code, which includes the classroom link