جامعة المستقبل

نحو جامعة مستدامة

Al-Mustaqbal University - College of engineering
Department of computer engineering

Second stage

Lecture Week 2

"Flip-Flops(edge triggered, master-slave)"

By DR. Mohammed Kadhim Rahma

2025

Objectives Overview

By the end of this lecture, students will be able to

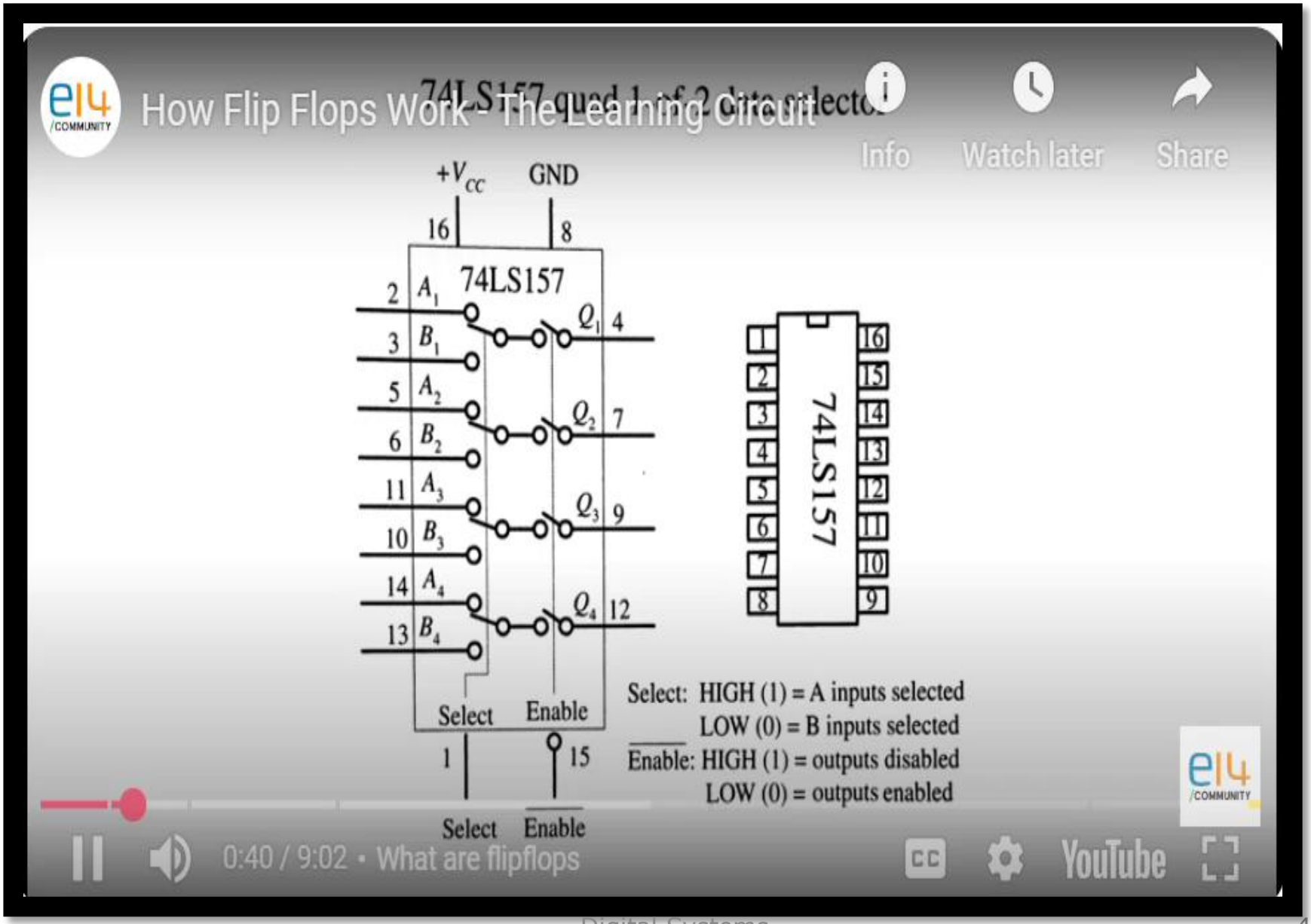
- Differentiate between edge-triggered and level-triggered flip-flops.
- Describe the operation of edge-triggered flip-flops (e.g., D, T, JK, and SR).
- Explain the master-slave configuration and its purpose in avoiding race conditions.

Objectives Overview

By the end of this lecture, students will be able to

- Analyze timing diagrams for both edge-triggered and master-slave flip-flops.
- Design and simulate basic circuits using edge-triggered and master-slave flip-flops.

break the ice كسر الجليد

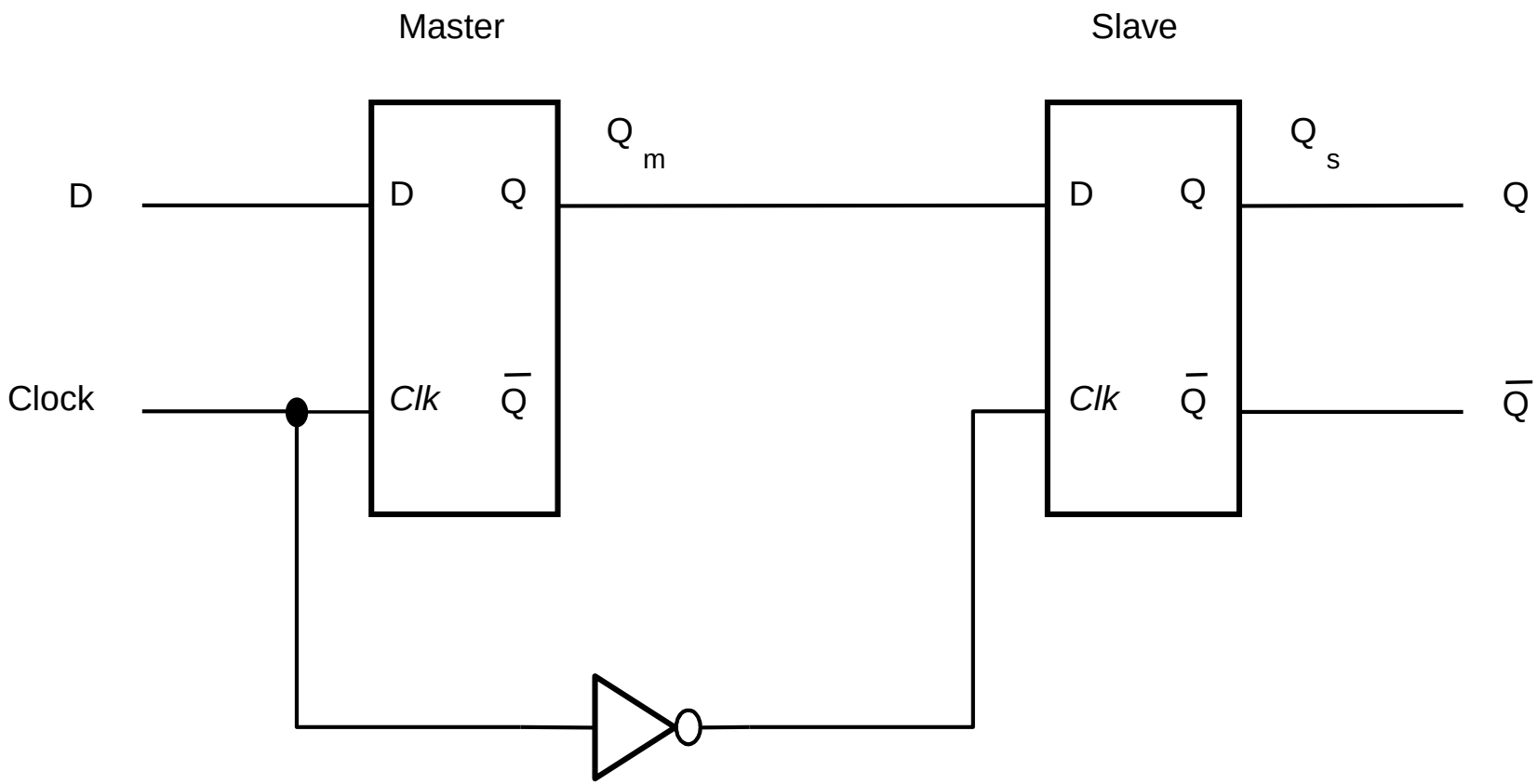


Edge-Triggered D Flip-Flops

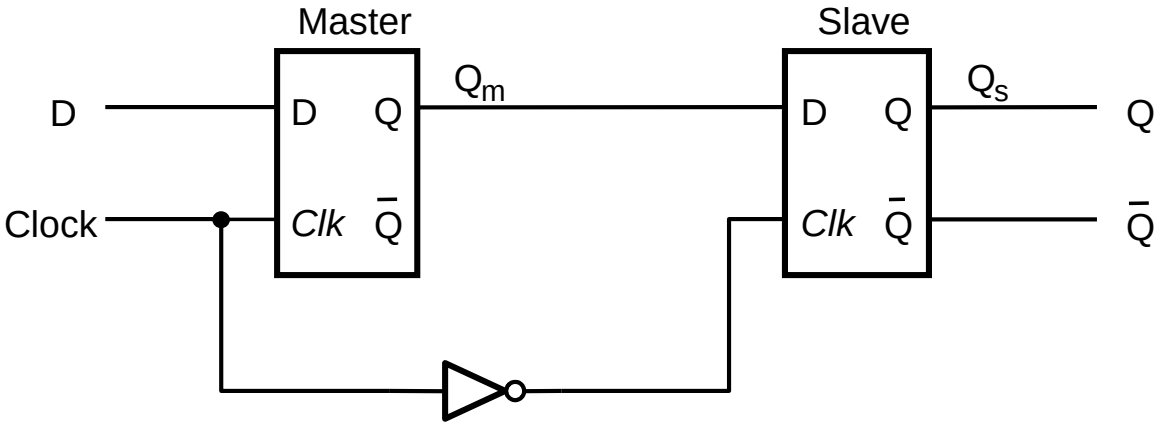
Motivation

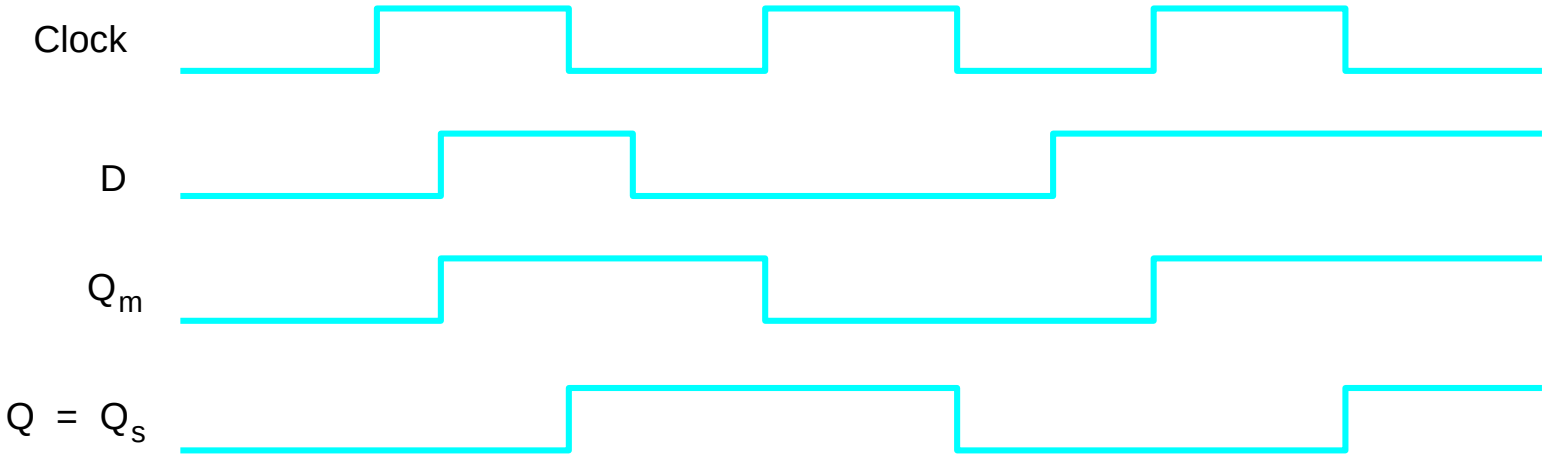
In some cases we need to use a memory storage device that can change its state no more than once during each clock cycle.

Master-Slave D Flip-Flop

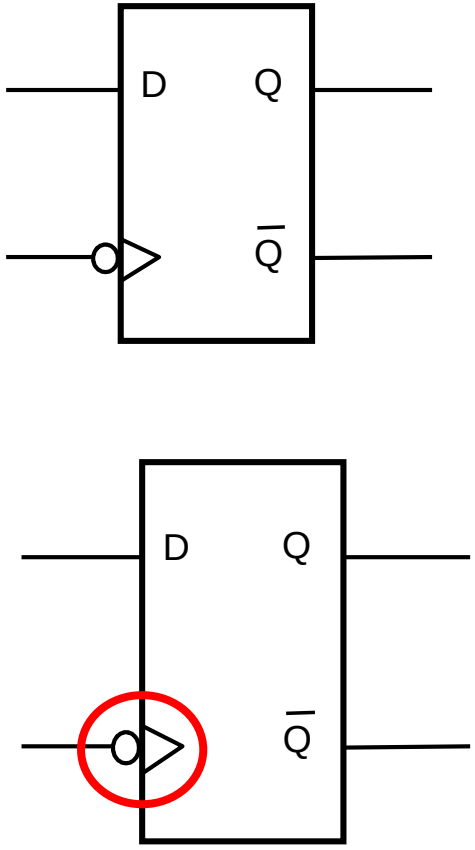


Timing Diagram for the Master-Slave D FF





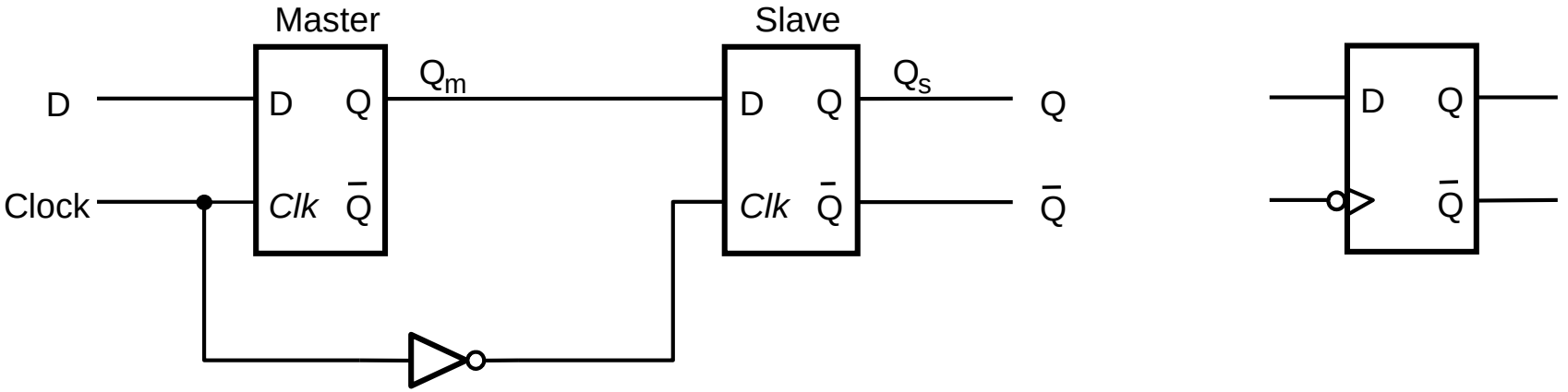
Graphical Symbol for the Master-Slave D Flip-Flop



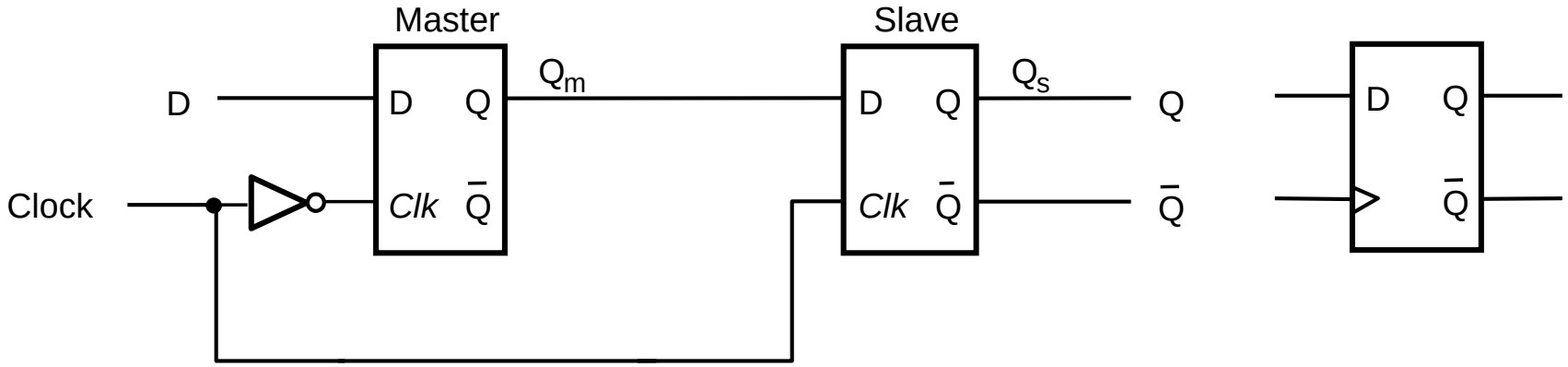
The > means that this is edge-triggered

The small circle means that is is the negative edge

Negative-Edge-Triggered Master-Slave D Flip-Flop

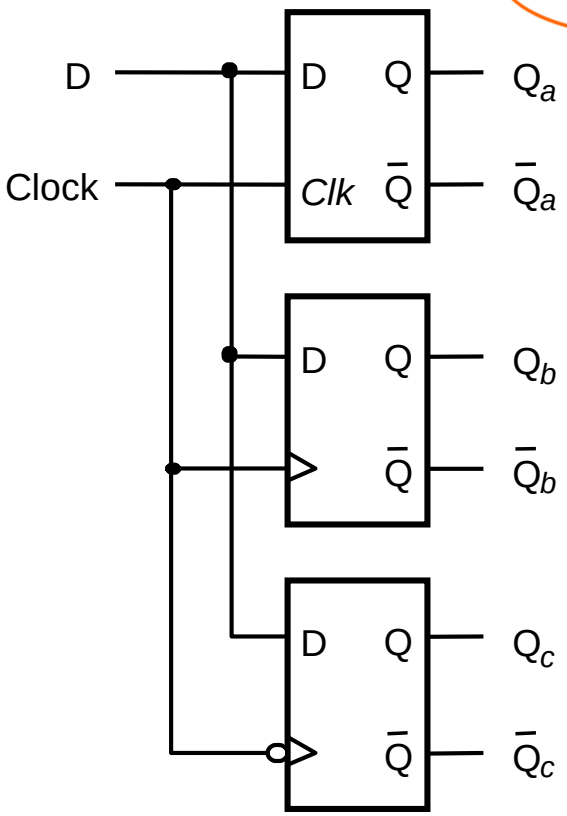


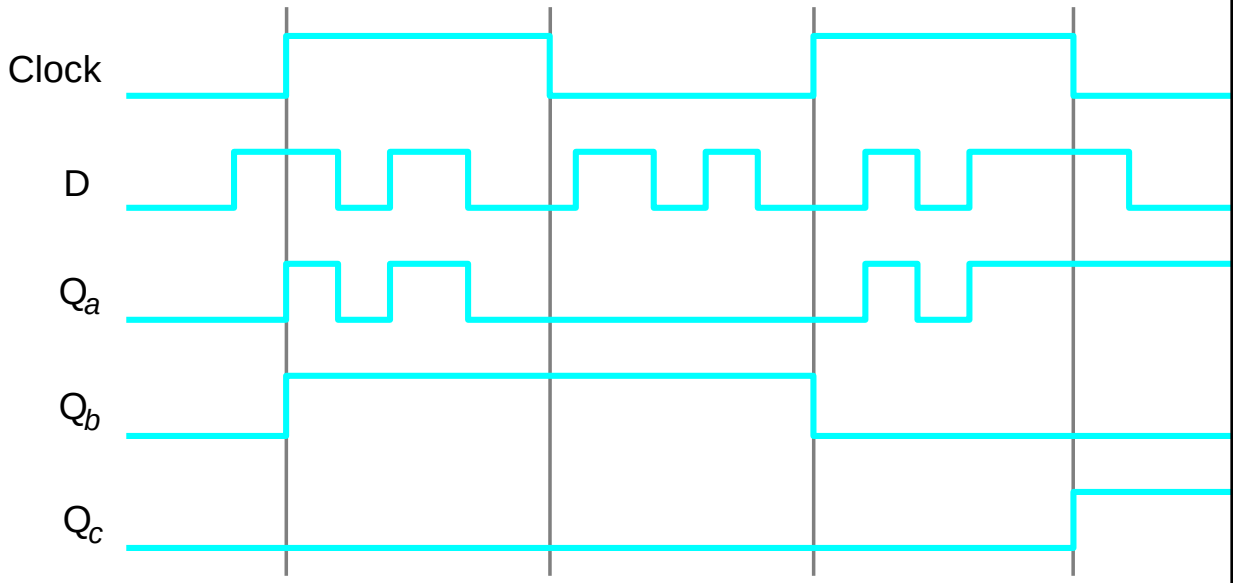
Positive-Edge-Triggered Master-Slave D Flip-Flop



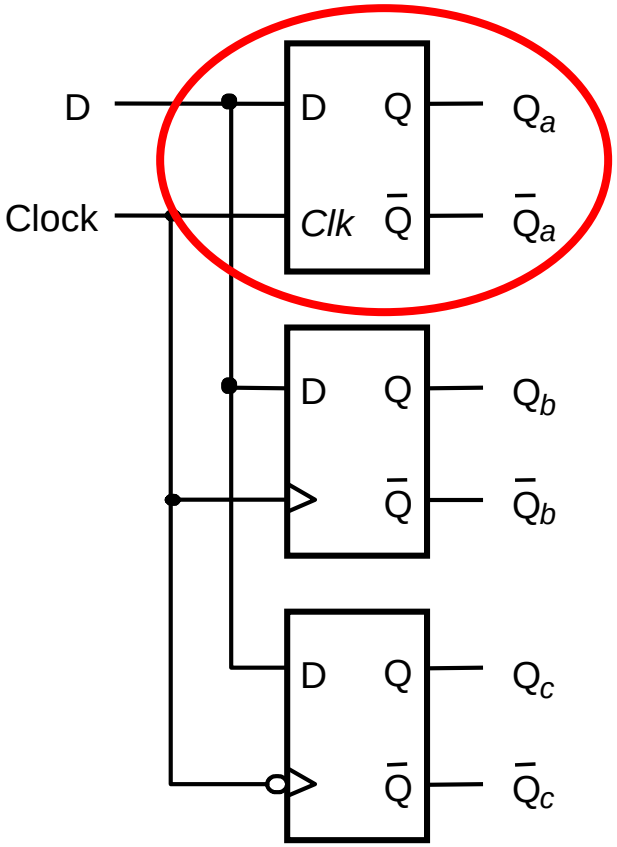
Other Types of Edge-Triggered D Flip-Flops

Comparison of level-sensitive and edge-triggered D storage elements

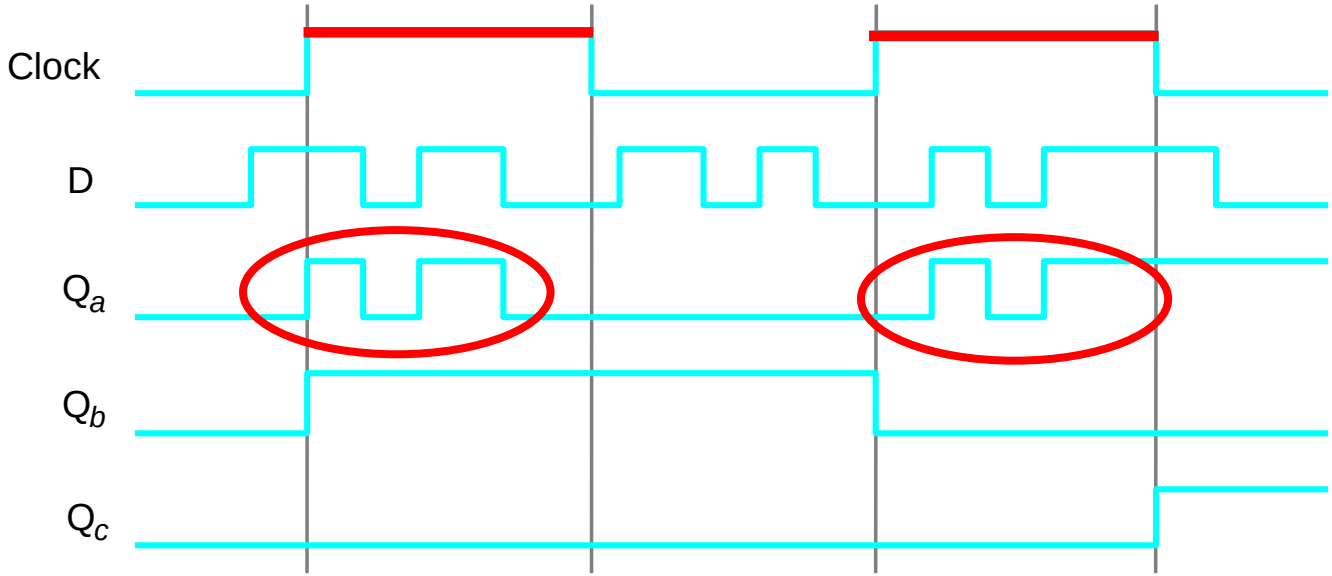




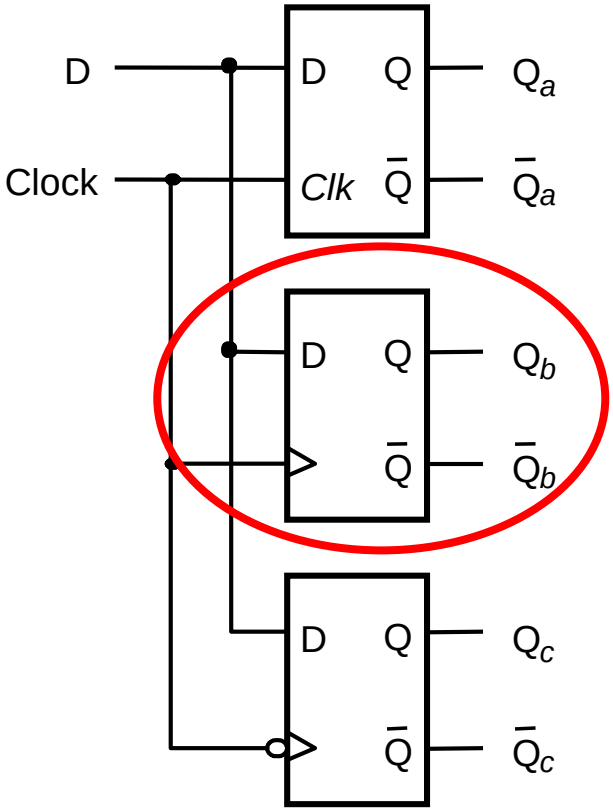
Comparison of level-sensitive and edge-triggered D storage elements



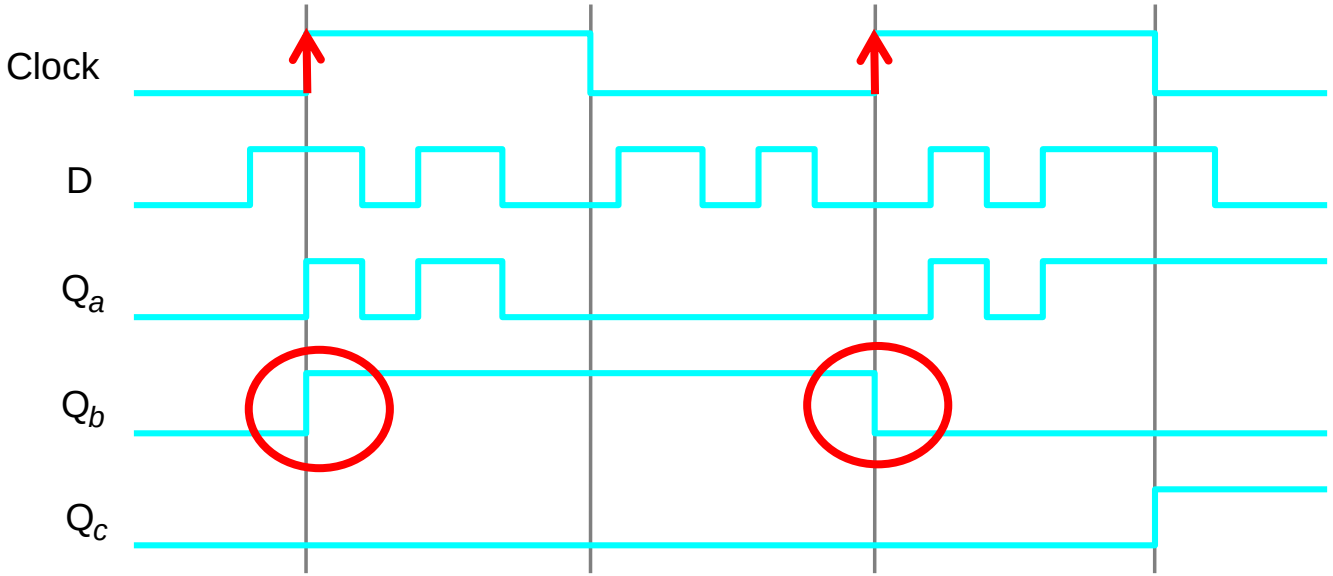
Level-sensitive
(the output mirrors the D input when Clk=1)



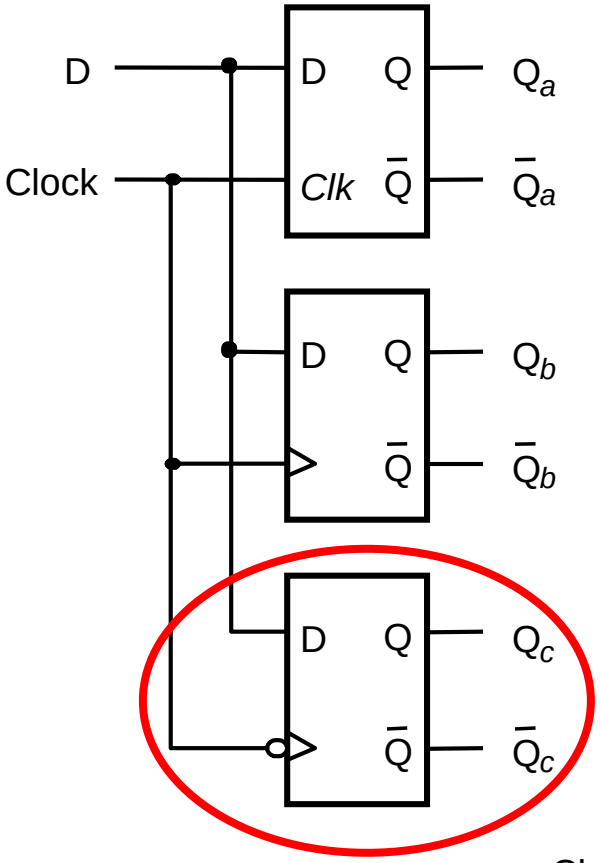
Comparison of level-sensitive and edge-triggered D storage elements



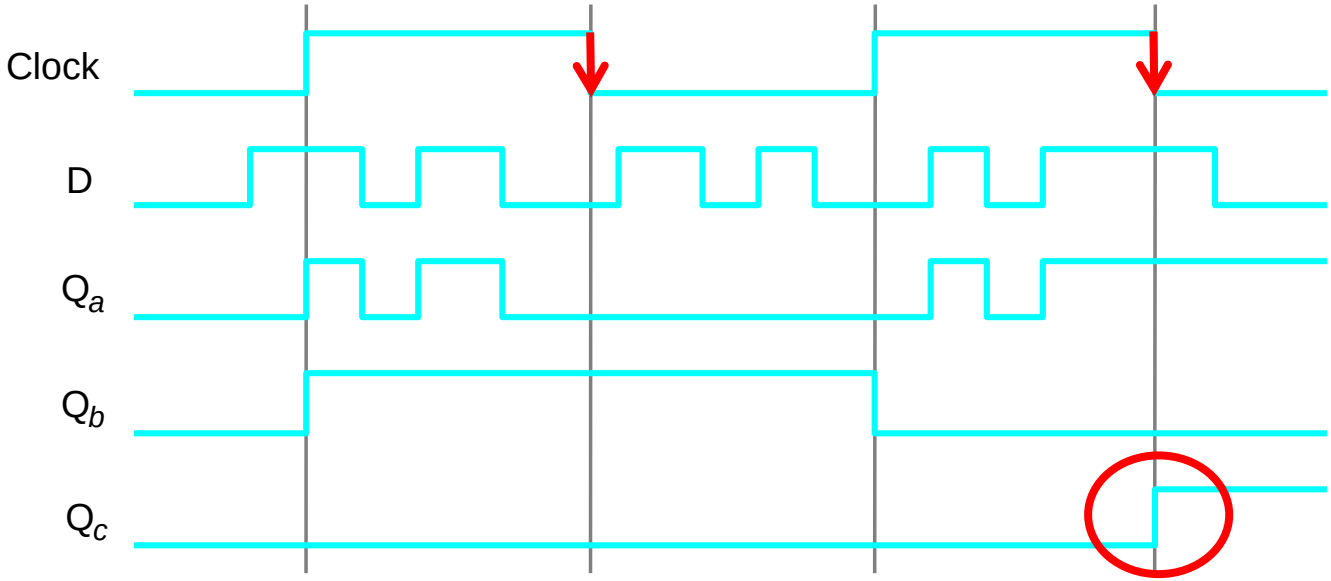
Positive-edge-triggered



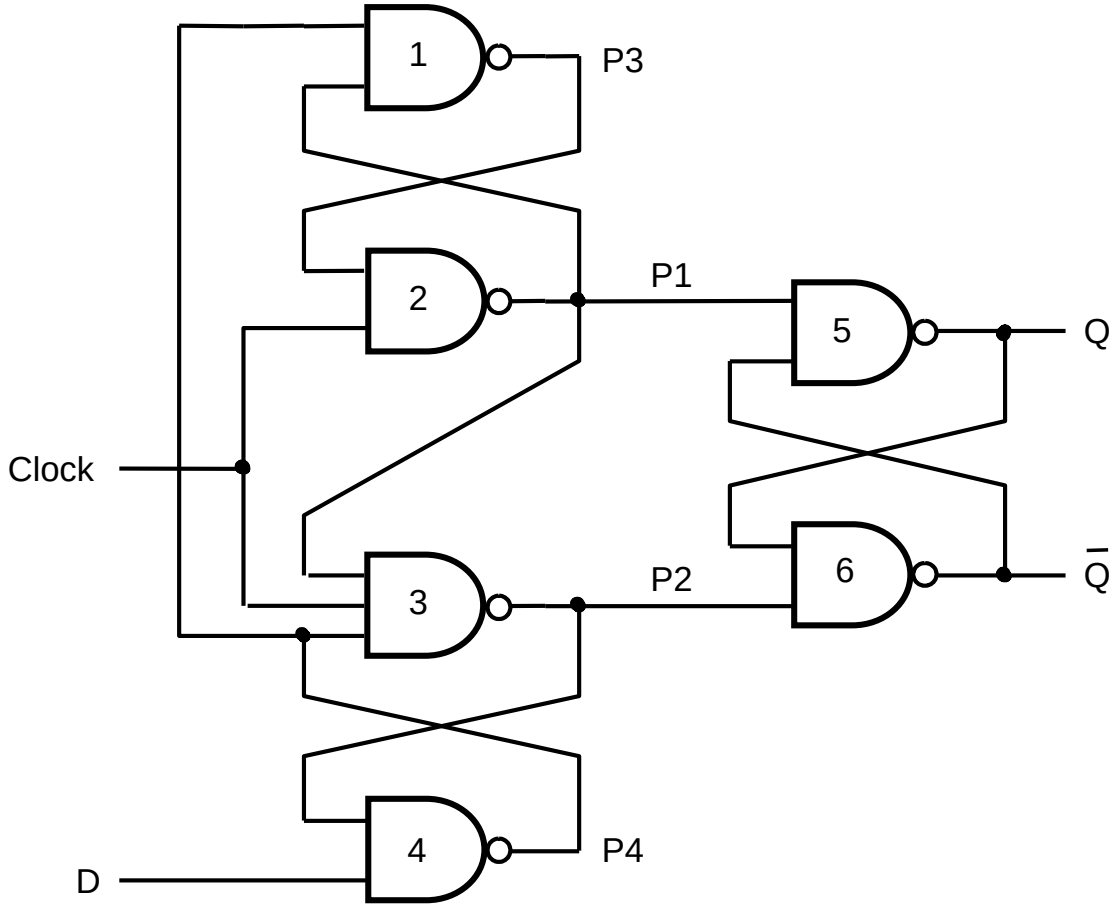
Comparison of level-sensitive and edge-triggered D storage elements



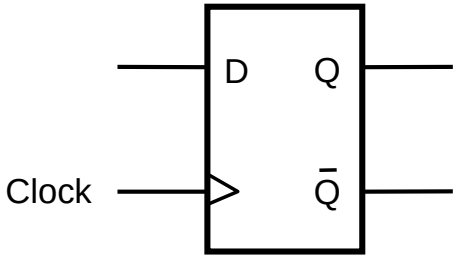
Negative-edge-triggered



A positive-edge-triggered D flip-flop



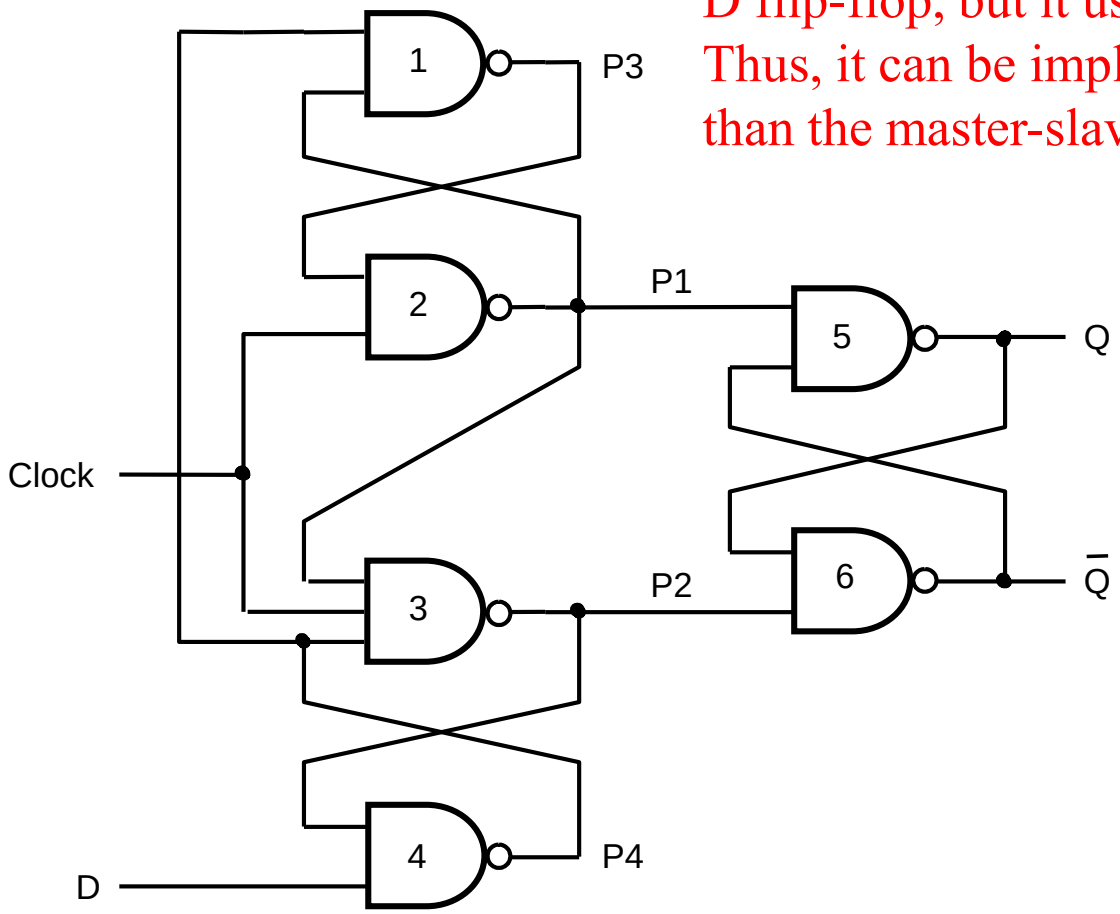
(a) Circuit



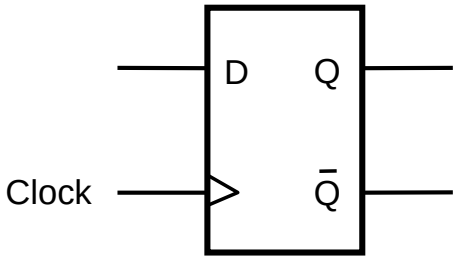
(b) Graphical symbol

A positive-edge-triggered D flip-flop

This circuit behaves like a positive-edge-triggered D flip-flop, but it uses only 6 NAND gates. Thus, it can be implemented with fewer transistors than the master-slave D flip-flop.

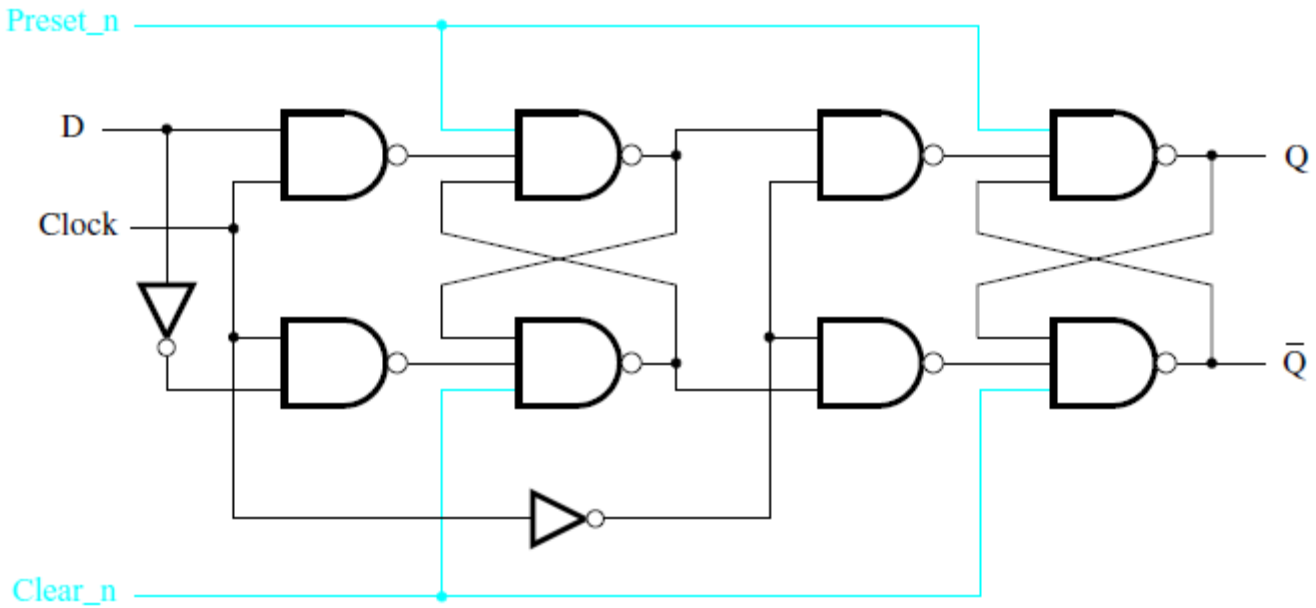


(a) Circuit

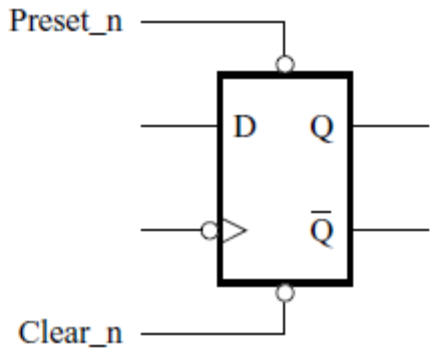


(b) Graphical symbol

Master-slave D flip-flop with Clear and Preset



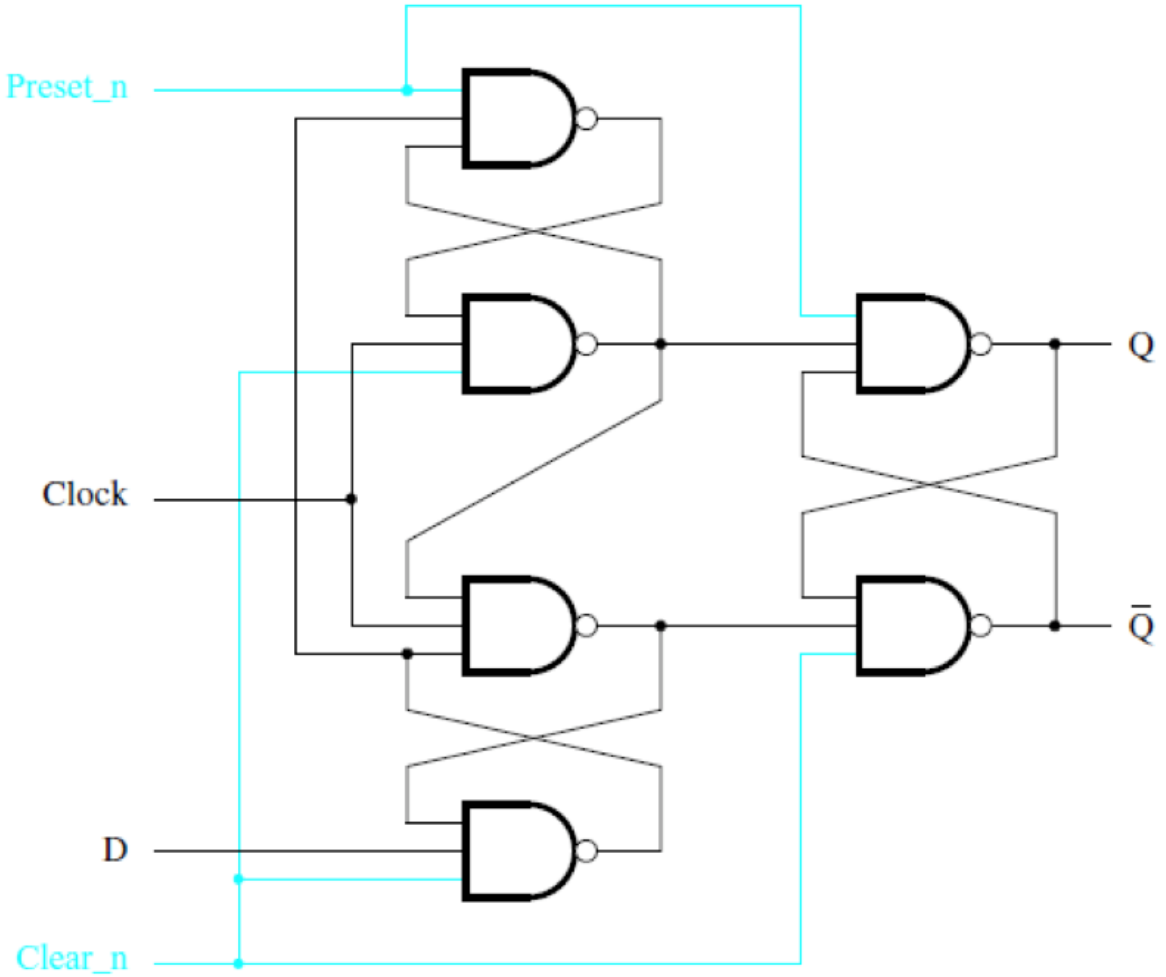
(a) Circuit



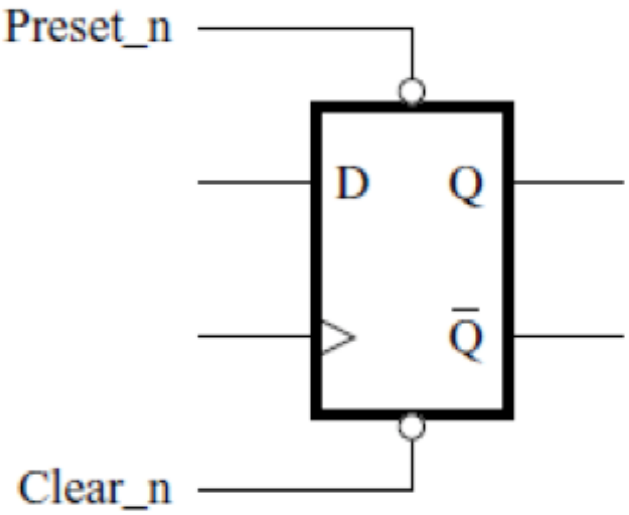
(b) Graphical symbol

Positive-edge-triggered D flip-flop with Clear and Preset

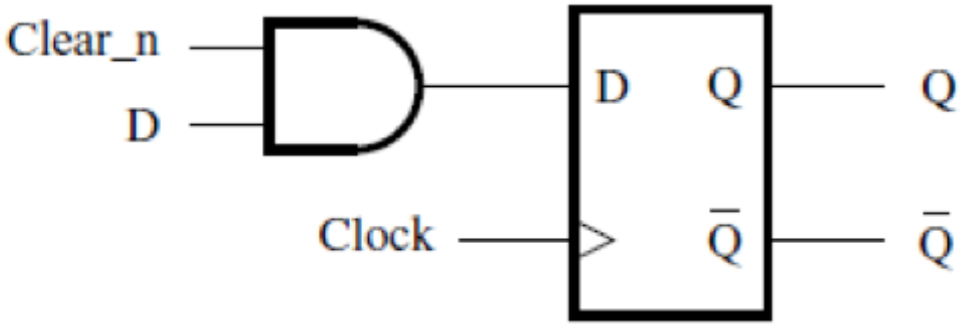
Positive-edge-triggered D flip-flop with Clear and Preset



Positive-edge-triggered D flip-flop with Clear and Preset

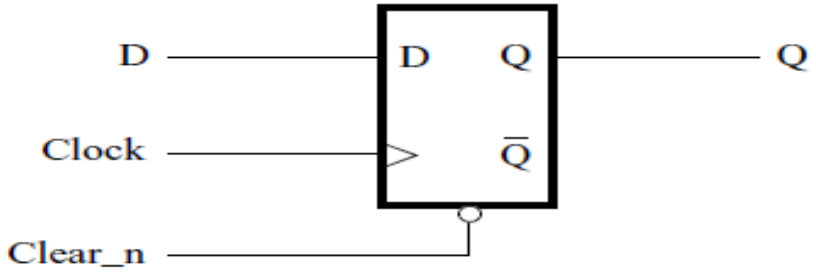


(b) Graphical symbol

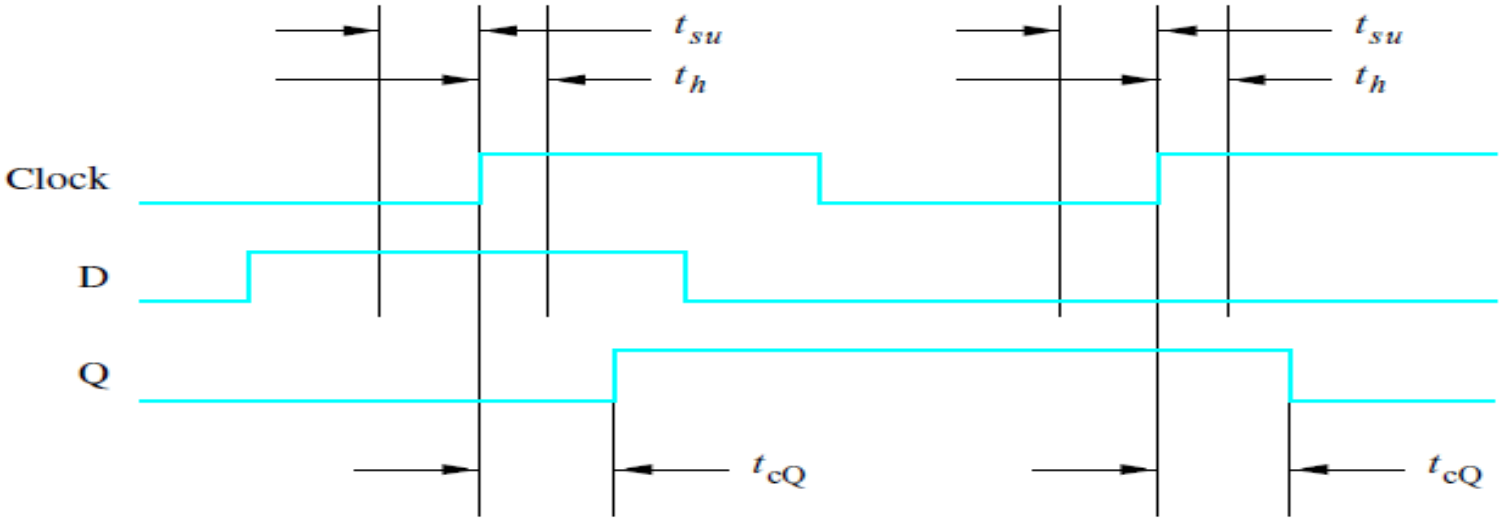


(c) Adding a synchronous clear

Flip-Flop Timing Parameters



(a) D flip-flop with asynchronous clear



(b) Timing diagram

(6 Minutes)

Group Activity

What is Positive-edge triggered and Negative-edge triggered **?**

Submit your answer using the QR code or the link below:

https://docs.google.com/forms/d/e/1FAIpQLScjbXOIiEl2M4GM_iLrYD-OZcvnenZ4MUqe3xLA2QNd_kMzpg/viewform?usp=header

Terminology

- **Basic Latch –** is a feedback connection of two NOR gates or two NAND gates, which can store one bit of information. It can be set using the S input and reset to 0 using the R input.
- **Gated Latch –** is a basic latch that includes input gating and a control input signal. The latch retains its existing state when the control input is equal to 0. Its state may be changed when the control signal is equal to 1.

Terminology

Two types of gated latches

(the control input is the clock):

- **Gated SR Latch –** uses the S and R inputs to set the latch to 1 or reset it to 0.
- **Gated D Latch –** uses the D input to force the latch into a state that has the same logic value as the D input.

Terminology

- **Positive-edge triggered –** if the state changes when the clock signal goes from 0 to 1.

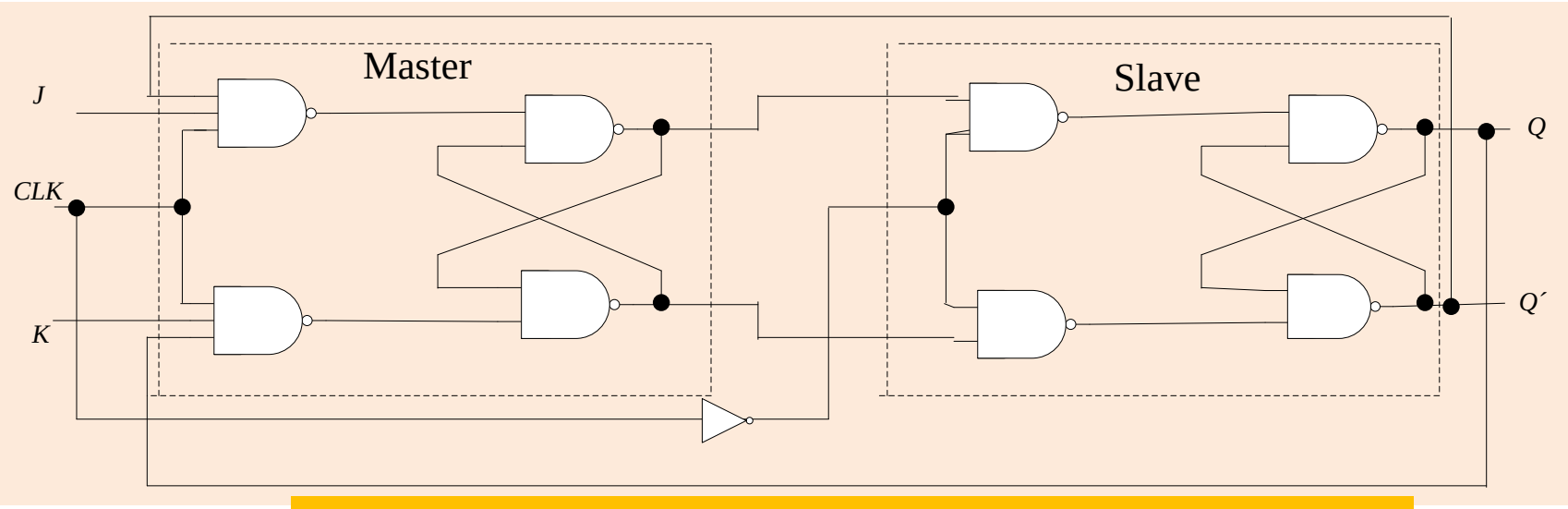
- **Negative-edge triggered –** if the state changes when the clock signal goes from 1 to 0.

Terminology

The word ***latch*** is mainly used for storage elements, while clocked devices are described as ***flip-flops***.

A **latch** is level-sensitive, whereas a **flip-flop** is edge-sensitive. That is, when a latch is enabled it becomes transparent, while a flip flop's output only changes on a single type (positive going or negative going) of clock edge.

Master / Slave JK Flip Flops



Clk { HIGH = Master enable; Slave isolate }
Clk { HIGH = Master isolate; Slave enable }

(Clk) High,	1.	$Q_S = 1,\ \overline{Q_S} = 0,$	J =1, K = 0	$Q_S, \overline{Q_S}$ output (no-change)
	2.	$Q_S = 0,\ \overline{Q_S} = 1,$	J =1, K = 0	$Q_{S\ output} = 1,\ \overline{Q_S}_{\ output} = 0$)
	3.	$Q_S = 1,\ \overline{Q_S} = 0,$	J =0, K = 1	$Q_{S\ output} = 0,\ \overline{Q_S}_{\ output} = 1$)
	4.	$Q_S = 0,\ \overline{Q_S} = 1,$	J =0, K = 1	$Q_S, \overline{Q_S}$ output (no-change)
	5.	$Q_S = X,\ \overline{Q_S} = X,$	J =0, K = 0	$Q_S, \overline{Q_S}$ output (no-change)
	6	$Q_S = 1,\ \overline{Q_S} = 0,$	J =1, K = 1	$Q_{S\ output} = 0,\ \overline{Q_S}_{\ output} = 1$)
	7.	$Q_S = 0,\ \overline{Q_S} = 1,$	J =1, K = 1	$Q_{S\ output} = 1,\ \overline{Q_S}_{\ output} = 0$)

Summary

- Edge-Triggered Flip-Flops change their state only at the rising or falling edge of the clock signal, ensuring more precise timing and control.
- Master-Slave Flip-Flops are made up of two flip-flops connected in series:
  - The Master is active on one clock edge (e.g., rising).
  - The Slave is active on the opposite edge (e.g., falling).
  - This structure avoids race conditions and ensures reliable data storage.

Summary

Types of Edge-Triggered Flip-Flops:

- D Flip-Flop: Data is transferred to the output on the clock edge.
- T Flip-Flop: Toggles the output on each clock edge if input T is high.
- JK Flip-Flop: More versatile; avoids invalid states of SR Flip-Flop.
- Applications:Used in counters, registers, shift registers, and memory units.

شكراً لحسن

إصغائكم

THANK YOU ☺

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Department of Computer Engineering

END LESSON 2: FLIP-FLOPS(EDGE TRIGGERED, MASTER-SLAVE)