جامعة المستقبل

نحو جامعة مستدامة

Al-Mustaqbal University - College of engineering
Department of computer engineering

Second stage

Lecture Week 5
"Synchronous Counter"

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2025

Objectives

By the end of this lecture, students will be able to

- Understand the Operation, Explain how synchronous counters work, including clock signal synchronization across all flip-flops.
- Design and Implementation synchronous counters using flip-flops and logic gates for various counting sequences (up, down, mod-N).
- Analyze and Troubleshoot, Interpret timing diagrams, state transitions, and identify issues in synchronous counter circuits.

Synchronous Counters

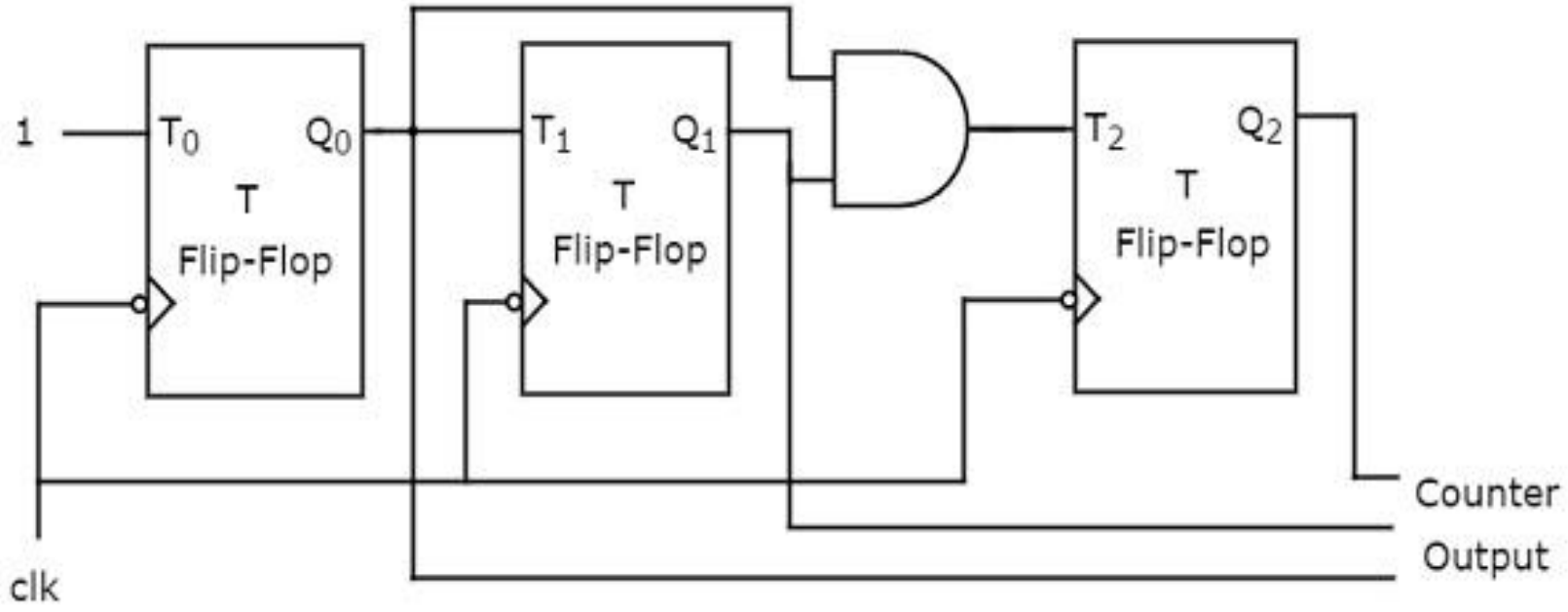
If all the flip-flops receive the same clock signal, then that counter is called as Synchronous counter. Hence, the outputs of all flip-flops change $affect$ at the same time.

Now, let us discuss the following two counters one by one.

1. **Synchronous Binary up counter**
2. **Synchronous Binary down counter**

Synchronous Binary Up Counter

- An ‘N’ bit Synchronous binary up counter consists of ‘N’ T flip-flops. It counts from 0 to $2^N - 1$.
- The block diagram of 3-bit Synchronous binary up counter is shown in the following figure.



Synchronous Binary Up Counter

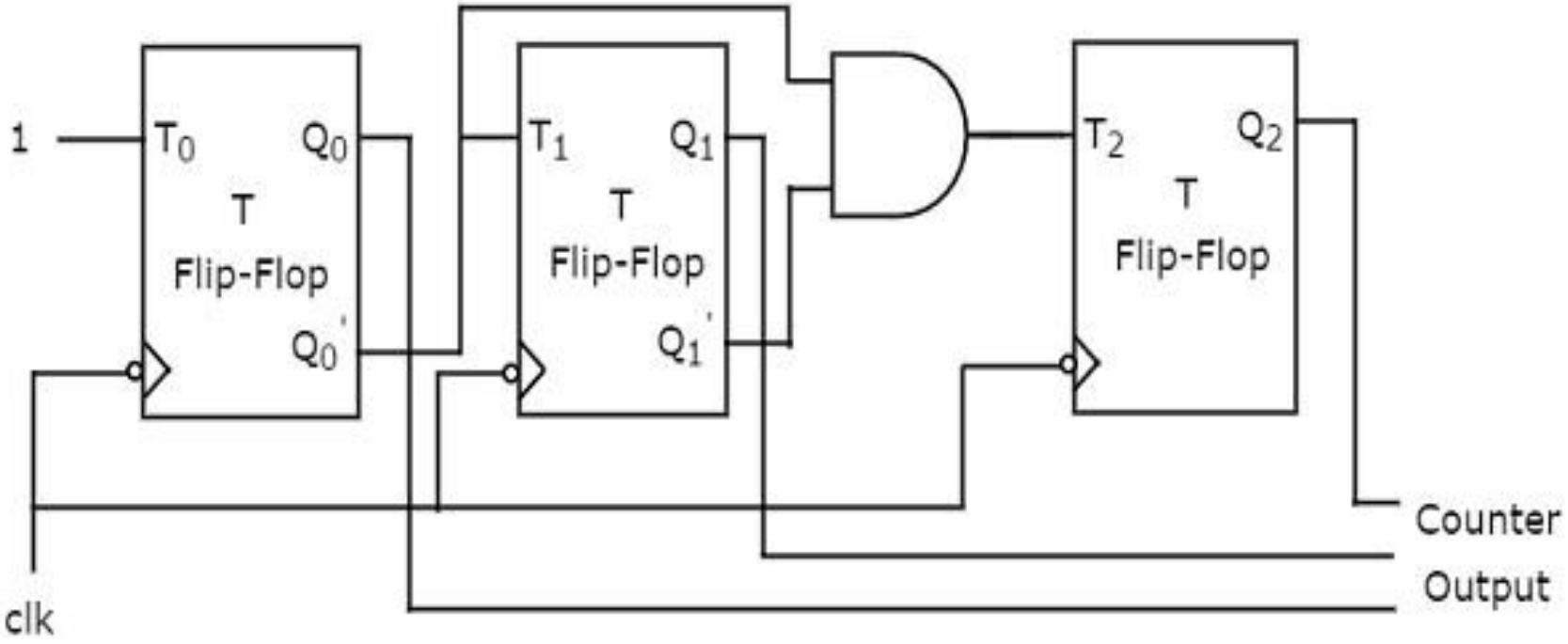
- The 3-bit Synchronous binary up counter contains three T flip-flops & one 2-input AND gate.
- All these flip-flops are negative edge triggered and the outputs of flip-flops change affect synchronously.
- The T inputs of first, second and third flip-flops are 1, Q0 & Q1Q0 respectively.

Synchronous Binary Up Counter

- The output of first T flip-flop toggles for every negative edge of clock signal.
- The output of second T flip-flop toggles for every negative edge of clock signal if Q0Q 0 is 1.
- The output of third T flip-flop toggles for every negative edge of clock signal if both Q0 & Q1 are 1.

Synchronous Binary Down Counter

An 'N' bit Synchronous binary down counter consists of 'N' T flip-flops. It counts from $2^N - 1$ to 0. The block diagram of 3-bit Synchronous binary down counter is shown in the following figure.



Synchronous Binary Down Counter

- The 3-bit Synchronous binary down counter contains three T flip-flops & one 2-input AND gate.
- All these flip-flops are negative edge triggered and the outputs of flip-flops change $affect$ synchronously.
- The T inputs of first, second and third flip-flops are 1, Q0′ &' Q1′ Q0′ respectively.

Synchronous Binary Down Counter

- The output of first T flip-flop **toggles** for every negative edge of clock signal.
- The output of second T flip-flop toggles for every negative edge of clock signal if Q0′ is 1.
- The output of third T flip-flop toggles for every negative edge of clock signal if both Q1′ & Q0′ are 1

(5 mins) Group Activity

https://docs.google.com/forms/d/e/1FAIpQLSeluP3bedMvvKkV0OnTKpzdTONSUZDEX88QUIpZ53KRGmjFZw/viewform?usp=header

Try thinking about what are the Applications of Synchronous Binary Counter!

Then Submit your answer using the QR code or the link above.

Applications of Synchronous Counters

- Digital Clocks and Timers
  Used to count seconds, minutes, and hours in timekeeping devices.
- Frequency Dividers
  Divide input clock frequency to lower frequencies in digital circuits.
- Control Systems and Sequencers
  Control the order of operations in automatic systems, such as vending machines and traffic lights.

Summary

- In synchronous counters, all flip-flops are triggered simultaneously by a common clock signal, ensuring synchronized state changes.
- They offer faster and more reliable operation compared to asynchronous counters due to reduced propagation delay.
- Synchronous counters are widely used in digital systems for counting, frequency division, and sequencing tasks.

THANK YOU ☺

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Department of Computer Engineering

END LESSON 5: SYNCHRONOUS COUNTER