جامعة المستقبل

نحو جامعة مستدامة

Al-Mustaqbal University - College of engineering
Department of computer engineering

Second stage

Lecture Week 1

"Flip-flops and laches"

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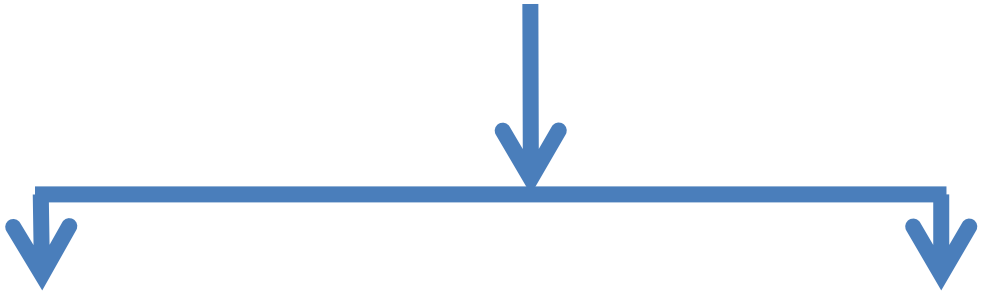
Objectives Overview

By the end of this lecture, students will be able to

- To define the concept of a Flip-Flop.
- To distinguish between different types of Flip-Flops: SR, D, JK, and T.
- To understand how each type of Flip-Flop operates using truth tables and timing diagrams.
- To draw logic circuits that include various types of Flip-Flops.
- To analyze the output of Flip-Flop-based circuits using timing diagrams.

سؤال سريع - a quick question

What are the types of digital circuits?



Sequential Circuits

1. **Synchronous**
2. **Asynchronous**

مقرر الكورس الثاني
الأنظمة الرقمية
Digital Systems
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Combinational Circuits

مقرر الكورس الأول
مباديء الرقمية
Digital Fundamentals
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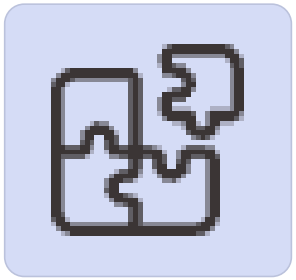
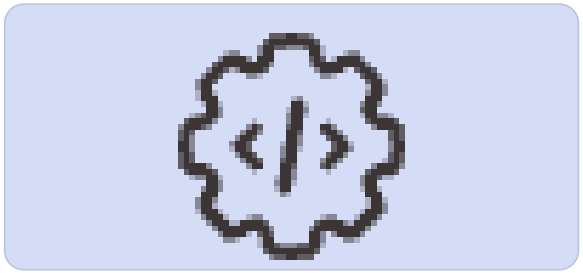
Sequential Logic

- The logic circuits discussed previously are known as *combinational*, in that the output depends only on the condition of the latest inputs
- However, we will now introduce a type of logic where the output depends not only on the latest inputs, but also on the condition of earlier inputs. These circuits are known as *sequential*, and implicitly they contain *memory* elements

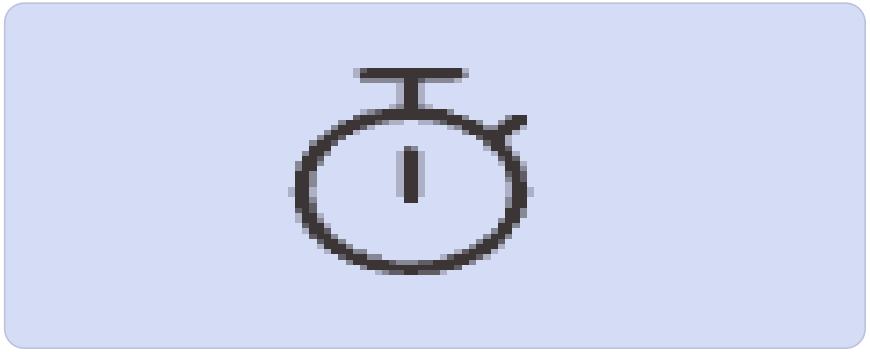
Key Difference : Design Complexity



Combinational: Simple Design
Uses only logic gates with straightforward implementation



Sequential: More Complex
Requires memory elements and clock synchronization



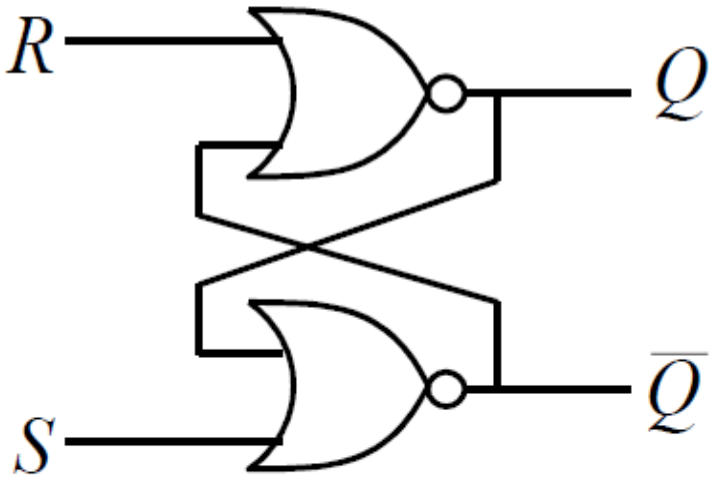
Sequential: Timing Critical
Demands careful timing considerations and signal management

Memory Elements

- A memory stores data – usually one bit per element
- A snapshot of the memory is called the *state*
- A one bit memory is often called a *bistable*, i.e., it has 2 stable internal states
- *Flip-flops* and *latches* are particular implementations of bistables

RS Latch

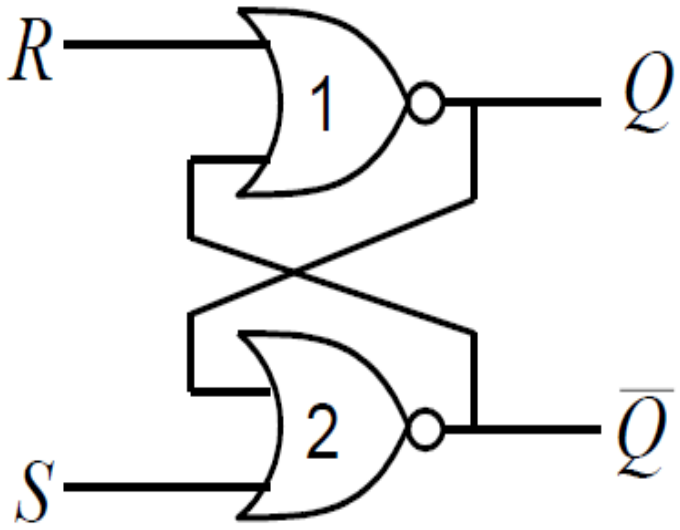
- An RS latch is a memory element with 2 inputs: Reset (R) and Set (S) and 2 outputs: Q and $\overline{Q}$.



S R	Q' $\overline{Q}'$	comment
0 0	Q $\overline{Q}$	hold
0 1	0 1	reset
1 0	1 0	set
1 1	0 0	illegal

Where Q' is the next state and Q is the current state

RS Latch - Operation

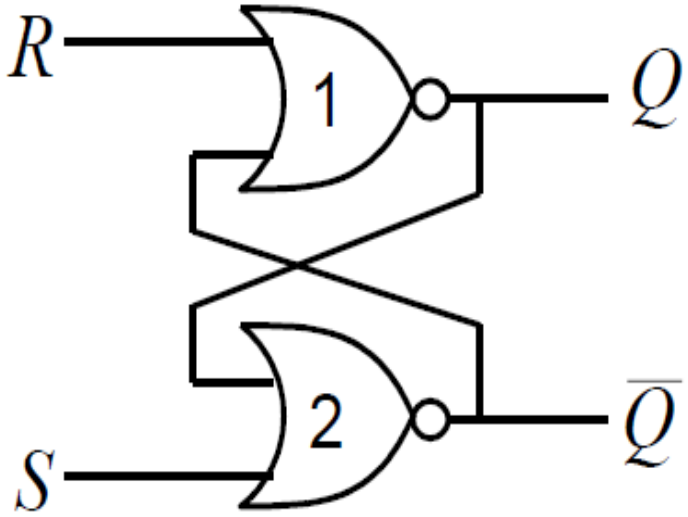


NOR truth table

a	b	y	
0	0	1	b complemented
0	1	0	
1	0	0	always 0
1	1	0	

- R = 1 and S = 0
  - Gate 1 output in 'always 0' condition, $Q = 0$
  - Gate 2 in 'complement' condition, so $\overline{Q} = 1$
- This is the (R)eset condition

RS Latch - Operation

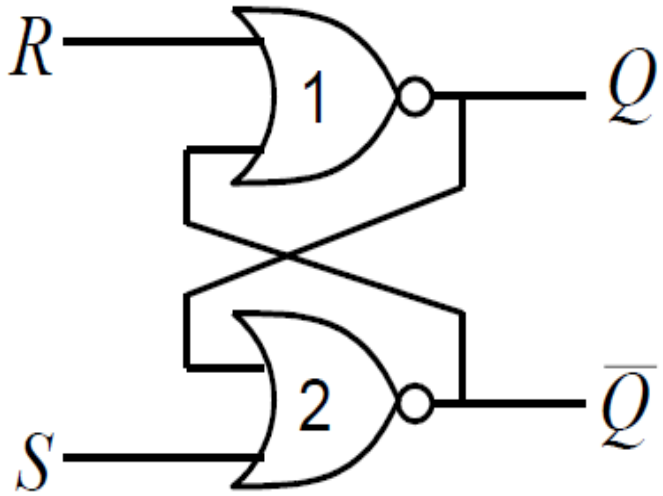


NOR truth table

a	b	y	
0	0	1	b complemented
0	1	0	
1	0	0	always 0
1	1	0	

- S = 0 and R to 0
  - Gate 2 remains in 'complement' condition, $\overline{Q} = 1$
  - Gate 1 into 'complement' condition, $Q = 0$
- This is the hold condition

RS Latch - Operation

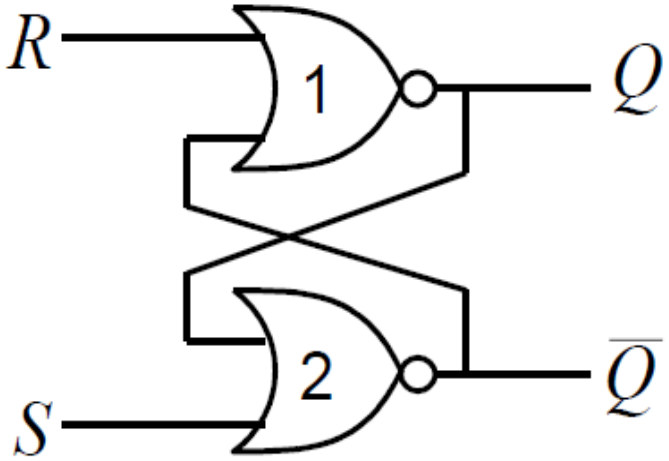


NOR truth table

a	b	y	
0	0	1	b complemented
0	1	0	
1	0	0	always 0
1	1	0	

- S = 1 and R = 0
  - Gate 1 into 'complement' condition, $Q = 1$
  - Gate 2 in 'always 0' condition, $\overline{Q} = 0$
- This is the (S)et condition

RS Latch - Operation



NOR truth table

a	b	y	
0	0	1	b complemented
0	1	0	
1	0	0	always 0
1	1	0	

- S = 1 and R = 1
  - Gate 1 in 'always 0' condition, $Q = 0$
  - Gate 2 in 'always 0' condition, $\overline{Q} = 0$
- This is the illegal condition

RS Latch – State Transition Table

- A *state transition table* is an alternative way of viewing its operation

Q	S	R	Q'	comment
0	0	0	0	hold
0	0	1	0	reset
0	1	0	1	set
0	1	1	0	illegal
1	0	0	1	hold
1	0	1	0	reset
1	1	0	1	set
1	1	1	0	illegal

- A state transition table can also be expressed in the form of a *state diagram*

What are Flip-Flops?

The flip-flops are basically the circuits that maintain a certain state unless and until directed by the input for changing that state. We can construct a basic flip-flop using four-NOR and four-NAND gates.

Types of Flip-Flops

The flip-flops are of the following types:

1. S-R Flip Flop

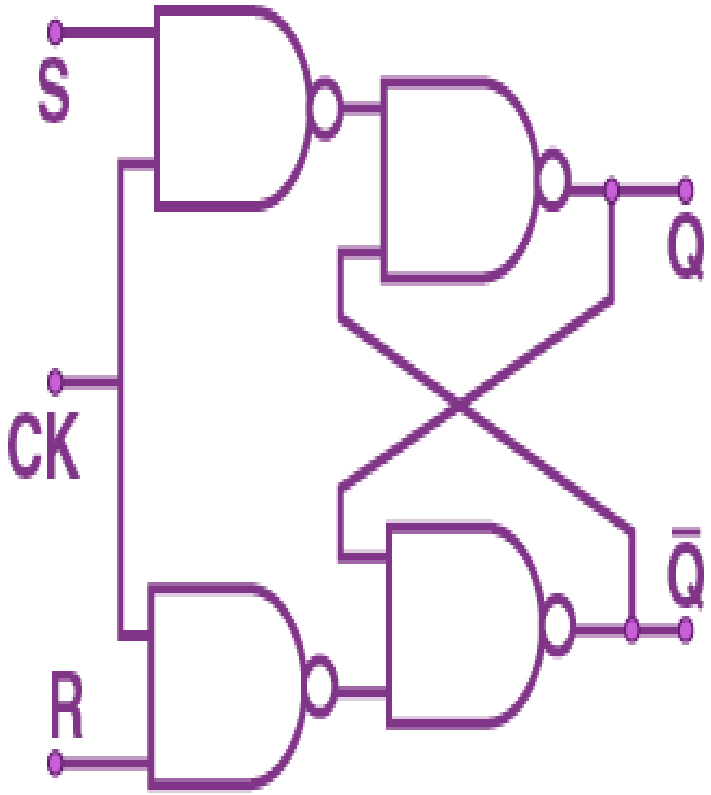
2. J-K Flip Flop

3. T Flip Flop

4. D Flip Flop

Next page, you can find the logic diagrams along with the truth tables of all the various types of flip-flops

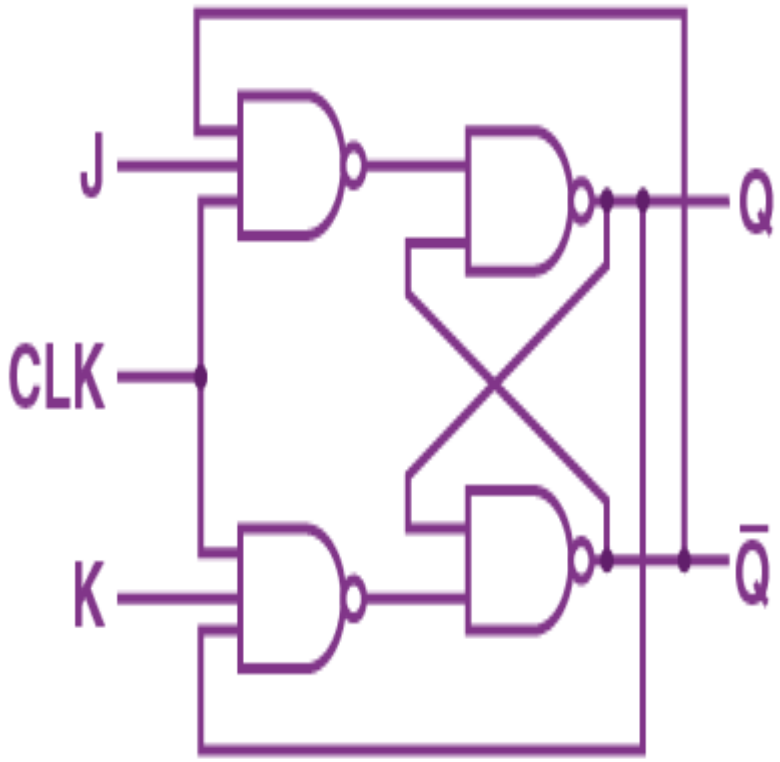
S-R Flip Flop



Truth Table

S	R	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

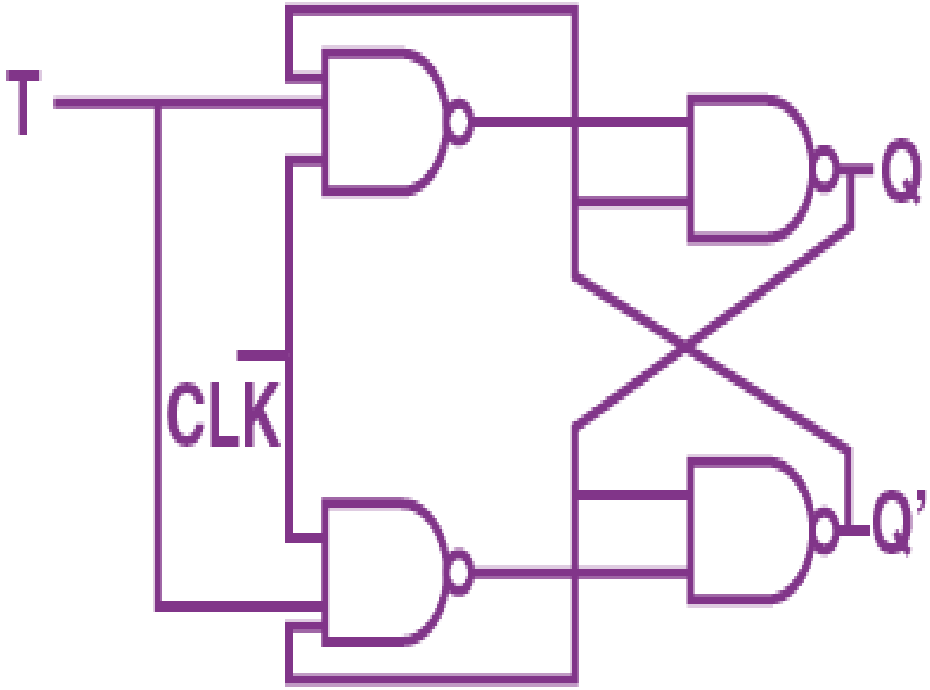
J-K Flip Flop



Truth Table

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

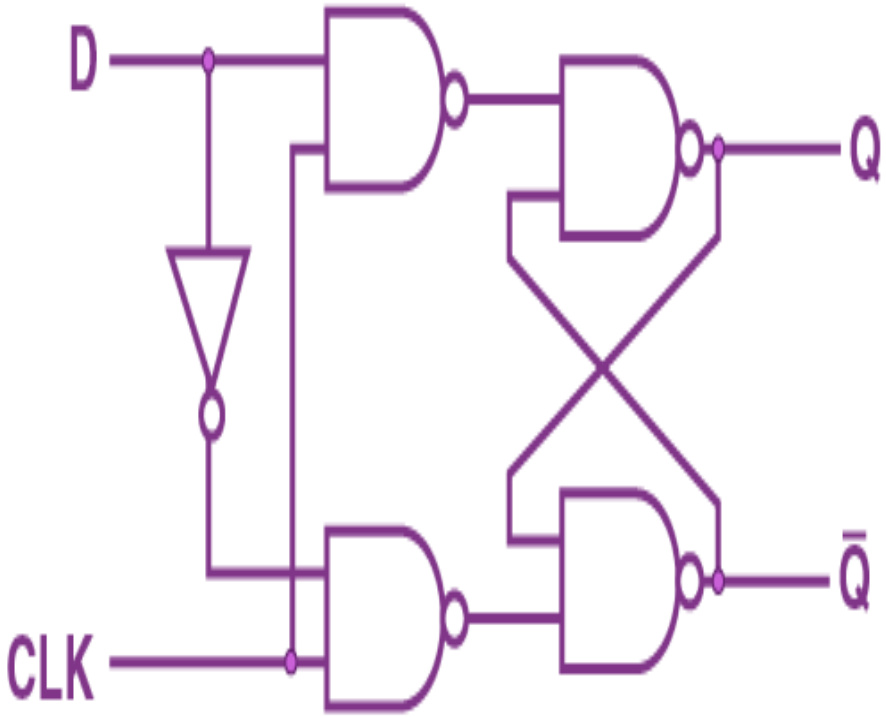
T Flip Flop



Truth Table

T	Q_N	Q_{N+1}
0	0	0
0	1	1
1	0	1
1	1	0

D Flip Flop



Truth Table

Q	D	$Q_{(t+1)}$
0	0	0
0	1	1
1	0	0
1	1	1

(3 mins)

Individual Activity
Quiz Yourself!

Complete the correct statement below?

1). The output of the sequential circuit depends upon _____

2). The flip flops are categorized into _____

3). The sequential circuits are categorized into _____

Submit your answer using the QR code:

https://docs.google.com/forms/d/e/1FAIpQLSd9AJb4Ogxy_oFxSI-omibbIEjozZVgmkMU3zn814-JcDs5uA/viewform?usp=header

Summary

Flip-Flop Type	Inputs	Output Behavior	Special Notes
SR Flip-Flop	S (Set), R (Reset)	- S=1, R=0 → Set (Q=1) - S=0, R=1 → Reset (Q=0) - S=0, R=0 → No change - S=1, R=1 → Invalid	Simple but has invalid condition
JK Flip-Flop	J, K	- J=1, K=0 → Set - J=0, K=1 → Reset - J=0, K=0 → No change - J=1, K=1 → Toggle	No invalid state, versatile
D Flip-Flop	D (Data)	Q follows D on clock edge (Q = D)	Acts as a data latch
T Flip-Flop	T (Toggle)	- T=0 → No change - T=1 → Toggle output ($Q \leftrightarrow \overline{Q}$)	Used in counters

شكراً لحسن

إصغائكم

THANK YOU ☺

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END LESSON 1: FLIP-FLOPS AND LACHES