جامعة المستقبل
نحو جامعة مستدامة

Al-Mustaqbal University - College of engineering
Department of computer engineering

Second stage

Lecture Week 12
“Digital-to-Analog Converter (DAC)”

By DR. Mohammed Kadhim Rahma

2025

Learning Objectives

After this Lecture you will be able to:

- Determine the resolution and accuracy of a digitized analog signal.
- Explain how digital-to-analog converts operate
- Compare and contrast the characteristics several commonly used digital-to-analog converts operate

Introduction

* Real signals (e.g., a voltage measured with a thermocouple or a speech signal recorded with a microphone) are analog quantities, varying continuously with time.
* Digital format offers several advantages: digital signal processing, storage, use of computers, robust transmission, etc.
* An ADC (Analog-to-Digital Converter) is used to convert an analog signal to the digital format.
* The reverse conversion (from digital to analog) is also required. For example, music stored in a DVD in digital format must be converted to an analog voltage for playing out on a speaker.
* A DAC (Digital-to-Analog Converter) is used to convert a digital signal to the analog format.

Two Problems

Input

Analog-to-digital conversion (ADC):
continuous signals converted to discrete values after sampling

Output

Digital-to-analog conversion (DAC)
Discrete values converted t continuous signals

Number of bits in digital signal determines the resolution of the digital signals. Resolution also

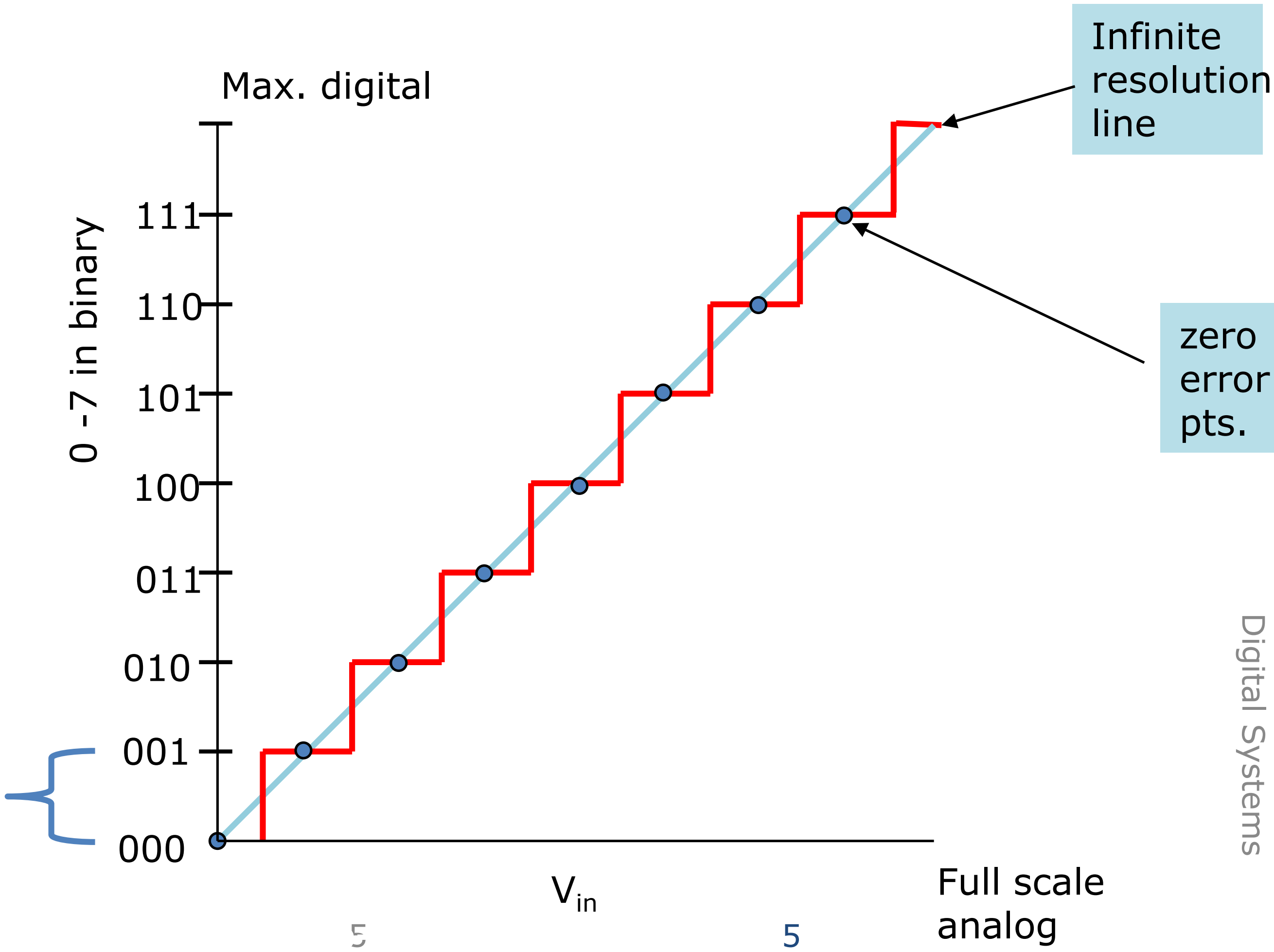
Resolution - smallest number that can be measured

Accuracy - is the number measured correct

ADC Resolution

The output is a discretized version of the continuous input.

Error determined by the step size of the digital representation



Resolution Formulas

Resolution, in terms of full scale voltage of ADC, is equal to value of Least Significant Bit (LSB)

$$V_{LSB} = \frac{V_{fs}}{2^n}$$

Where V_{fs} = full scale voltage
n = number of bits
V_{LSB} = voltage value of LSB

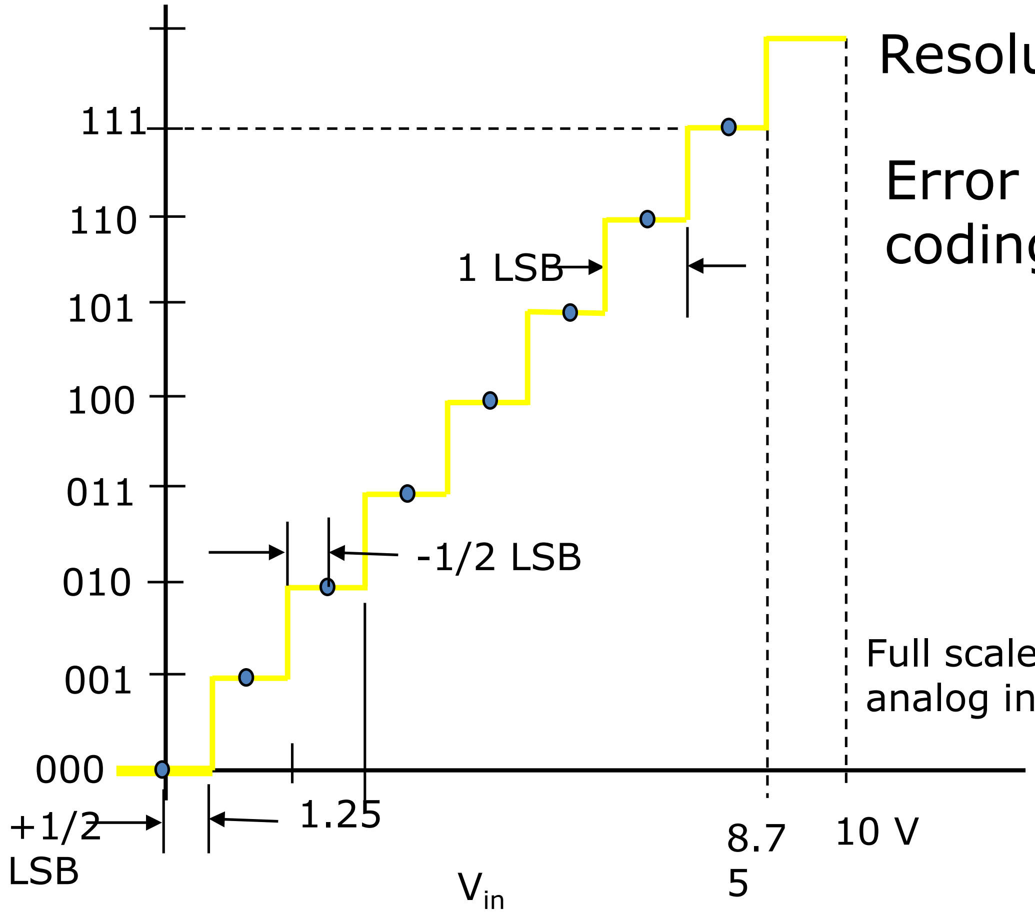
Finite bit digital conversion introduces quantization errors that range from $\pm V_{LSB}/2$

Maximum quantization error is

$$Q.E. = \frac{V_{LSB}}{2}$$

Where Q.E. = quantization error
V_{LSB} = voltage value of LSB

Digital Resolution and Error in ADC



Resolution 3-bit system

Error in natural binary coding is ±1/2 LSB

$$V_{LSB} = \frac{V_{fs}}{2^n}$$

$$V_{LSB} = \frac{10V}{2^3} = \frac{10}{8} = 125$$

All voltage values between 8.75-10 V map to the 111 code
Number of counts reduced by 1

Resolution Formulas

Percent Resolution- Based on the number of transitions (2^{n-1})

$$\%resolution = \frac{1}{2^n - 1} \cdot 100\%$$

Where n = number of bits in digital representation

<u>Example 1:</u> An 8-bit digital system is used to convert an analog signal to digital signal for a data acquisition system. The voltage range for the conversion is 0-10 V. Find the resolution of the system and the value of the least significant bit

n=8 so signal converted to 256 different levels.

V_{fs}=10 Vdc

$$V_{LSB} = \frac{V_{fs}}{2^n}$$

$$\%resolution = \frac{1}{2^n - 1} \cdot 100\%$$

$$\%resolution = \frac{1}{2^8 - 1} \cdot 100\%$$

$$\%resolution = 0.392\%$$

$$V_{LSB} = \frac{V_{fs}}{2^n} = \frac{10\ V}{2^8} = \frac{10}{256} = 0.0390625\ V$$

Example 2: The 8-bit converter of the previous example is replaced with a 12 bit system. Compute the resolution and the value of the least significant bit.

Signal converted to 4096 different levels n = 12

$$V_{LSB} = \frac{V_{fs}}{2^n}$$

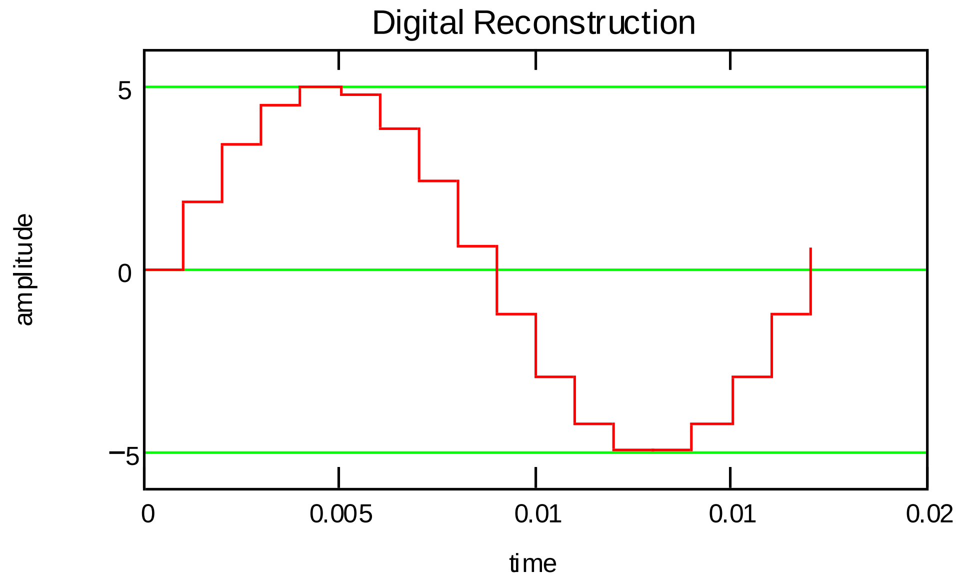
n = 12 bits V_{fs} = 10 Vd

$$V_{LSB} = \frac{V_{fs}}{2^n} = \frac{10\ V}{2^{12}} = \frac{10}{4096} = 0.002441\ V$$

$$\%resolution = \frac{1}{2^{12} - 1} \cdot 100\%$$

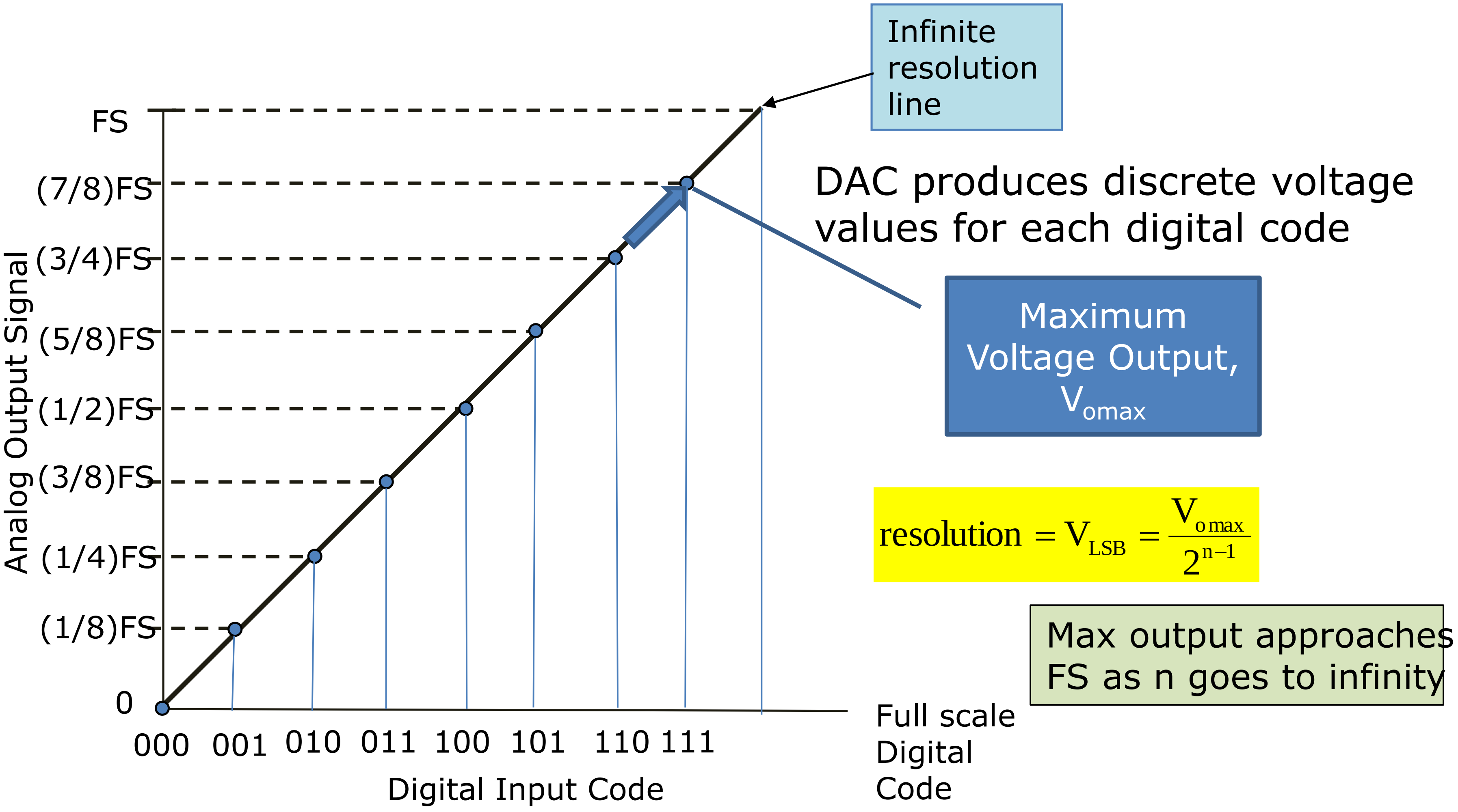
$$\%resolution = 0.0244\%$$

Difference between analog value and digital reconstruction is quantizing error



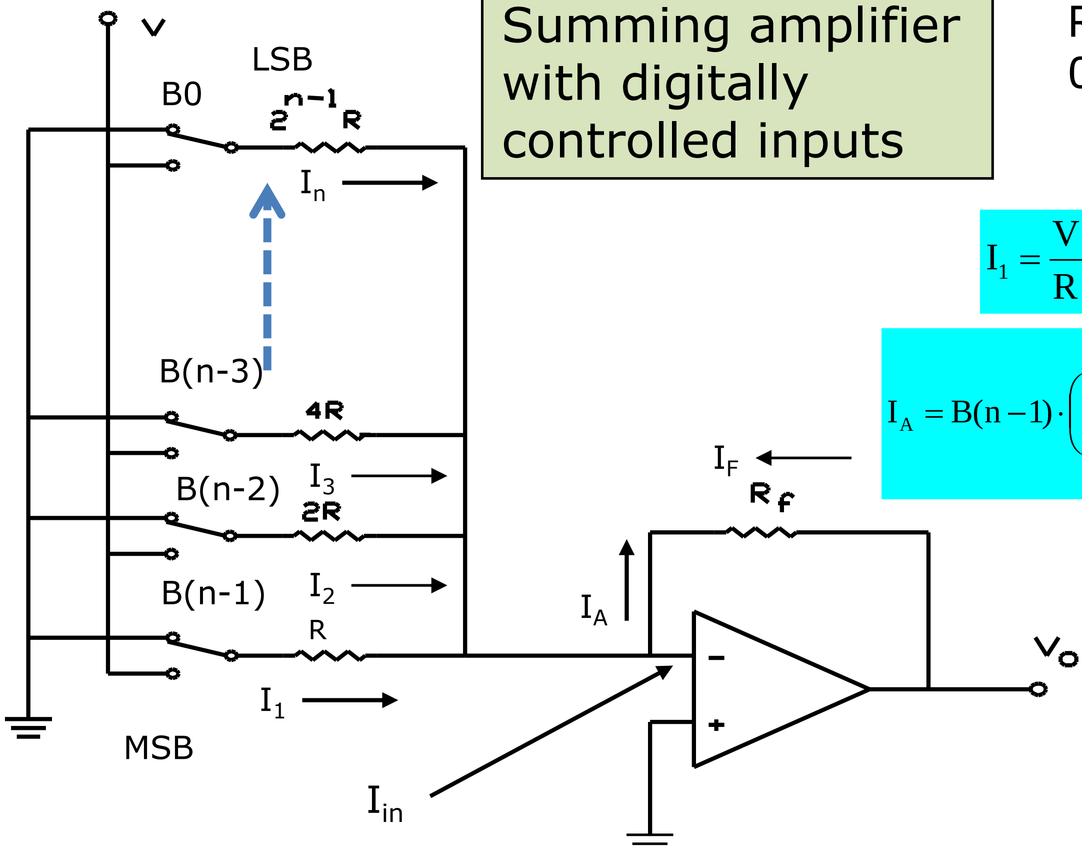
Digital-to-Analog Conversion

Digital-to-Analog Converter (DAC) Transfer Function



DAC produces discrete voltage values for each digital code

Binary-Weighted Resistor DAC



Summing amplifier with digitally controlled inputs

Rules of Ideal OP AMPs $I_{in} = 0$, Z_{in} = infinity

$$I_A = I_1 + I_2 + I_3 .... + I_n$$

$$I_1 = \frac{V}{R}, \quad I_2 = \frac{V}{2R}, \quad I_3 = \frac{V}{4R}, \ldots \; I_n = \frac{V}{(2^{n-1})R}$$

$$I_A = B(n-1)\cdot\left(\frac{V}{R}\right) + B(n-2)\cdot\left(\frac{V}{2R}\right) + B(n-3)\cdot\left(\frac{V}{4R}\right) \ldots + B0\cdot\left(\frac{V}{(2^{n-1})R}\right)$$

Formula for output V

$$V_0 = -I_F \cdot R_F$$

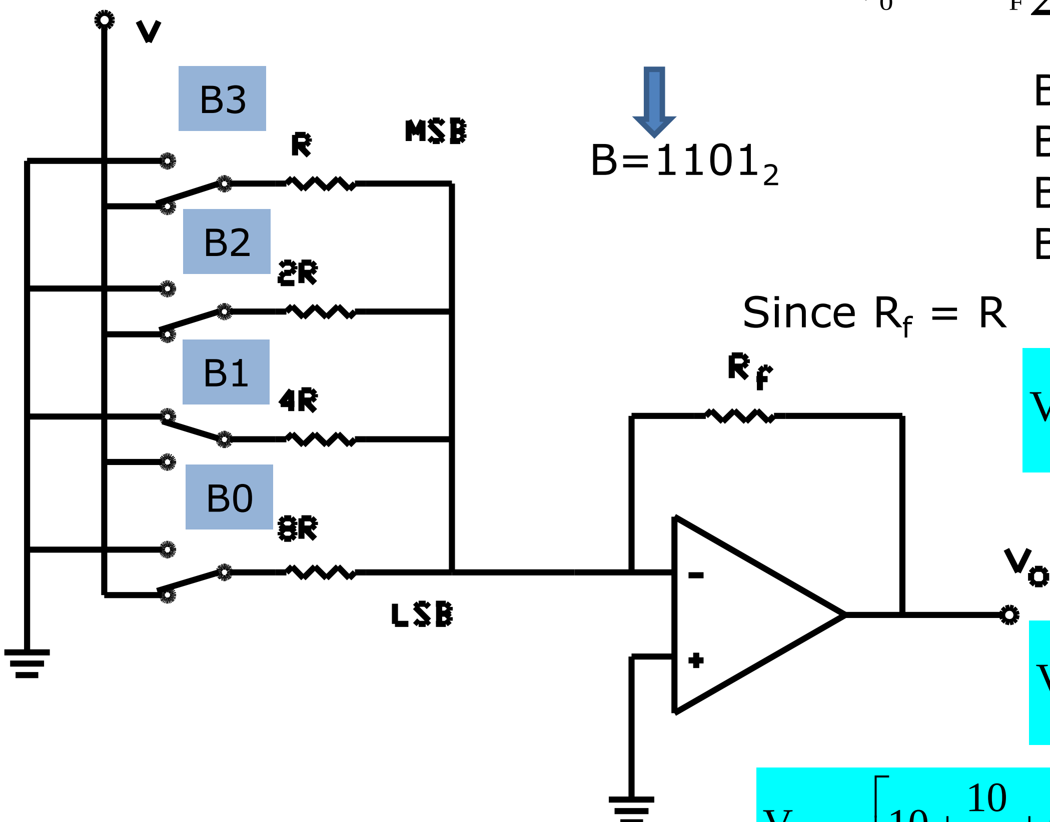
$$V_0 = -R_F \sum_{i=1}^{n} \frac{B(n-i)\cdot V}{2^{i-1} R}$$

B0, B(n-3), B(n-2), ...B(n-1) take on values of 1 or 0 depending of the digital output controlling switch

Binary Weighted DAC Example

Example: For the binary-weighted resistor DAC below find the output when the input word is 1101_2 V = 10 Vdc, R_f = R

$$V_0 = -R_F \sum_{i=1}^{n} \frac{B(n-i)\cdot V}{2^{i-1}R} \qquad n=4$$



$B=1101_2$

B(4-1)=B3=1 MSB
B(4-2)=B2=1
B(4-3)=B1=0
B(4-4)=B0=1 LSB

Since R_f = R

$$V_o = -R\cdot\left[\frac{B3\cdot V}{2^{1-1}R} + \frac{B2\cdot V}{2^{2-1}R} + \frac{B1\cdot V}{2^{3-1}R} + \frac{B0\cdot V}{2^{4-1}R}\right]$$

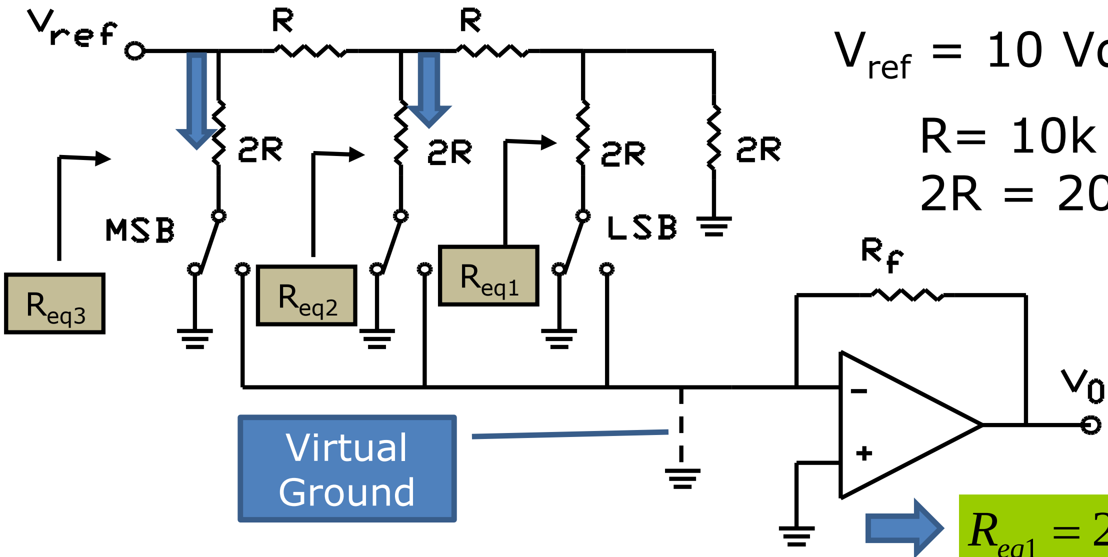
$$V_o = -\frac{R}{R}\cdot\left[\frac{1\cdot V}{2^0} + \frac{1\cdot V}{2^1} + \frac{0\cdot V}{2^2} + \frac{1\cdot V}{2^3}\right]$$

$$V_o = -1\cdot\left[\frac{1\cdot 10}{2^0} + \frac{1\cdot 10}{2^1} + \frac{0\cdot 10}{2^2} + \frac{1\cdot 10}{2^3}\right]$$

$$V_o = -\left[10 + \frac{10}{2} + 0 + \frac{10}{8}\right] = -[10+5+1.25] = -16.25$$

R-2R Binary Ladder DAC

R-2R Ladder produces binary weighted current values from only 2 resistance values.



V_{ref} = 10 Vdc

R= 10k

2R = 20k

Find R_{eq3} by assuming all switches are closed to ground

$$R_{eq1} = 20\ \text{k}\Omega \parallel 20\ \text{k}\Omega + 10\ \text{k}\Omega = 20\ \text{k}\Omega$$

$$R_{eq2} = R_{eq1} \parallel 20\ \text{k}\Omega + 10\ \text{k}\Omega = 20\ \text{k}\Omega$$

$$R_{eq3} = R_{eq2} \parallel 20\ \text{k}\Omega = 10\ \text{k}\Omega$$

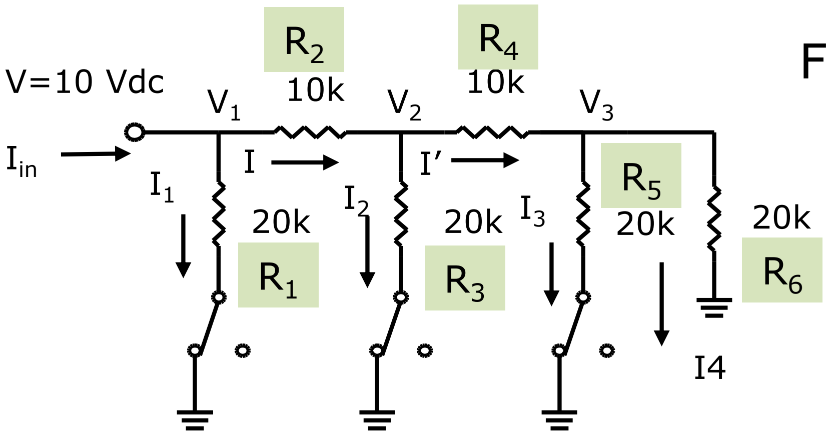
$$R_{eq3} = 10\ \text{k}\Omega$$

Network equivalent resistance is R

<u>Circuit Analysis</u>

Currents through each 2R value resistor directed to OP AMP or ground by digital switch

R-2R Ladder Analysis (Continued)



Find I_{in} from R_{eq3} and V

$$I_{in} = \frac{V}{R_{eq3}} = \frac{10\ \text{V}}{10\ \text{k}\Omega} = 1.0\ \text{mA}$$

$$I_1 = \frac{V_1}{R_1} = \frac{10\ \text{V}}{20\ \text{k}\Omega} = 0.5\ \text{mA} \quad I = I_{in} - I_1 = 1\ \text{mA} - 0.5\ \text{mA} = 0.5\ \text{mA}$$

$$V_2 = V_1 - I \cdot R_2 \quad \Rightarrow \quad V_2 = 10 - 0.5\ \text{mA} \cdot 10\ \text{k}\Omega = 10 - 5 = 5\ \text{V}$$

$$I_2 = \frac{V_2}{R_3} = \frac{5\ \text{V}}{20\ \text{k}\Omega} = 0.25\ \text{mA} \quad I' = I_1 - I_2 = 0.5\ \text{mA} - 0.25\ \text{mA} = 0.25\ \text{mA}$$

$$V_3 = V_2 - I' \cdot R_4 \quad \Rightarrow \quad V_3 = 5 - 0.25\ \text{mA} \cdot 10\ \text{k}\Omega = 5 - 2.5 = 2.5\ \text{V}$$

$$I_3 = \frac{V_3}{R_5} = \frac{2.5\ \text{V}}{20\ \text{k}\Omega} = 0.125\ \text{mA} \quad I_4 = \frac{V_3}{R_6} = \frac{2.5\ \text{V}}{20\ \text{k}\Omega} = 0.125\ \text{mA}$$

Current Values

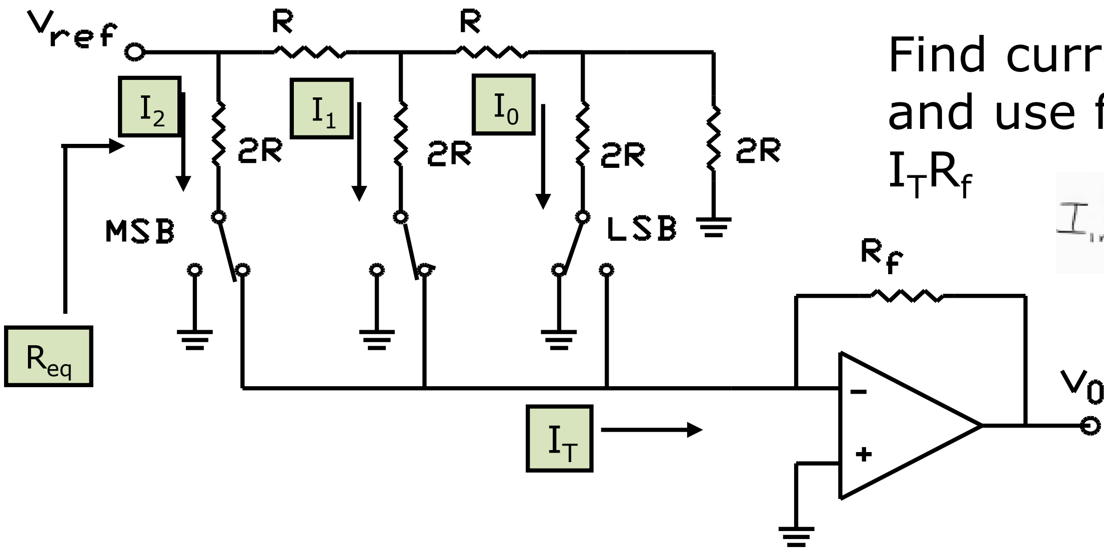
I_1 = 0.5 mA MSB
I_2 = 0.25 mA
I_3 = 0.125 mA LSB

Current values directed to OP AMP summing junction or ground. At summing junction:

$$V_o = -R_f \cdot I_T$$

R-2R Example

Find the output voltage for the R-2R DAC shown below. The digital input is 110_2. R=15k, 2R=30k and R_f=15k , Vref=5 Vdc



Find currents I_0, I_1, I_2 and use formula $V_0 = -I_T R_f$

$$I_{in} = \frac{V_{ref}}{R} = \frac{5V}{15k\Omega} = 0.333 \text{ mA}$$

$$I_2 = \frac{V_{ref}}{2R} = \frac{5}{30k\Omega} = \boxed{0.1667 \text{ mA}}$$

All other currents reduced by factor of 2.

$$I_1 = \frac{I_2}{2} \Rightarrow I_1 = \frac{0.1667 \text{ mA}}{2} = \boxed{0.0833 \text{ mA}} = 83.33 \text{ µA}$$

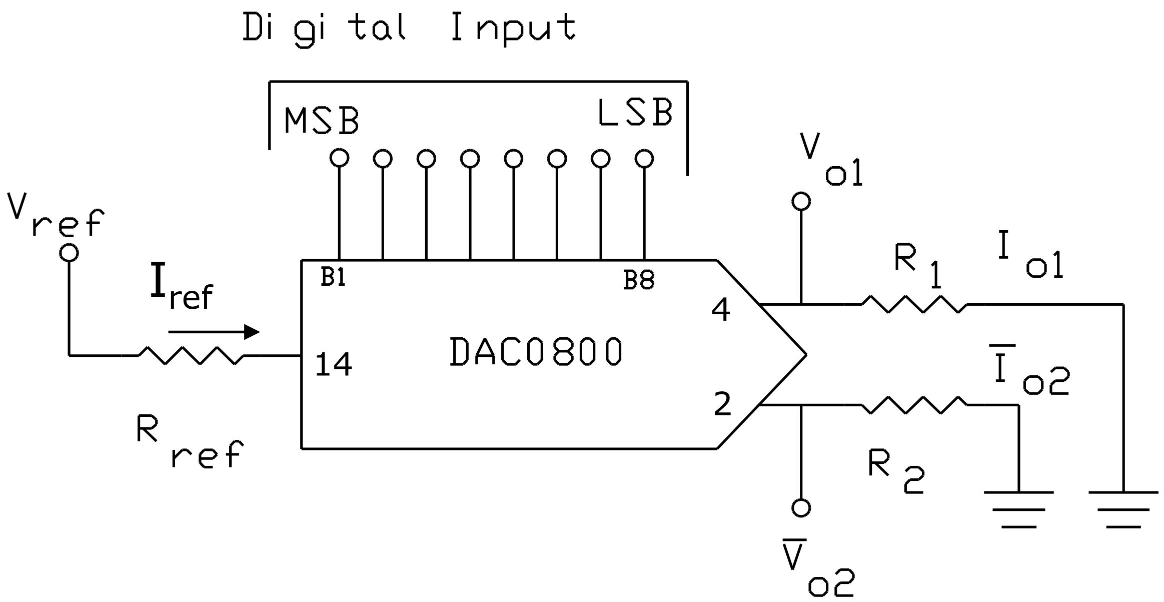
$$I_0 = \frac{I_1}{2} = \frac{0.0833 \text{ mA}}{2} = \boxed{0.04166 \text{ mA}} = 41.66 \text{ µA}$$

$$I_T = I_2 + I_1 = 0.1667 \text{ mA} + 0.0833 \text{ mA} = 0.25003 \text{ mA}$$

$$V_0 = -I_T R_f = -(0.25003 \text{ mA})(15 \text{ k}\Omega) = \boxed{-3.75045 \text{ V}}$$

Commercial DACs: DAC0800 Family

Devices used in practical designs use integrated R-2R networks and transistor switching. They have TTL compatible inputs.



Design Equations

$$I_{ref} = \frac{V_{ref}}{R_{ref}}$$

$$I_0 = I_{ref}\left(\frac{D}{256}\right)$$

D = decimal equivalent of binary input

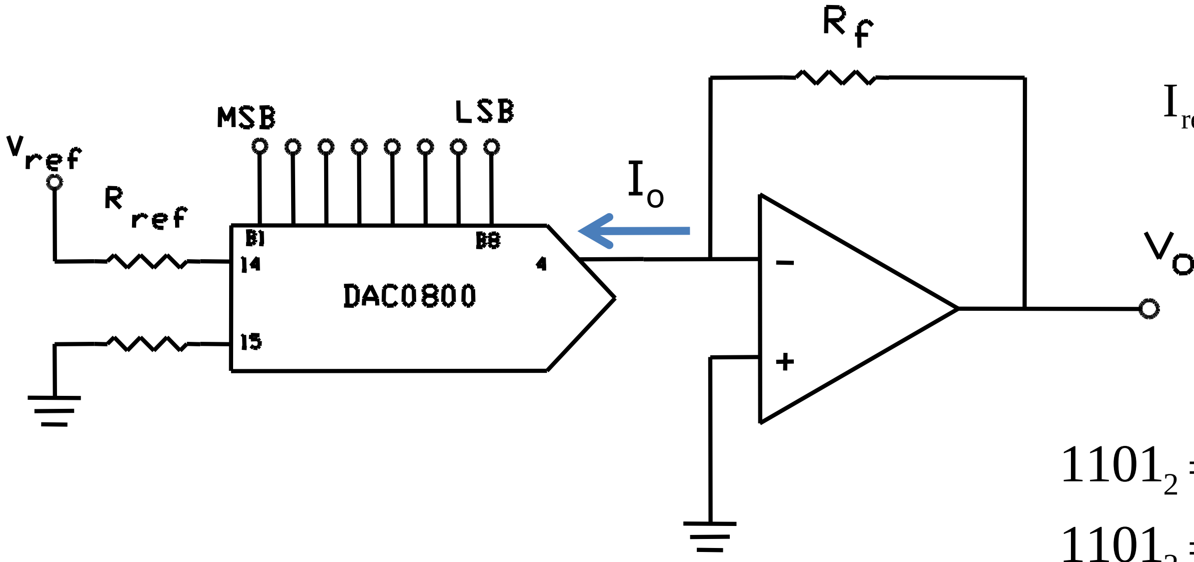
8-bit binary code converted to 256 levels of I_0. Full scale value set by reference current. 1 bit change produces change of 1/256 in I_0

$$I_{fs} = \frac{V_{ref}}{R_{ref}}\left(\frac{255}{256}\right)$$

Full scale output

DAC0800 Example

Use OP AMP to convert current to voltage. The reference voltage is +10 V dc and the reference resistance is 5kΩ. The value of R_f = 2.5kΩ



$$I_{ref} = \frac{V_{ref}}{R_{ref}} = \frac{10\text{ V}}{5\text{ k}\Omega} = 2.0\text{ mA}$$

a.) convert binary to decimal

$$1101_2 = 2^3(1) + 2^2(1) + 2^1(0) + 2^0(1)$$

$$1101_2 = 8 + 4 + 1 = 13$$

$$D = 13$$

a.) Digital input 00001101_2

b.) Digital input 10001101_2

Find I_0

$$I_0 = I_{ref}\left(\frac{D}{256}\right)$$

$$I_0 = (2.0\text{ mA})\left[\frac{13}{256}\right] = 0.1015625\text{ mA} = 101.5625\ \mu\text{A}$$

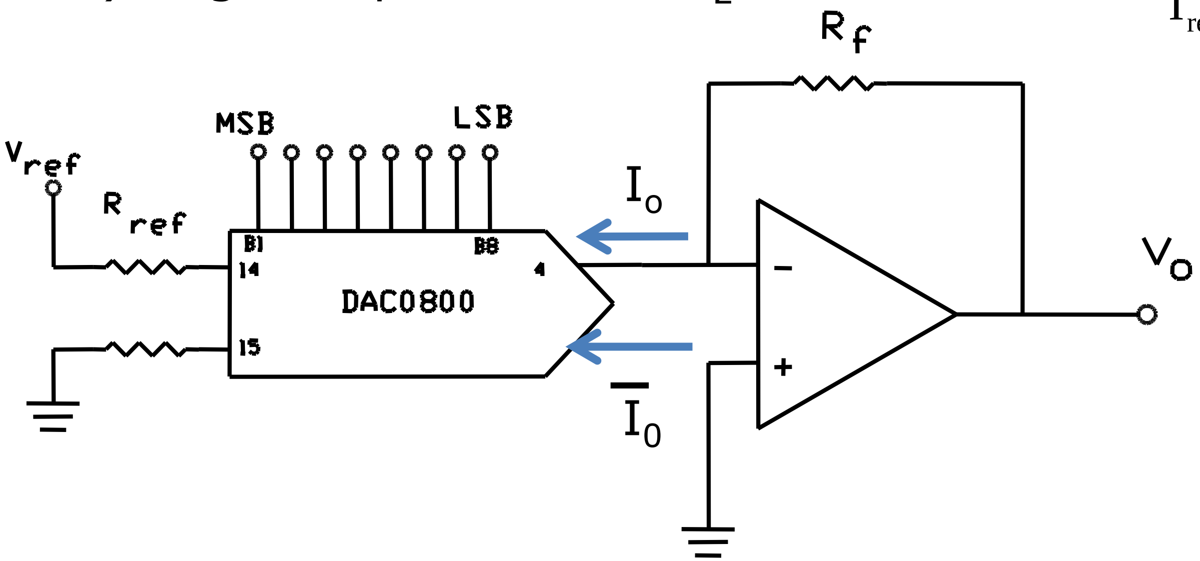
I_o enters so negative

$$V_0 = -(-I_0)\cdot R_f = -(-0.1015625\text{ mA})(2.5\text{ k}\Omega) = 0.253906\text{ V}$$

DAC0800 Example (Continued)

b.) Digital input 10001101_2

$$I_{ref} = \frac{V_{ref}}{R_{ref}} = \frac{10\text{ V}}{5\text{ k}\Omega} = 2.0\text{ mA}$$



b.) convert binary to decimal

$$10001101_2 = 2^7(1) + 2^6(0) + 2^5(0) + 2^4(0) + 2^3(1) + 2^2(1) + 2^1(0) + 2^0(1)$$

$$1101_2 = 128 + 8 + 4 + 1 = 141$$

$$D = 141$$

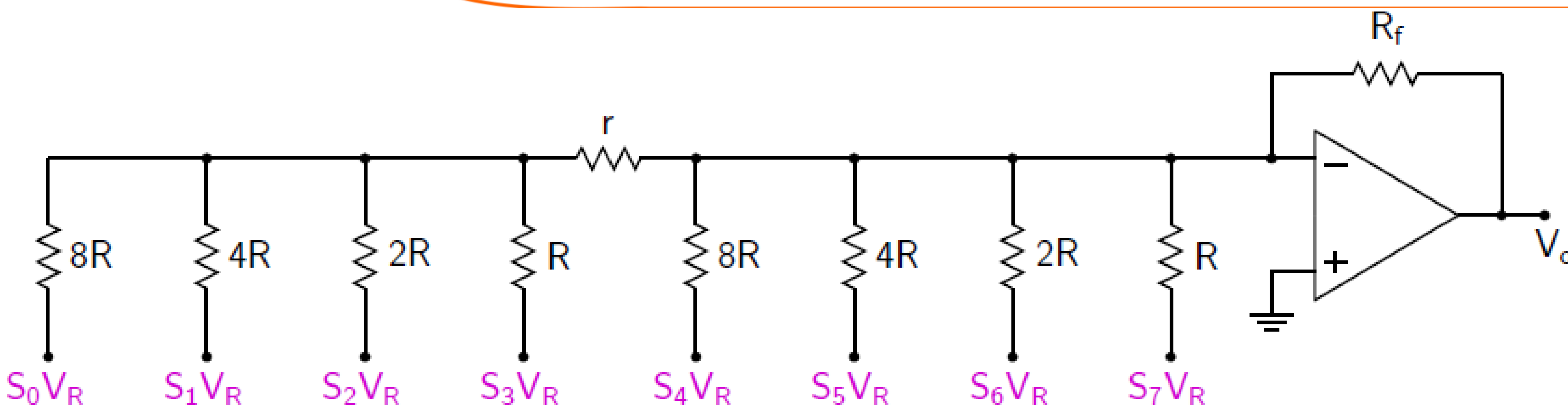
I_o enters so negative

$$\bar{I}_0 = I_{ref} - I_0 = 2.0 - 1.1015625\text{mA} = 0.8984375\text{mA}$$

$$I_0 = I_{ref}\left(\frac{D}{256}\right) = (2.0)\cdot\left(\frac{141}{256}\right) = 1.1015626\text{ mA}$$

$$V_0 = -(-I_0)\cdot R_f = -(-1.1015625\text{ mA})(2.5\text{ k}\Omega) = 2.753906\text{ V}$$

DAC: home work

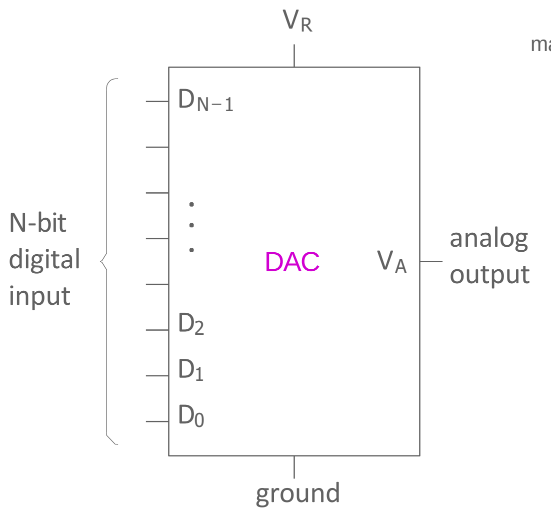


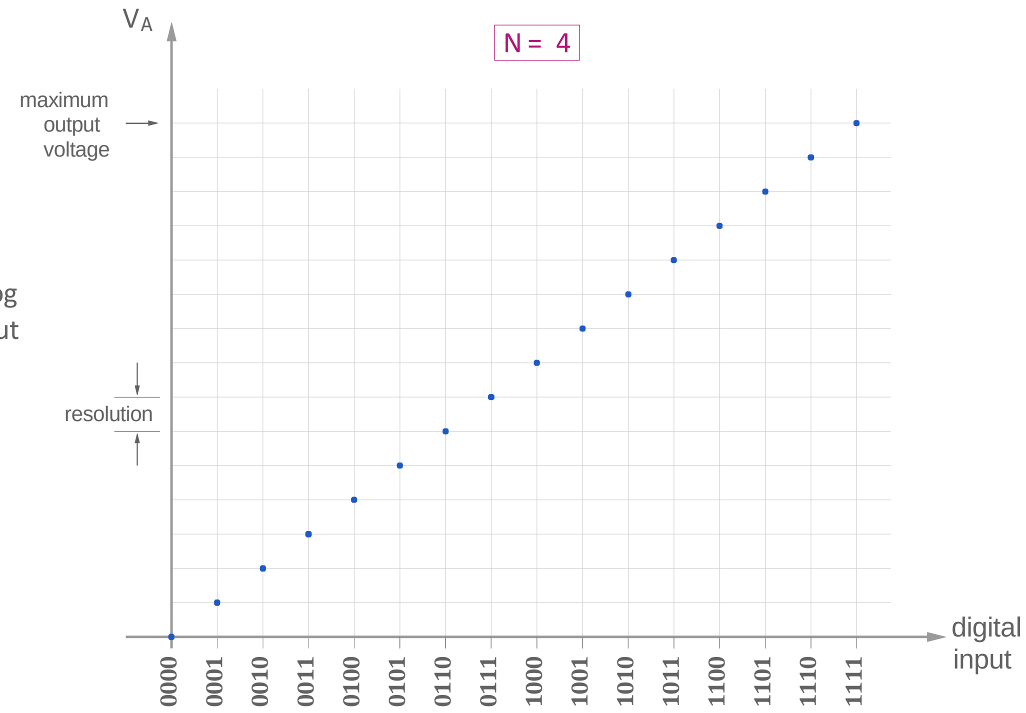
* Find the value of r for the circuit to work as a regular (i.e., binary to analog) DAC.
* Find the value of r for the circuit to work as a BCD to analog DAC

https://docs.google.com/forms/d/e/1FAIpQLSdHTIou63HKXrUfYDB_8CuxvKe8Mb0UHkR2JUqFVM02KyOPkg/viewform?usp=header

Then Submit your answer using the QR code or the link

Summary





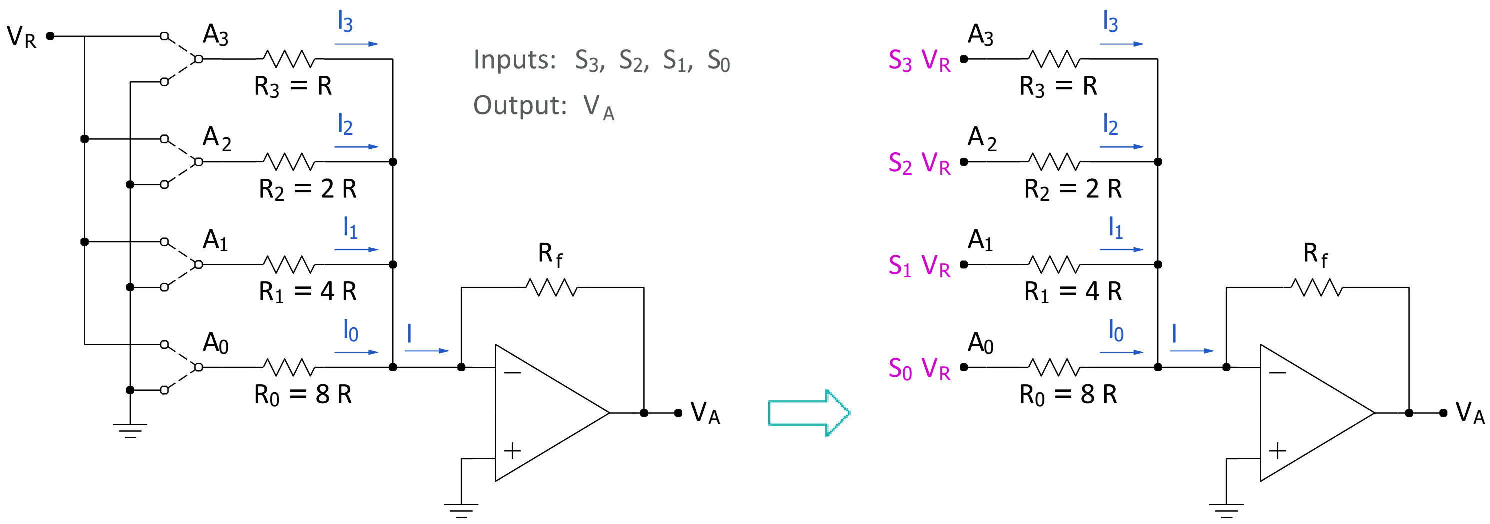
* For a 4-bit DAC, with input $S_3S_2S_1S_0$, the output voltage is

$$V_A = K\ \left((S_3 \times 2^3) + (S_2 \times 2^2) + (S_1 \times 2^1) + (S_0 \times 2^0) \right).$$

In general, $V_A = K \sum_0^{N-1} S_k 2^k$.

* K is proportional to the reference voltage V_R. Its value depends on how the DAC is implemented.

DAC using binary-weighted resistors



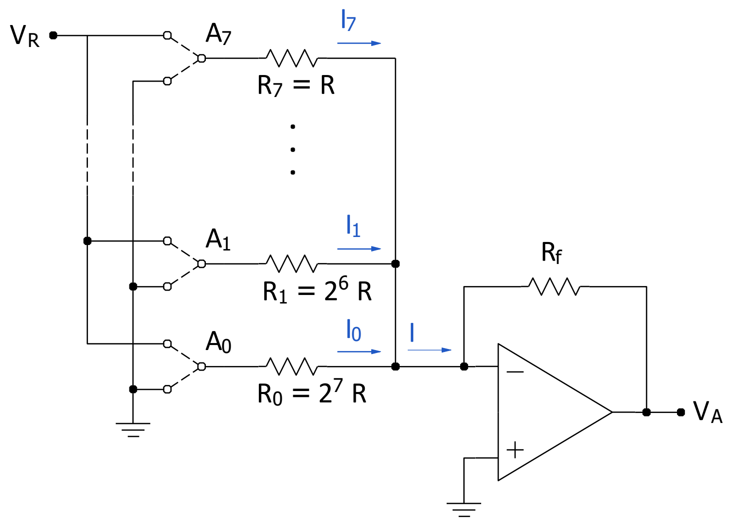
* If the input bit S_k is 1, A_k gets connected to V_R; else, it gets connected to ground. $\rightarrow V(A_k) = S_k \times V_R$.

* Since the inverting terminal of the op-amp is at virtual ground, $I_k = \dfrac{V(A_k) - 0}{R_k} = \dfrac{S_k V_R}{R_k}$.

* $I = \dfrac{S_0 V_R}{8R} + \dfrac{S_1 V_R}{4R} + \dfrac{S_2 V_R}{2R} + \dfrac{S_3 V_R}{R} = \dfrac{V_R}{2^{N-1} R} \sum_{0}^{N-1} S_k \times 2^k \;\; (N = 4)$.

* The output voltage is $V_o = -R_f \, I = -V_R \dfrac{R_f}{2^{N-1} R} \sum_{0}^{N-1} S_k \times 2^k$.

DAC using binary-weighted resistors: Example



* Consider an 8-bit DAC with $V_R = 5\,\text{V}$. What is the smallest value of R which will limit the current drawn from the supply (V_R) to 10 mA?

Maximum current is drawn from V_R when the input is 1111 1111.

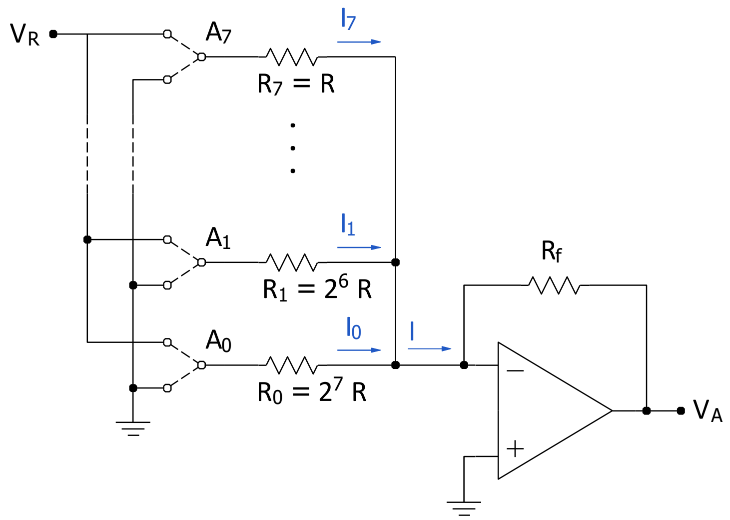
→ All nodes A_0 to A_7 get connected to V_R.

$$\rightarrow 10\,\text{mA} = \frac{V_R}{R} + \frac{V_R}{2R} + \cdots + \frac{V_R}{2^7 R} = \frac{1}{2^7}\frac{V_R}{R}\left(2^0 + 2^1 + \cdots + 2^7\right)$$

$$= \frac{1}{2^7}\frac{V_R}{R}\left(2^8 - 1\right) = \frac{255}{128}\frac{V_R}{R} \rightarrow R_{min} = \frac{5\,\text{V}}{10\,\text{mA}} \times \frac{255}{128} = 996\,\Omega\,.$$

(Ref.: K. Gopalan, *Introduction to Digital Microelectronic Circuits*, Tata McGraw-Hill, New Delhi, 1998)

DAC using binary-weighted resistors: Example (from Gopalan)

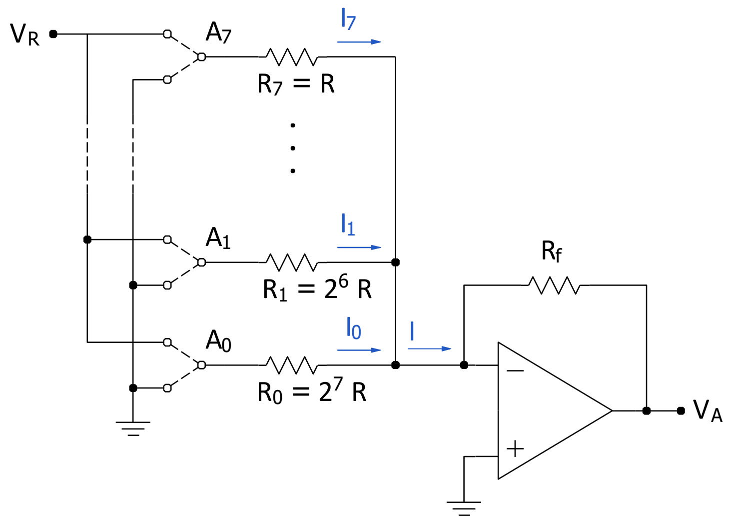


* If $R_f = R$, what is the resolution (i.e., ΔV_A corresponding to the input LSB changing from 0 to 1 with other input bits constant)?

$$V_A = -V_R \frac{R_f}{2^{N-1}R} \left[S_7 2^7 + \cdots + S_1 2^1 + S_0 2^0 \right]$$

$$\rightarrow \Delta V_A = \frac{V_R}{2^{N-1}} \frac{R_f}{R} = \frac{5\,\text{V}}{2^{8-1}} \times 1 = \frac{5}{128} = 0.0391\,\text{V}.$$

DAC using binary-weighted resistors: Example (from Gopalan)



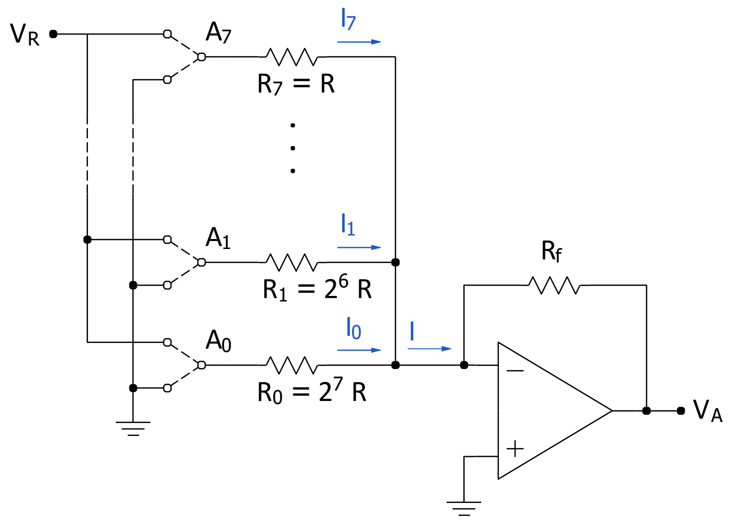
* What is the maximum output voltage (in magnitude)?

$$V_A = -\frac{V_R}{2^{N-1}}\frac{R_f}{R}\left[S_7 2^7 + \cdots + S_1 2^1 + S_0 2^0\right].$$

Maximum V_A (in magnitude) is obtained when the input is $1111\ 1111$.

$$|V_A|^{max} = \frac{5}{128} \times 1 \times \left[2^0 + 2^1 + \cdots + 2^7\right] = \frac{5}{128} \times \left(2^8 - 1\right) = 5 \times \frac{255}{128} = 9.961\,\text{V}.$$

DAC using binary-weighted resistors: Example (from Gopalan)

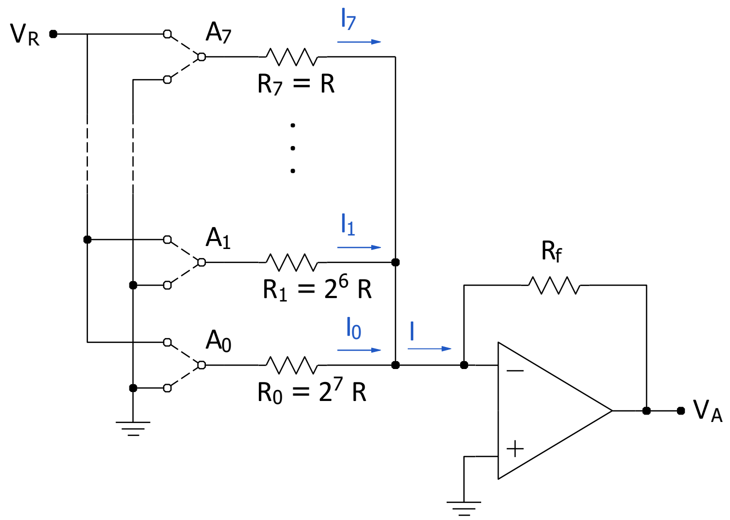


- Find the output voltage corresponding to the input 1010 1101.

$$V_A = -\frac{V_R}{2^{N-1}} \frac{R_f}{R} \left[S_7 2^7 + \cdots + S_1 2^1 + S_0 2^0 \right] .$$

$$= -\frac{5}{128} \times 1 \times \left[2^7 + 2^5 + 2^3 + 2^2 + 2^0 \right] = -5 \times \frac{173}{128} = -6.758\,\text{V} .$$

DAC using binary-weighted resistors: Example (from Gopalan)



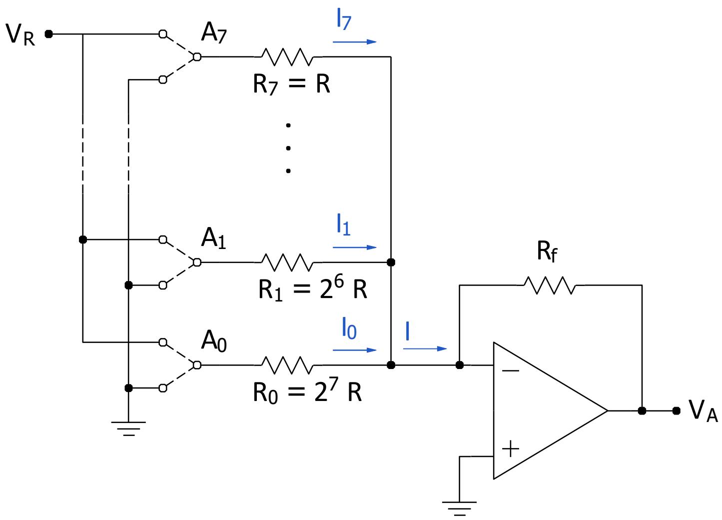
* If the resistors are specified to have a tolerance of 1 %, what is the range of $|V_A|$ corresponding to input 1111 1111?

  $|V_A|$ is maximum when (a) currents I_0, I_1, etc. assume their maximum values, with $R_k = R_k^0 \times (1 - 0.01)$ and (b) R_f is maximum, $R_f = R_f^0 \times (1 + 0.01)$.
  (The superscript '0' denotes nominal value.)

  $$\rightarrow\ |V_A|^{\text{max}}_{11111111} = V_R \times \frac{255}{128} \times \frac{R_f}{R}^{\text{max}} = 5 \times \frac{255}{128} \times \frac{1.01}{0.99} = 10.162\,\text{V}.$$

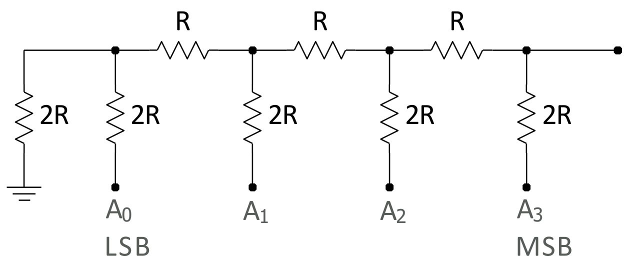
  Similarly, $|V_A|^{\text{min}}_{11111111} = 5 \times \dfrac{255}{128} \times \dfrac{0.99}{1.01} = 9.764\,\text{V}.$

DAC using binary-weighted resistors: Example (from Gopalan)



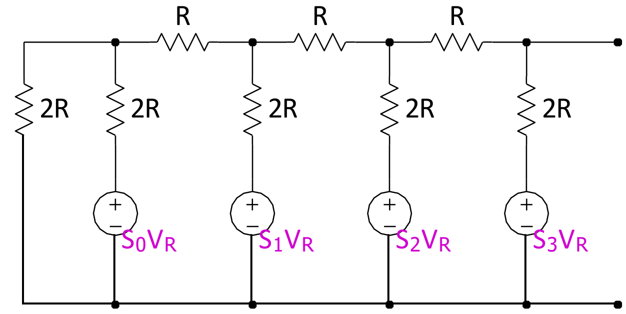
* ΔV_A for input $1111\ 1111$ = $10.162 - 9.764 \approx 0.4$V which is larger than the resolution (0.039 V) of the DAC. This situation is not acceptable.
* The output voltage variation can be reduced by using resistors with a smaller tolerance. However, it is difficult to fabricate an IC with widely varying resistance values (from R to $2^{N-1}R$) and each with a small enough tolerance. $\rightarrow$ use $R - 2R$ ladder network instead.

R-2R ladder network

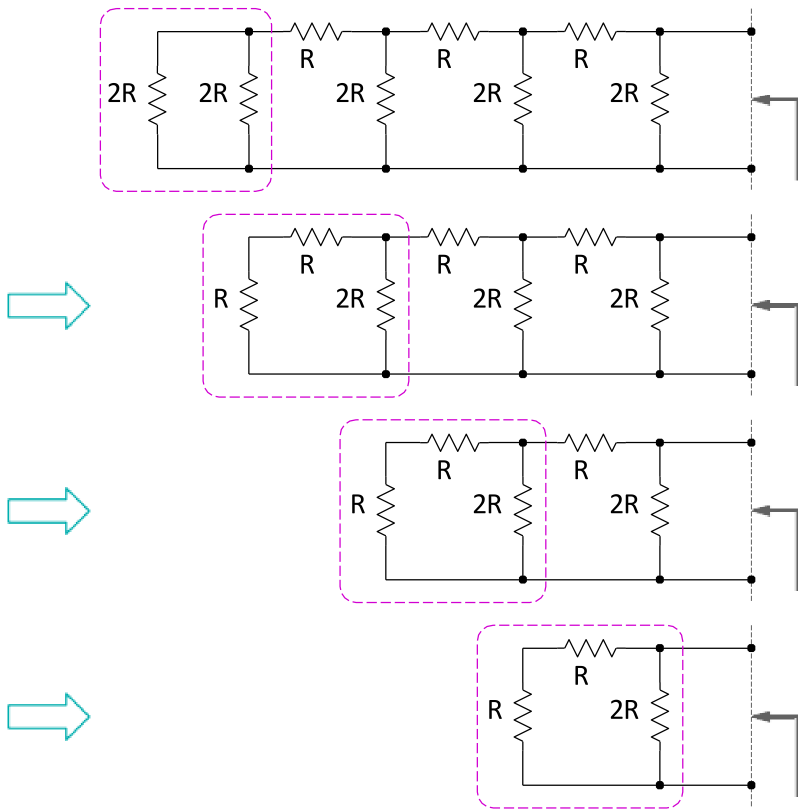


Node A_k is connected to V_R if input bit S_k is 1; else, it is connected to ground.

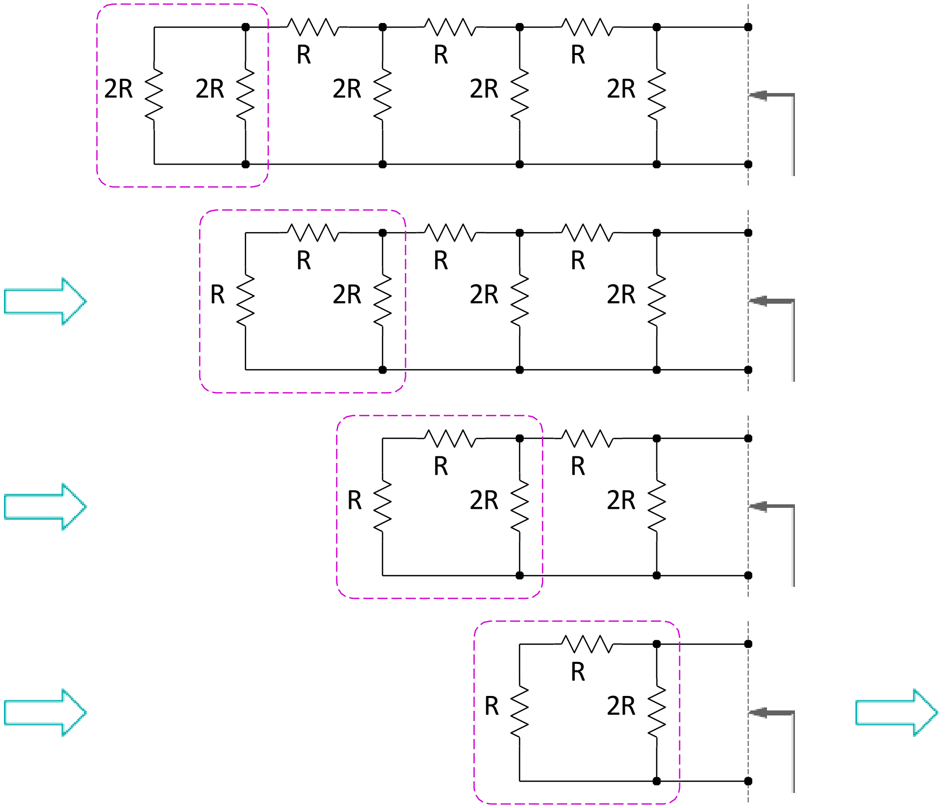
The original network is equivalent to



R-2R ladder network: Thevenin resistance

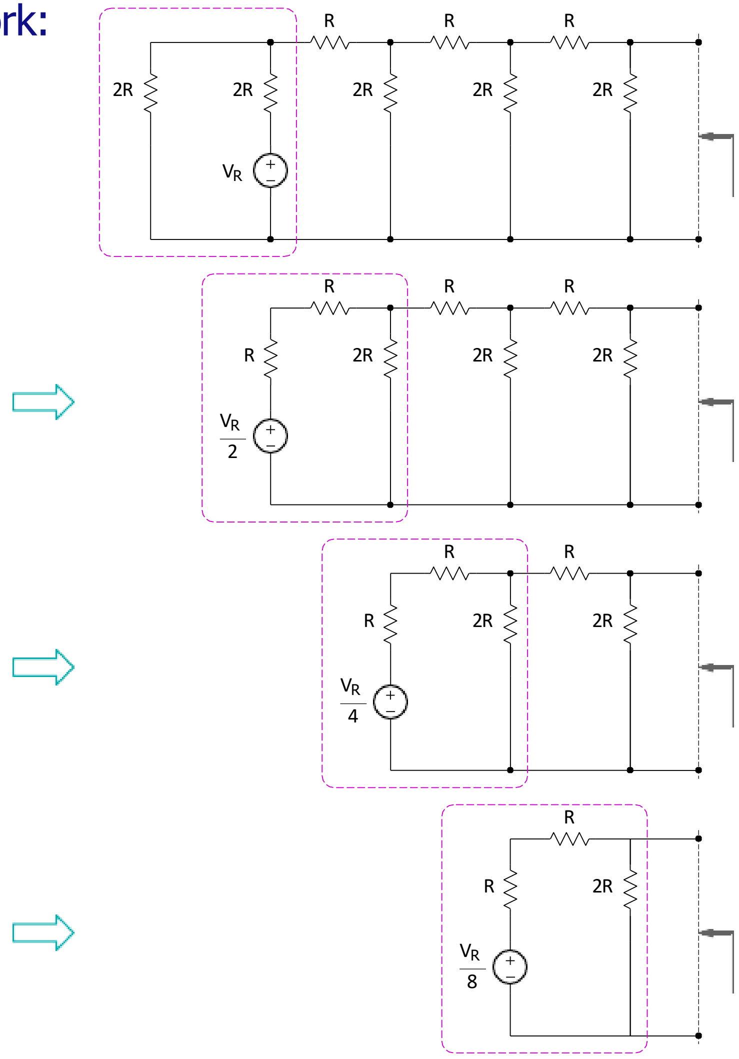


R-2R ladder network: Thevenin resistance

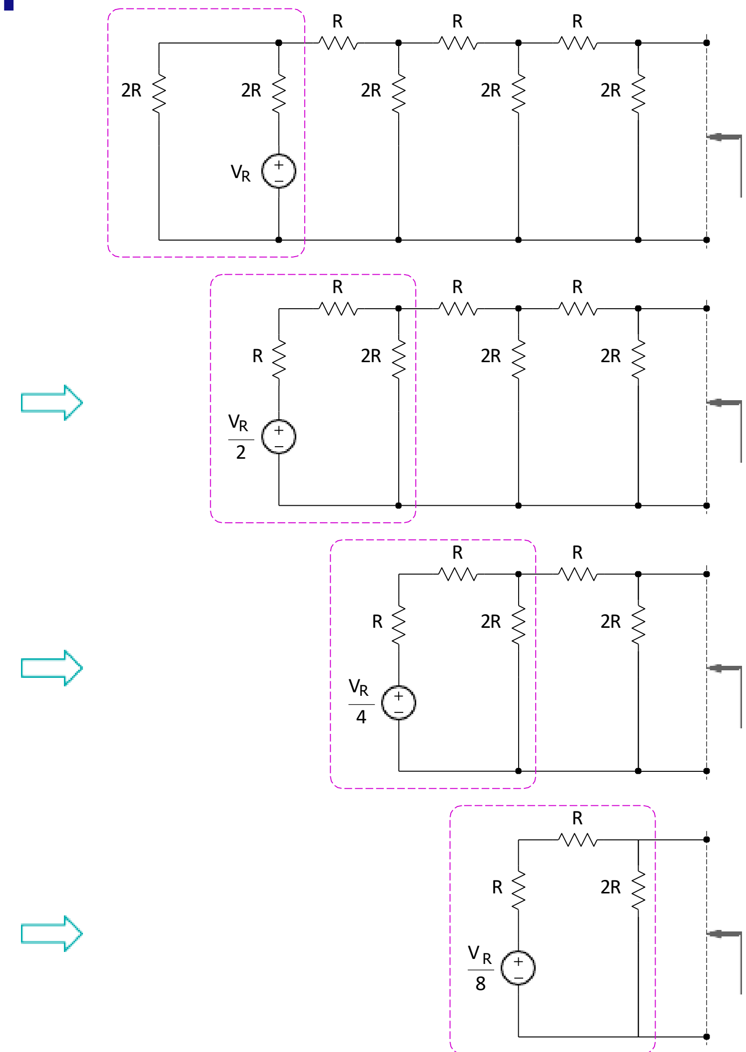


$R_{Th} = R$

R-2R ladder network:
V_{Th} for $S_0 = 1$

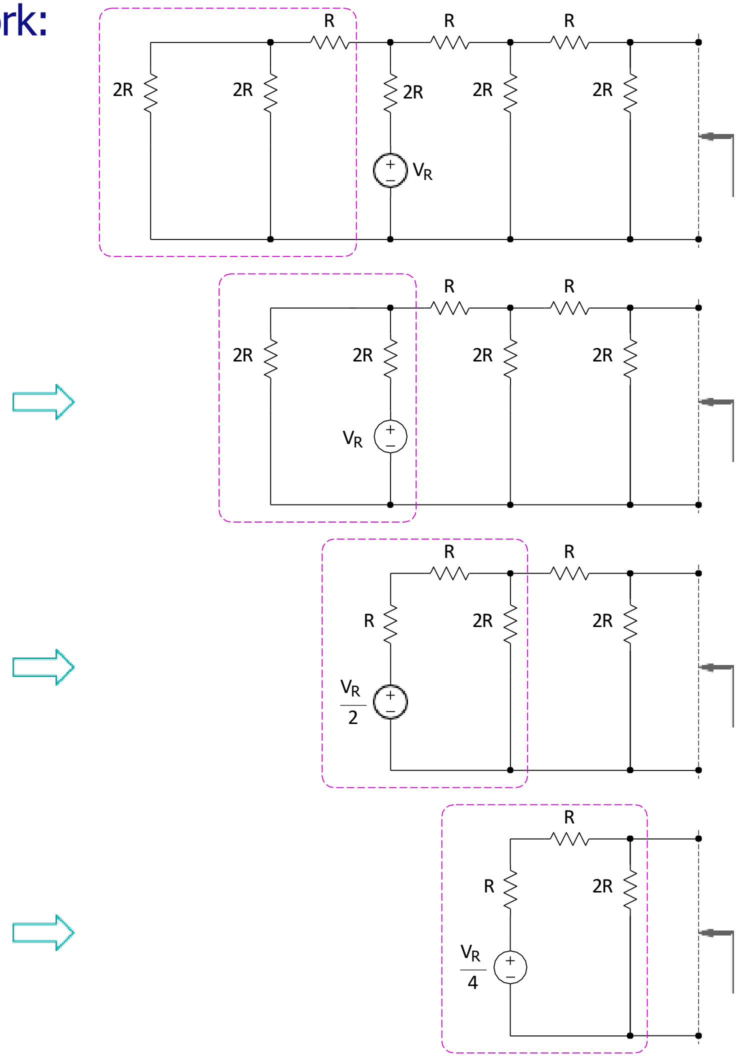


R-2R ladder network: V_{Th} for $S_0 = 1$

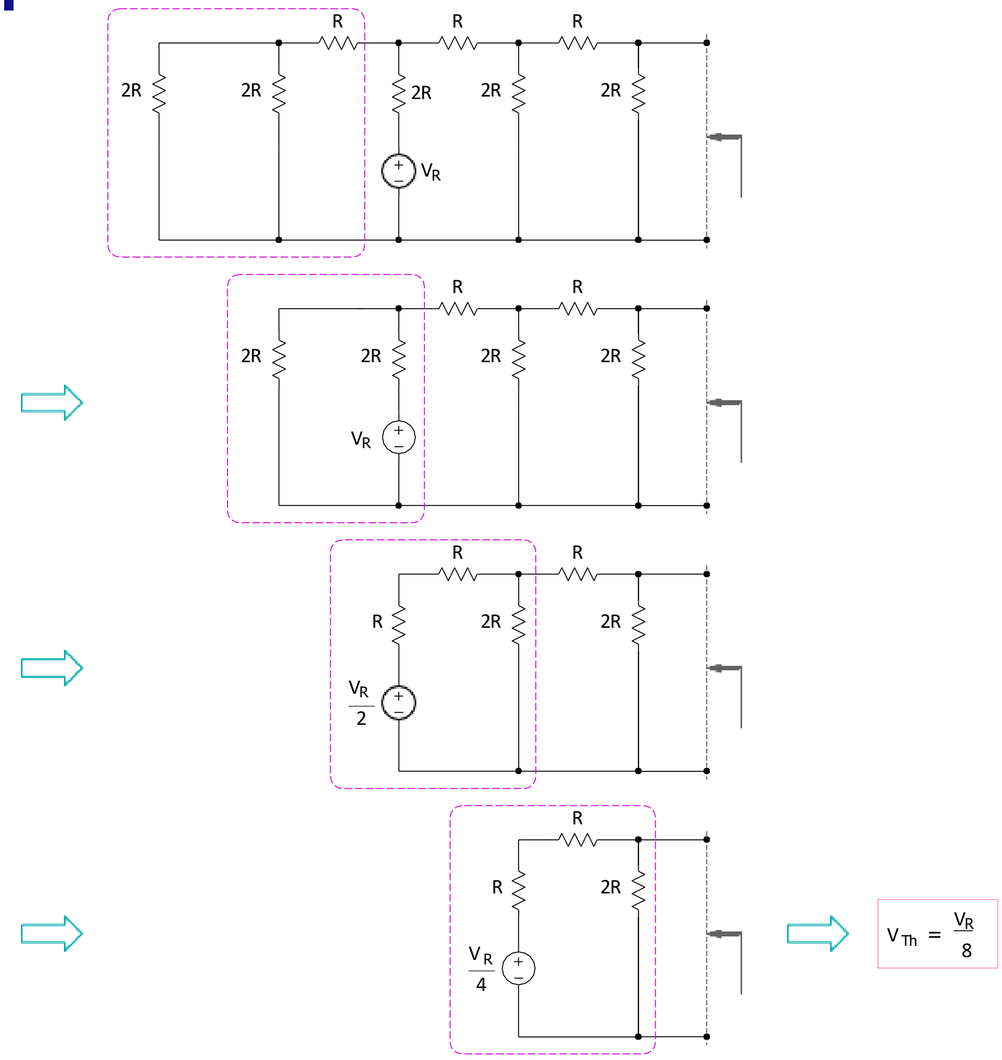


$$V_{Th} = \frac{V_R}{16}$$

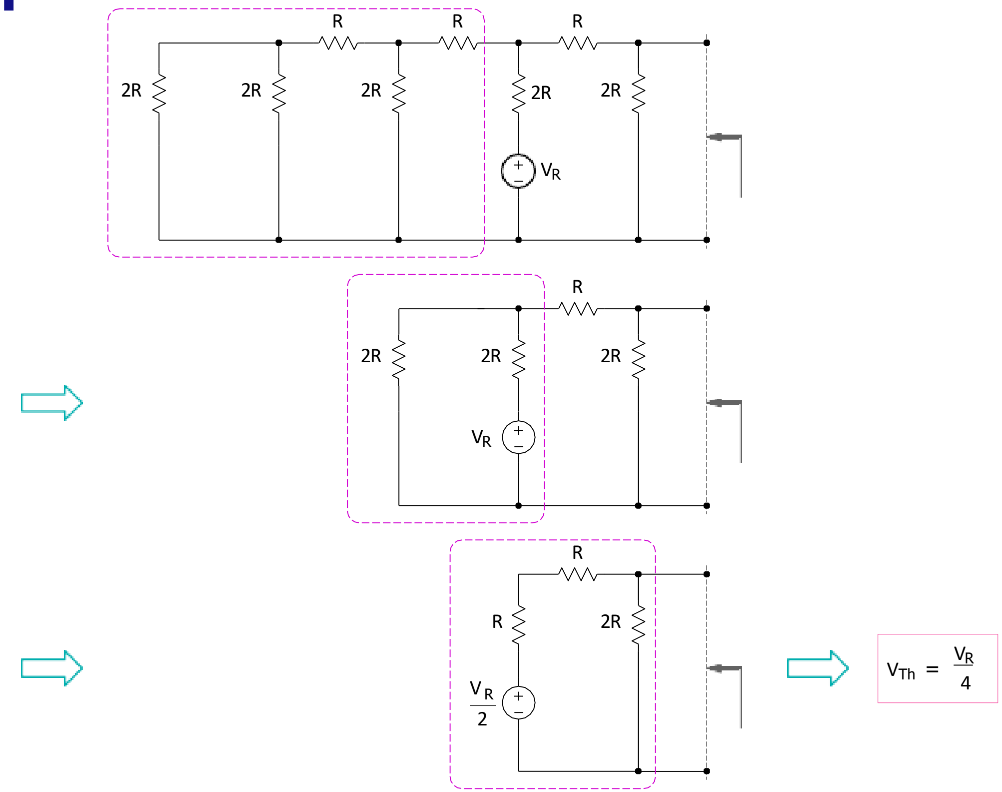
R-2R ladder network: V_{Th} for $S_1 = 1$



R-2R ladder network: V_{Th} for $S_1 = 1$

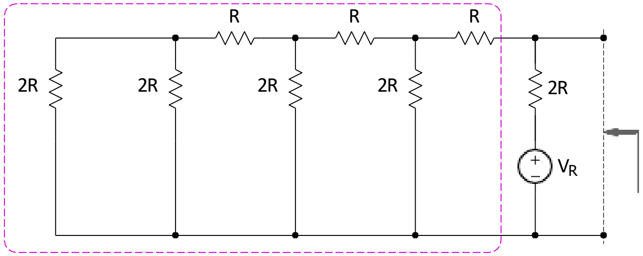


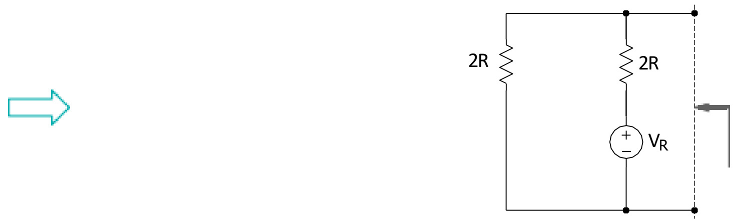
R-2R ladder network: V_{Th} for $S_2 = 1$



R-2R ladder network:

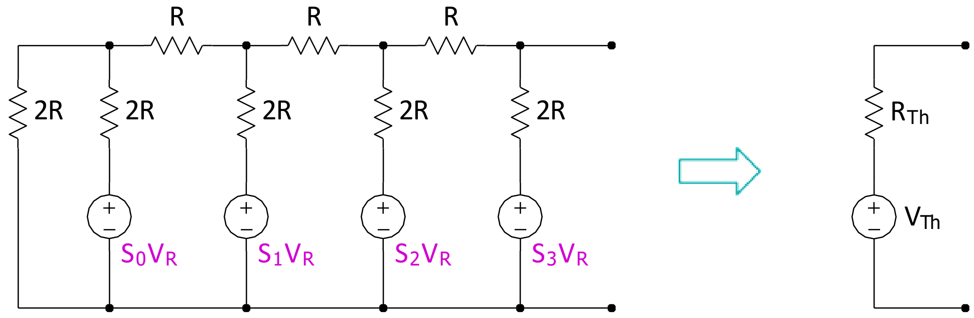
V_{Th} for $S_3 = 1$





$$V_{Th} = \frac{V_R}{2}$$

R-2R ladder network: R_{Th} and V_{Th}



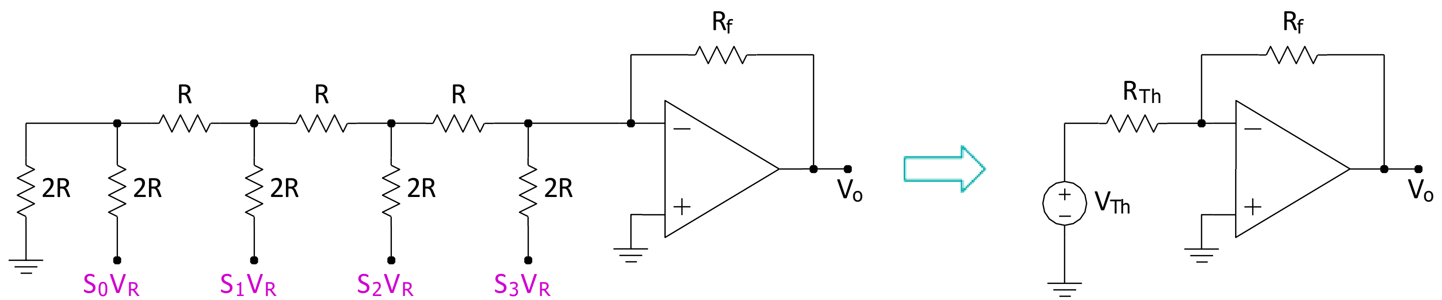
* $R_{Th} = R$.

* $V_{Th} = V_{Th}^{(S0)} + V_{Th}^{(S1)} + V_{Th}^{(S2)} + V_{Th}^{(S3)}$

$$= \frac{V_R}{16}\left[S_0\, 2^0 + S_1\, 2^1 + S_2\, 2^2 + S_3\, 2^3 \right] .$$

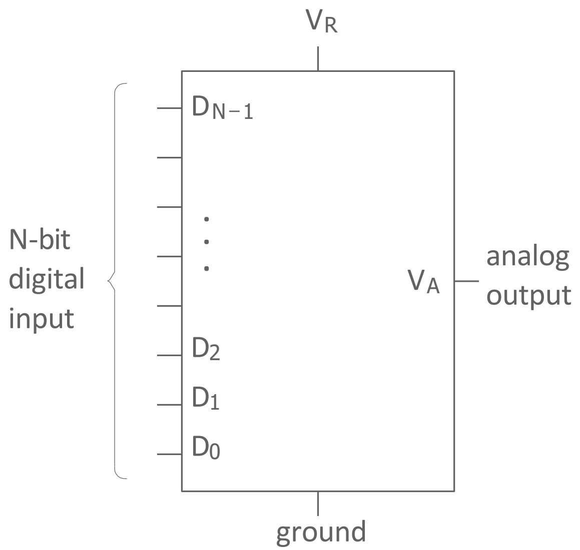
* We can use the *R*-2*R* ladder network and an op-amp to make up a DAC → next slide.

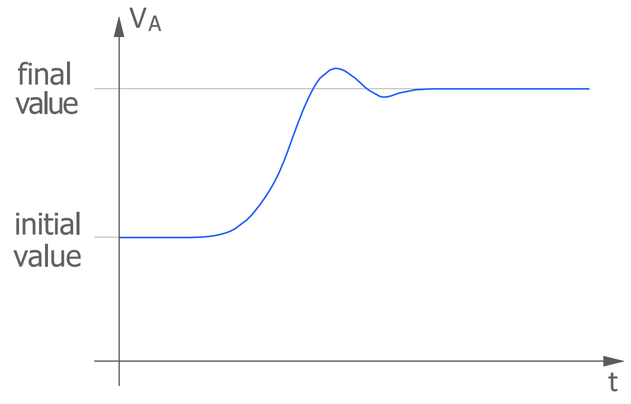
DAC with R-2R ladder



* $V_o = -\dfrac{R_f}{R_{Th}} V_{Th} = -\dfrac{R_f}{R_{Th}} \dfrac{V_R}{16} \left[S_0\, 2^0 + S_1\, 2^1 + S_2\, 2^2 + S_3\, 2^3 \right].$
* For an N-bit DAC, $V_o = -\dfrac{R_f}{R_{Th}} V_{Th} = -\dfrac{R_f}{R_{Th}} \dfrac{V_R}{2^N} \sum_{0}^{N-1} S_k\, 2^k .$
* 6- to 20-bit DACs based on the R-2R ladder network are commercially available in monolithic form (single chip).
* Bipolar, CMOS, or BiCMOS technology is used for these DACs.

DAC: settling time





* When there is a change in the input binary number, the output V_A takes a finite time to settle to the new value.
* The finite settling time arises because of stray capacitances and switching delays of the semiconductor devices used within the DAC chip.
* Example: 500 ns to 0.2 % of full scale.

شكراً لحسن

إصغائكم

THANK YOU ☺

END LESSON 12: DIGITAL-TO-ANALOG CONVERTER (DAC)