جامعة المستقبل

نحو جامعة مستدامة

Al-Mustaqbal University - College of engineering
Department of computer engineering

Second stage

Lecture Week 7

"Cascade counter, Counter decoding"

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Objectives Cascade counter

By the end of this lecture, students will be able to

- Understand the Structure and Operation,
  Describe the concept of cascading counters (connecting multiple counters in series).
  Explain how the output of one counter drives the clock input of the next.
- Differentiate Between Counter Types
  Compare cascade counters with synchronous and asynchronous counters.
- Apply Cascade Counters in Practical Circuits
  Analyze timing and propagation delay issues in cascade counters.
  Design multi-stage counters using cascading technique for applications like frequency division and digital clocks.

Objectives Counter decoding

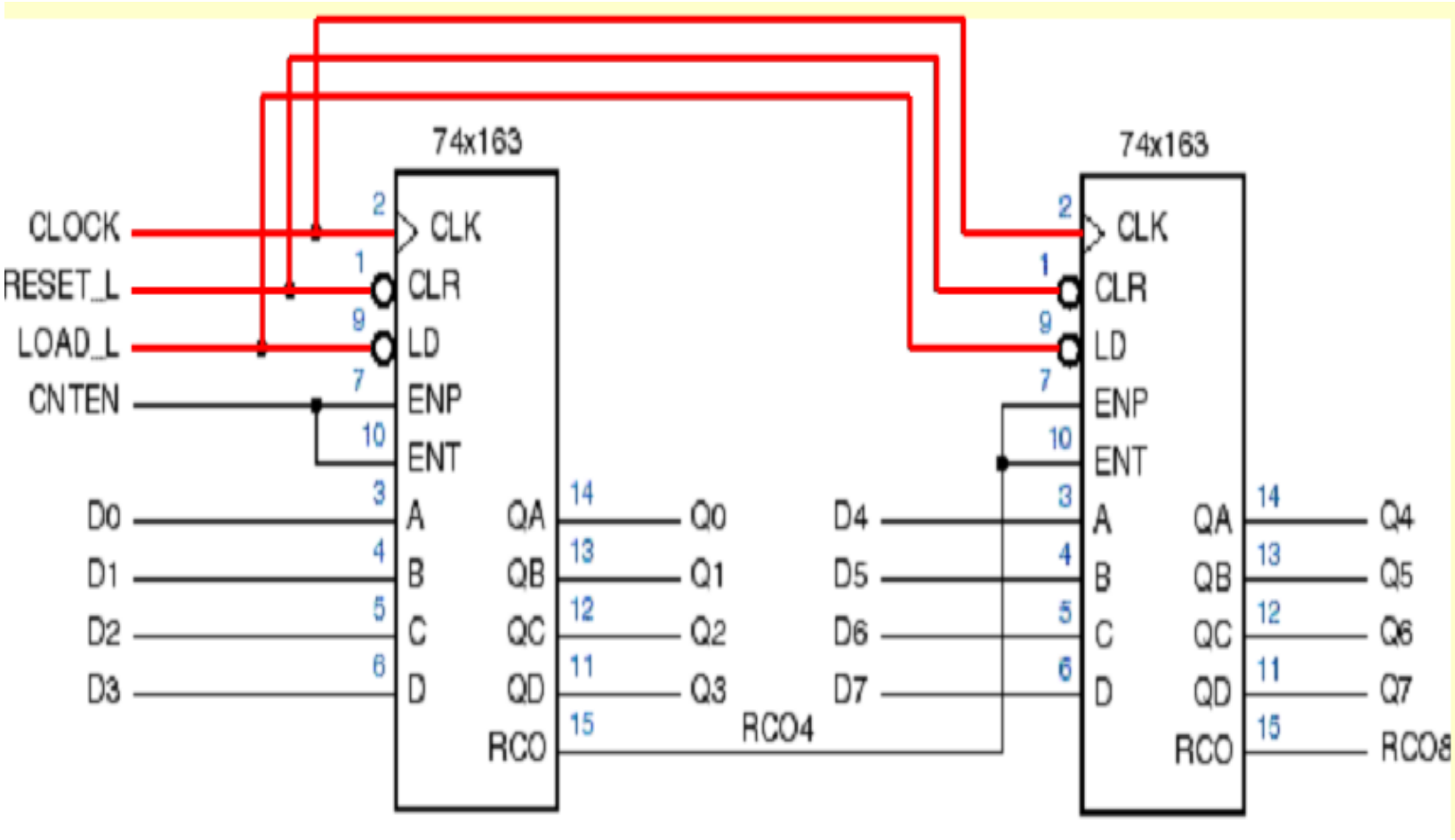
By the end of this lecture, students will be able to

- Understand the Purpose of Decoding:
  Explain the role of decoding in digital counters, particularly how it converts binary outputs into usable forms like decimal or display signals.
- Describe Decoding Techniques:
  Identify and describe common decoding methods used with counters (e.g., logic gates, 7-segment decoders, BCD to decimal decoders).
- Apply Decoding in Practical Circuits:
  Demonstrate how to design and implement counter-decoder combinations in applications such as digital clocks, frequency counters, or event counters.

Cascade counter

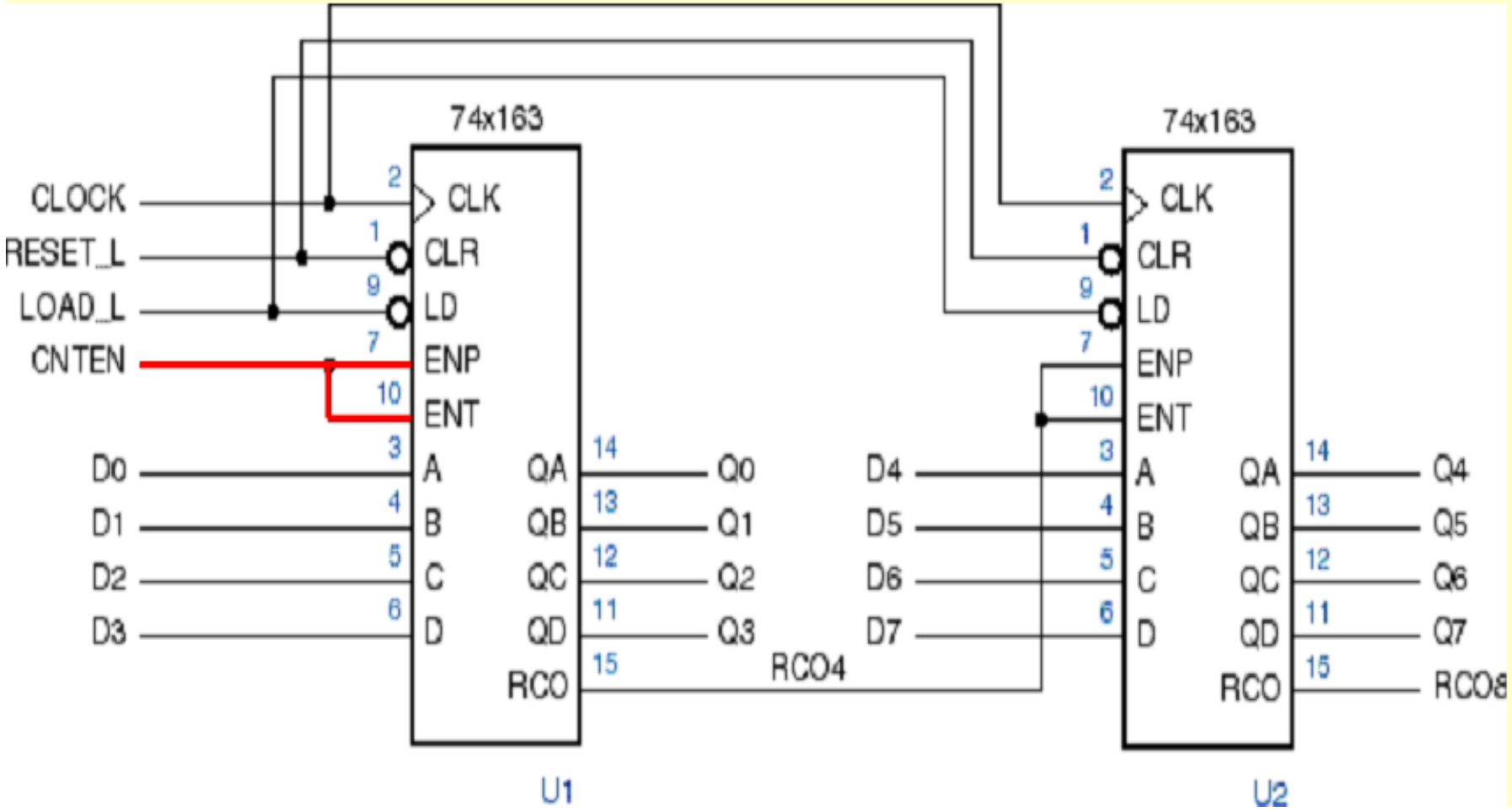
Cascade counter

CLOCK, RESET_L, and LOAD_L are connected in parallel.



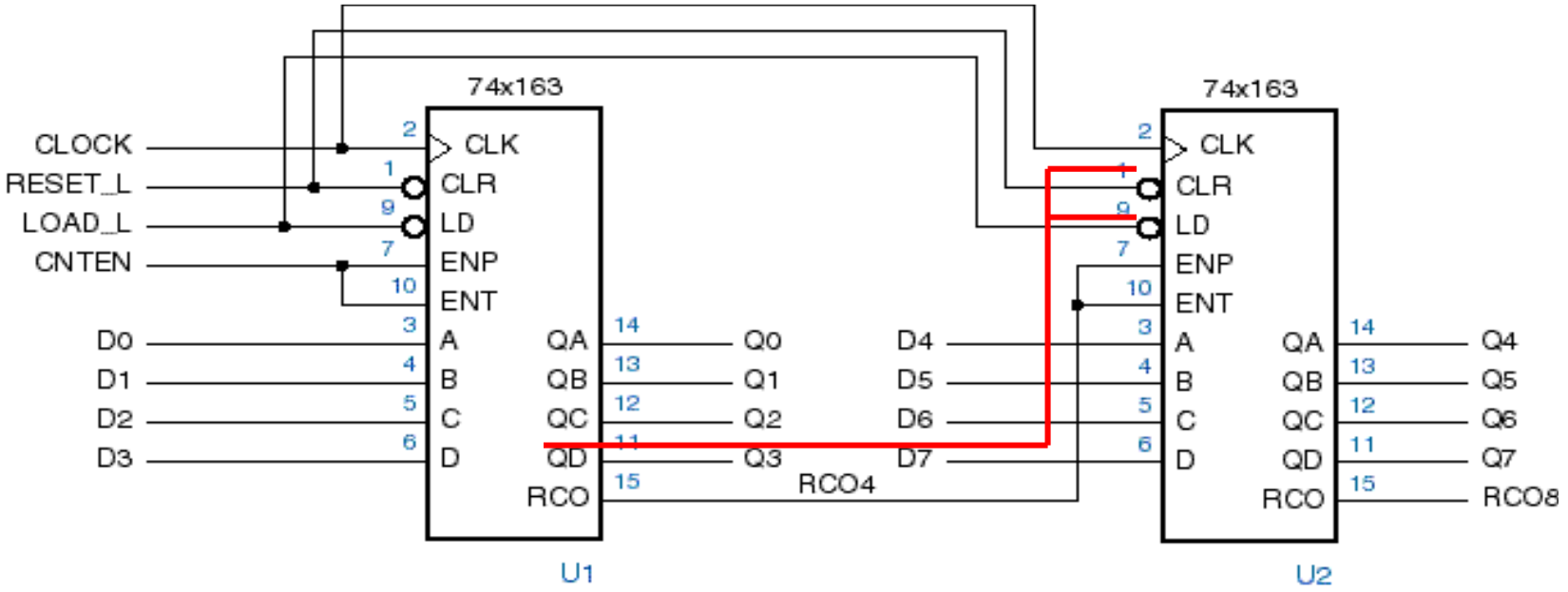
Cascade counter

A master count-enable (CNTEN) is connect to the low order 74x163.



Cascade counter

- The RC04 output is asserted if and only if the low-order ‘163 is in state15 and CNTEN is asserted.
- Cascading counters has the same ripple effect as a serial counter.
- The maximum counting speed is limited by the propagation delay.

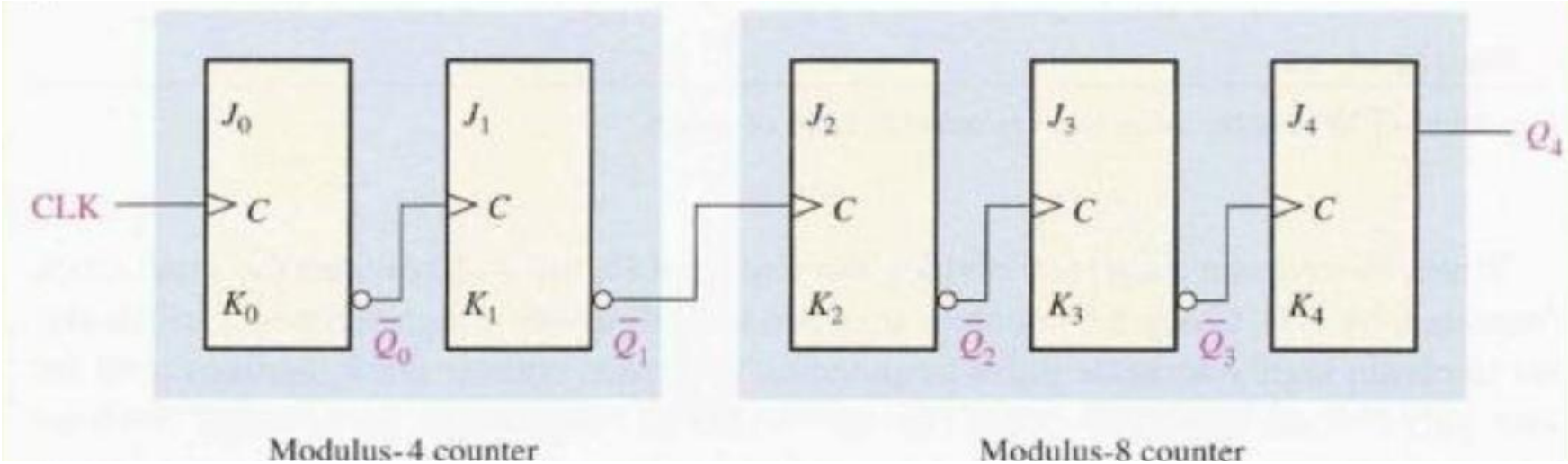


Cascade counter

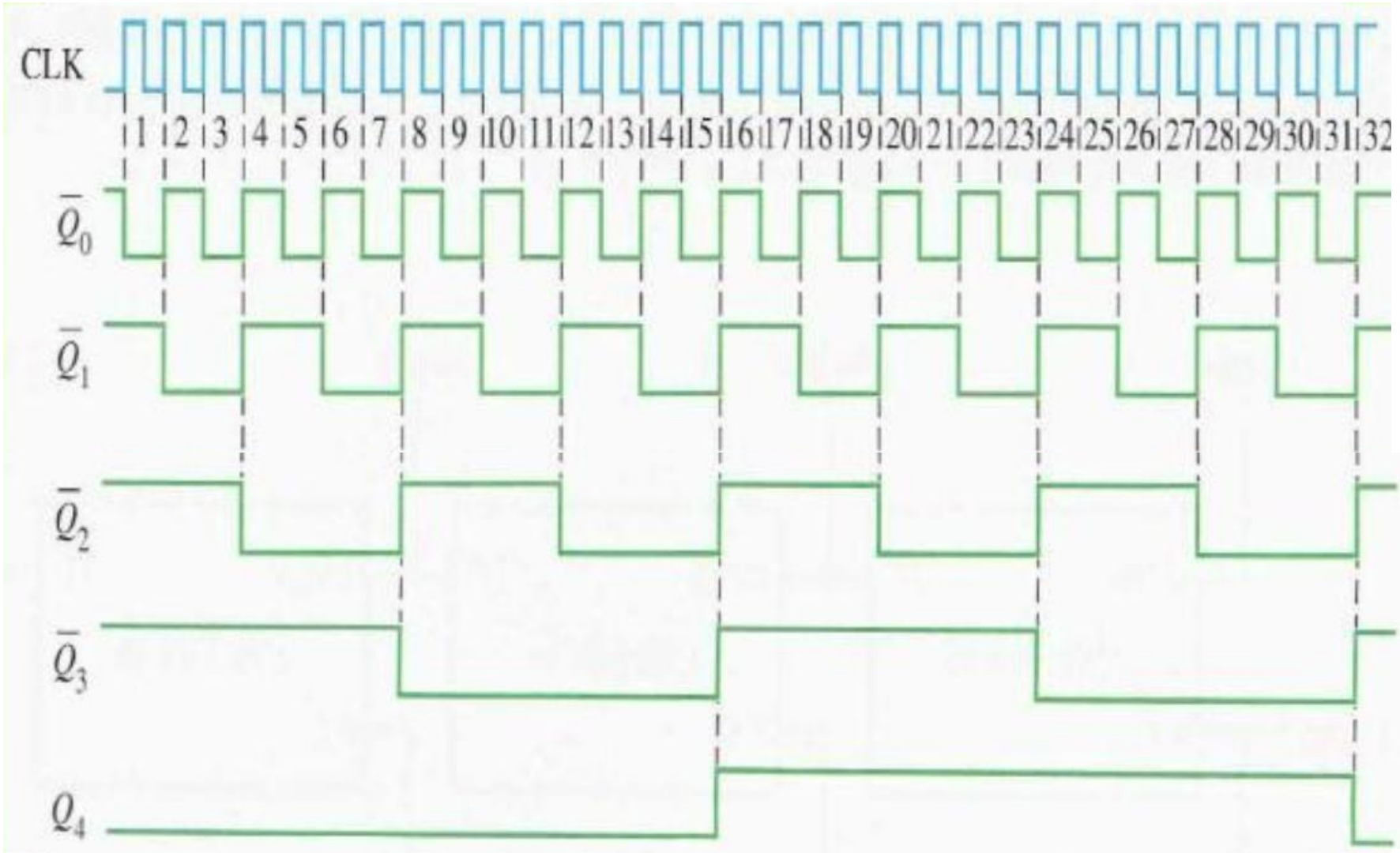
- Counters can be connected to achieve higher modulus operation.
- Cascading means that the last stage output of one counter drives the input of the next counter.
- A mod-M and a mod-N counter in cascade give a mod-MN counter.
- 2 types of cascading: Asynchronous cascading and synchronous cascading

Asynchronous cascading

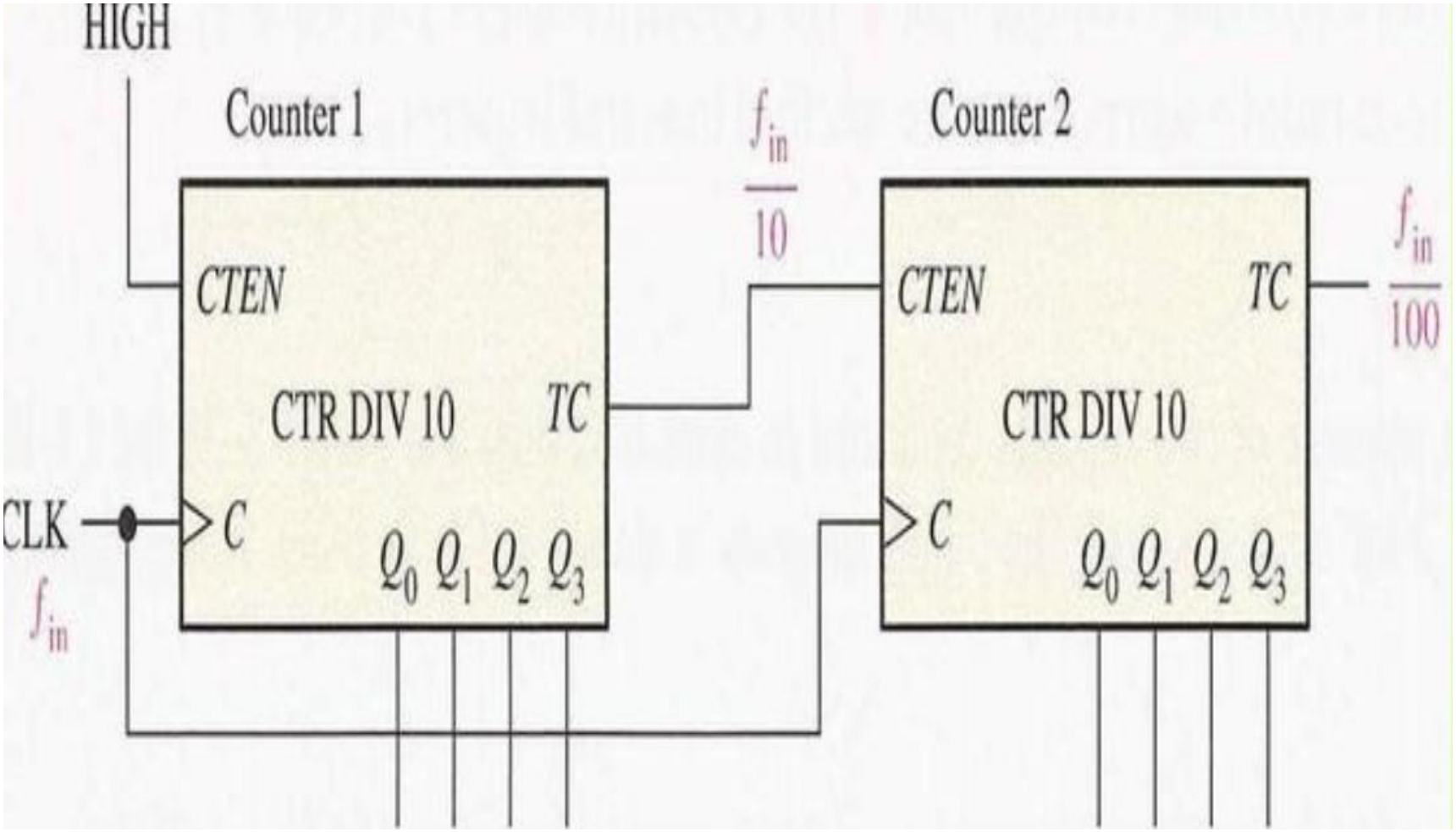
- Two asynchronous counters connected in cascade for a 2 bit and a 3 bit ripple counter.
- The overall modulus of the two cascaded counters is 4 x 8 = 32; that is they act as a divide-by- 32 counter.
- Figure below show two cascaded countes (all J and K inputs are HIGH)



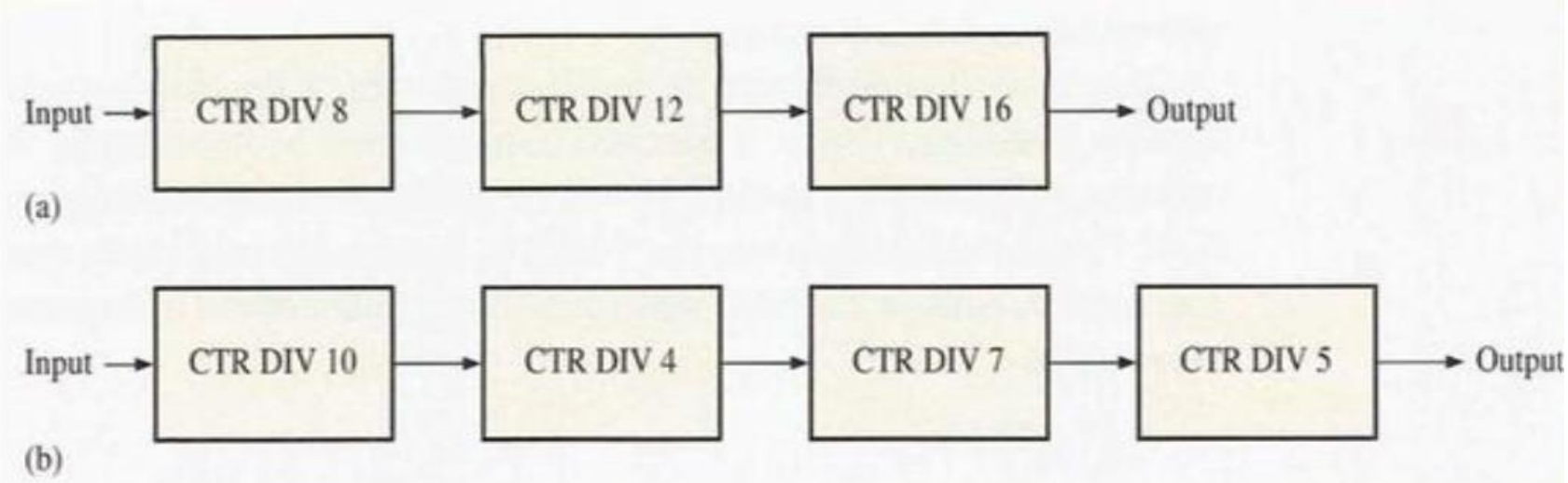
Asynchronous cascading –Timing



A modulus -100 counter using two cascaded decade counters



Determine the overall of the two cascaded counter configurations in figure belwo (a,b)



Solution:

- In figure (a) the overall modulus for 3-counter configuration is : 8 * 12 * 16 = 1536
- In figure (b) the overall modulus for 4-counter configuration is : 10* 4 * 7 *5= 1400

(3 mins) Individual activity

https://docs.google.com/forms/d/e/1FAIpQLSdD9Hm4xTdM7pT3bgXmhFjSS8IjajB3hdvmAq7f82AORfm67w/viewform?usp=header

A cascade of three identical modulo-5 counters has an overall modulus of_____.

Then Submit your answer using the QR code or the link above.

Counter decoding

Counter decoding

Counter decoding refers to the process of identifying specific output states of a counter by using logic gates. It is used to detect when a counter reaches a certain count value.

Purpose of Counter Decoding

- To detect a specific count (e.g., when the counter reaches 9 or 15).
- To create **non-binary sequences** or specific timing signals.
- To **reset** the counter at a certain value (e.g., for decade counters).
- To control other parts of a system based on the counter state.

How Counter Decoding Works:

- Counter Output: A counter (binary) produces outputs like Q0, Q1, Q2, Q3.
- Decoder Logic: Combinational logic (AND, OR, NOT) is used to detect specific output combinations.
- Action: The decoded output can trigger events like resetting the counter or enabling another circuit.

Example:

Detecting count 9 (1001) from a 4-bit binary counter:

- Inputs: Q3 Q2 Q1 Q0
- Desired output: High only when Q3=1, Q2=0, Q1=0, Q0=1
- Logic:

  Decode9= Q3 AND NOT(Q2) AND NOT(Q1) AND Q0

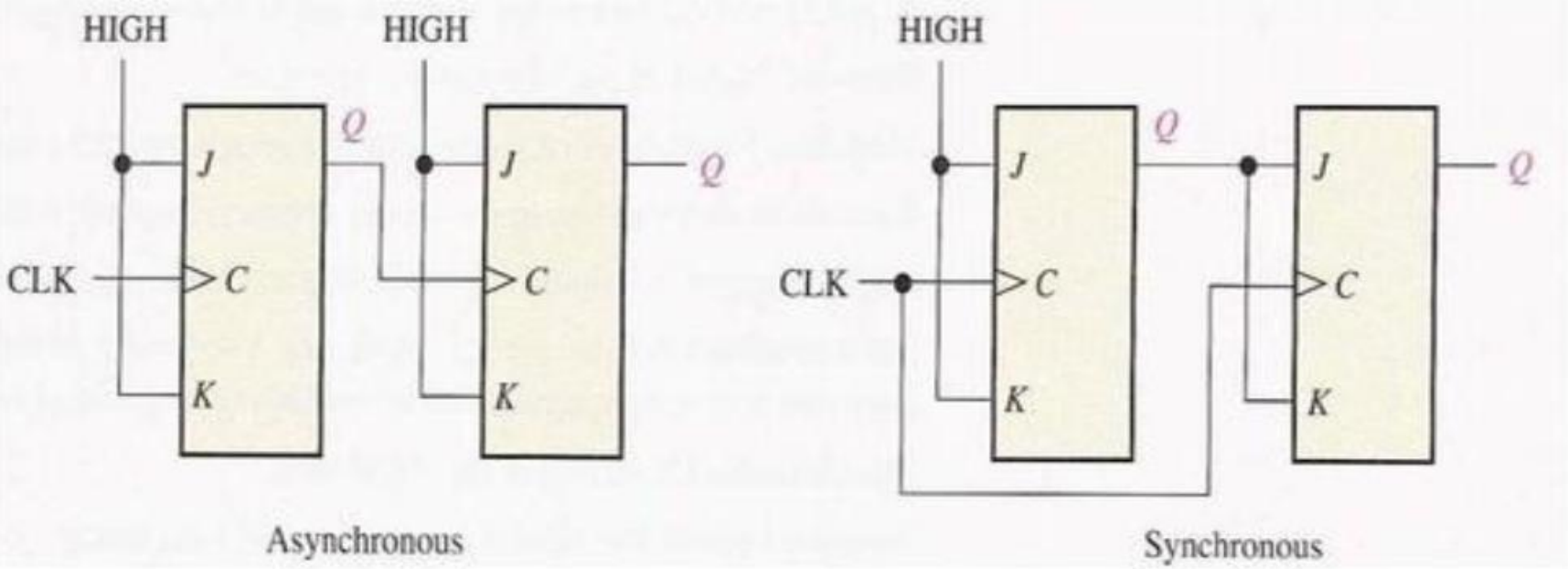
Applications of Counter Decoding

- Digital clocks
- Frequency division
- Sequence generation
- Event counting
- Finite State Machines (FSMs)

Type of Decoding	Description
Full decoding	Detects one specific state exactly
Partial decoding	Detects a group of states (e.g., ranges)

Summary Cascade counter

- Asynchronous and synchronous counters differ only in the way in which they are clocked.
- Asynchronous not occurring the same time because the stages do not all change together.
- Synchronous occurring at the same time



Summary Counter decoding

- Purpose:
  To detect specific counts in binary counters.
- Method:
  Uses logic gates (AND, OR, NOT) on counter outputs.
- Application:
  Decade counters, timers, digital clocks, control circuits.

THANK YOU ☺

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Department of Computer Engineering

END LESSON 7: CASCADE COUNTER, COUNTER DECODING