جامعة المستقبل

نحو جامعة مستدامة

Al-Mustaqbal University - College of engineering
Department of computer engineering

Second stage

Lecture Week 4

"Asynchronous counter"

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Objectives

By the end of this lecture, students will be able to

- Understand Operation of Ripple Counters: Learn how asynchronous (ripple) counters work, where each flip-flop is triggered by the previous one, not a common clock.
- Design and Analyze Counting Circuits.
- Explore Applications in Digital Systems: Understand the practical uses of asynchronous counters in devices such as digital clocks, frequency dividers, and event counters.

Digital Circuits - Counters

In this lecture, we will discuss various counters using T flip-flops. We know that T flip-flop toggles the output either for every positive edge of clock signal or for negative edge of clock signal.

An 'N' bit binary counter consists of 'N' T flip-flops.

- If the counter counts from 0 to $2^N - 1$, then it is called as binary **up counter**.
- Similarly, if the counter counts down from $2^N - 1$ to 0, then it is called as binary **down counter**.

There are two **types of counters** based on the flip-flops that are connected in synchronous or not.

1) Asynchronous counters **2) Synchronous counters**

Asynchronous Counters

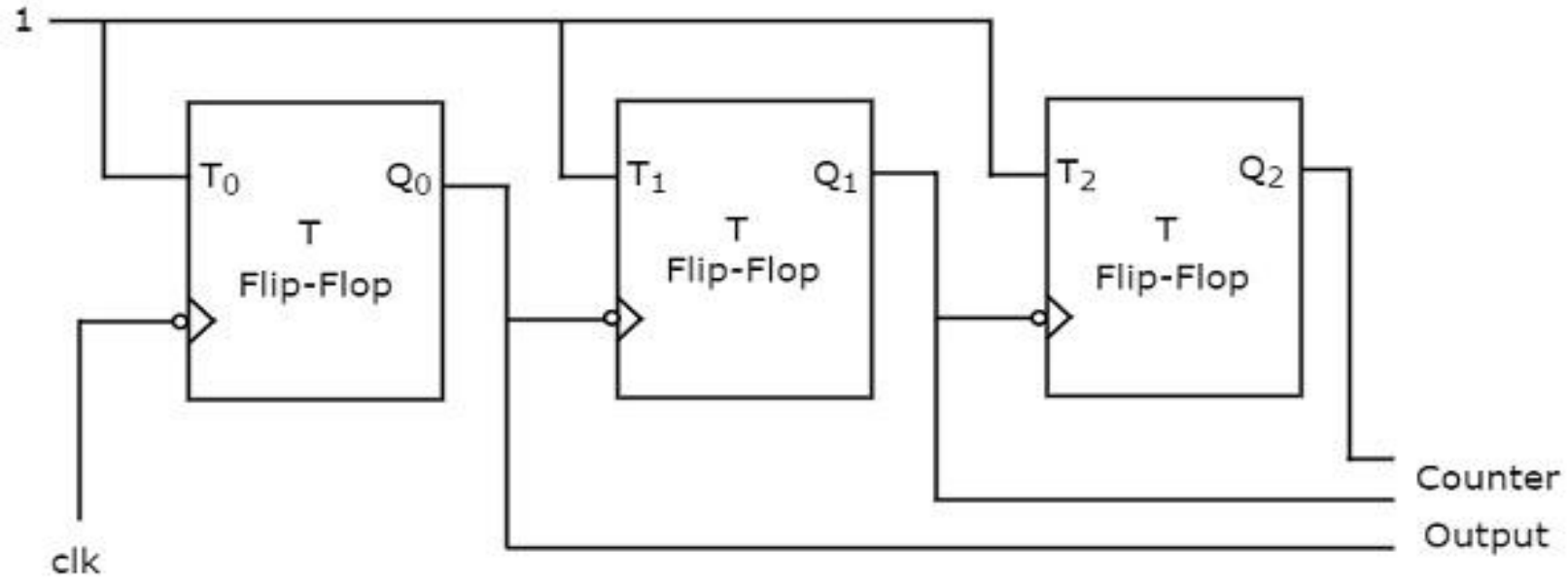
If the flip-flops do not receive the same clock signal, then that counter is called as **Asynchronous counter**. The output of system clock is applied as clock signal only to first flip-flop. The remaining flip-flops receive the clock signal from output of its previous stage flip-flop. Hence, the outputs of all flip-flops do not change affect at the same time.

Now, let us discuss the following two counters one by one.

1. **Asynchronous Binary up counter**
2. **Asynchronous Binary down counter**

Asynchronous Binary Up Counter

- An ‘N’ bit Asynchronous binary up counter consists of ‘N’ T flip-flops. It counts from 0 to $2^N - 1$.
- The **block diagram** of 3-bit Asynchronous binary up counter is shown in the following figure.



Asynchronous Binary Up Counter

- The 3-bit Asynchronous binary up counter contains three T flip-flops and the T-input of all the flip-flops are connected to ‘1’.
- All these flip-flops are negative edge triggered but the outputs change asynchronously.
- The clock signal is directly applied to the first T flip-flop.

So, the output of first T flip-flop **toggles** for every negative edge of clock signal.

Asynchronous Binary Up Counter

- The output of first T flip-flop is applied as clock signal for second T flip-flop.
- So, the output of second T flip-flop toggles for every negative edge of output of first T flip-flop.
- Similarly, the output of third T flip-flop toggles for every negative edge of output of second T flip-flop, since the output of second T flip-flop acts as the clock signal for third T flip-flop.

Asynchronous Binary Up Counter

Assume the initial status of T flip-flops from rightmost to leftmost is Q2Q1Q0=000. Here, Q2 & Q0 are MSB & LSB respectively. We can understand the **working** of 3-bit asynchronous binary counter from the following table.

No of negative edge of Clock	Q_0LSB	Q_1	Q_2MSB
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

Asynchronous Binary Up Counter

- Q0 toggled for every negative edge of clock signal.
- Q1 toggled for every Q0 that goes from 1 to 0, otherwise remained in the previous state.
- Similarly, Q2 toggled for every Q1 that goes from 1 to 0, otherwise remained in the previous state.

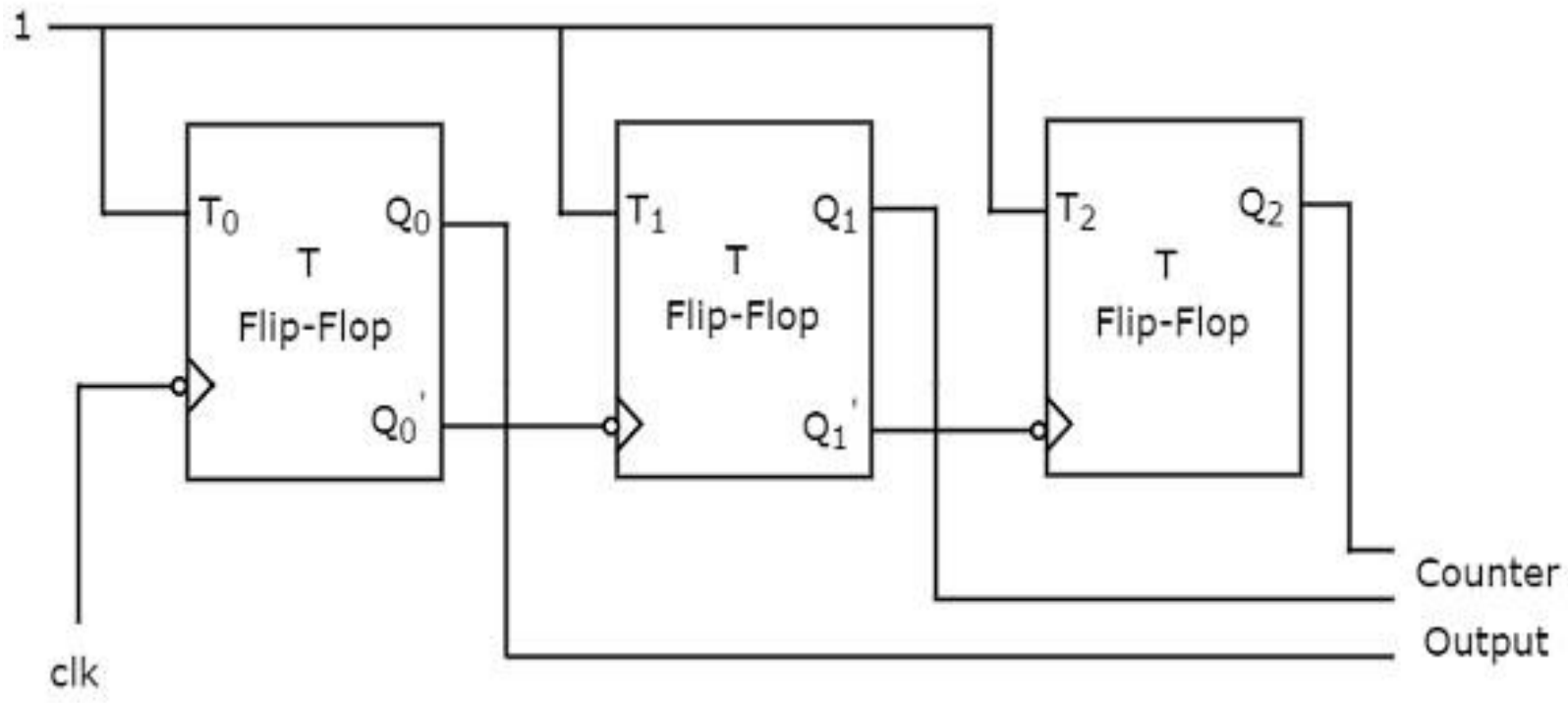
The initial status of the T flip-flops in the absence of clock signal is Q2Q1Q0=000.

This is incremented by one for every negative edge of clock signal and reached to maximum value at 7th negative edge of clock signal.

This pattern repeats when further negative edges of clock signal are applied.

Asynchronous Binary Down Counter

An 'N' bit Asynchronous binary down counter consists of 'N' T flip-flops. It counts from $2N - 1$ to 0. The block diagram of 3-bit Asynchronous binary down counter is shown in the following figure.



Asynchronous Binary Down Counter

The block diagram of 3-bit Asynchronous binary down counter is similar to the block diagram of 3-bit Asynchronous binary up counter.

But, the only difference is that instead of connecting the normal outputs of one stage flip-flop as clock signal for next stage flip-flop, connect the complemented outputs of one stage flip-flop as clock signal for next stage flip-flop.

Complemented output goes from 1 to 0 is same as the normal output goes from 0 to 1.

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Asynchronous Binary Down Counter

Assume the initial status of T flip-flops from rightmost to leftmost is Q2Q1Q0=000. Here, Q2 & Q0 are MSB & LSB respectively. We can understand the **working** of 3-bit asynchronous binary down counter from the following table.

No of negative edge of Clock	Q_0LSB	Q_1	Q_2MSB
0	0	0	0
1	1	1	1
2	0	1	1
3	1	0	1
4	0	0	1
5	1	1	0
6	0	1	0
7	1	0	0

Asynchronous Binary Down Counter

- Q0 toggled for every negative edge of clock signal.
- Q1 toggled for every Q0 that goes from 0 to 1, otherwise remained in the previous state.
- Similarly, Q2 toggled for every Q1 that goes from 0 to 1, otherwise remained in the previous state.

Asynchronous Binary Down Counter

- The initial status of the T flip-flops in the absence of clock signal is Q2Q1Q0=000.
- This is decremented by one for every negative edge of clock signal and reaches to the same value at 8th negative edge of clock signal.
- This pattern repeats when further negative edges of clock signal are applied.

(5 mins) Group Activity

https://docs.google.com/forms/d/e/1FAIpQLSckGaWVNYeZH3hXssqAqIkN3WdU3BsyJ90H2nNZhijk-D3oOA/viewform?usp=header

Try thinking about what are the Applications of Asynchronous Binary Counter!

Then Submit your answer using the QR code or the link above.

Summary

- Definition:
  An asynchronous counter (also called a ripple counter) is a sequential circuit in which flip-flops are triggered one after another, not simultaneously. The output of one flip-flop acts as the clock input for the next.
- Operation:
  The first flip-flop is triggered by the external clock.Each subsequent flip-flop toggles when the previous one changes from high to low (falling edge).This causes a delay (rippling effect), making it slower than synchronous counters.
- Applications:
  Digital clocks , Frequency dividers, Simple timers and event counters

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إصغائكم

THANK YOU ☺

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Department of Computer Engineering

END LESSON 4: ASYNCHRONOUS COUNTER