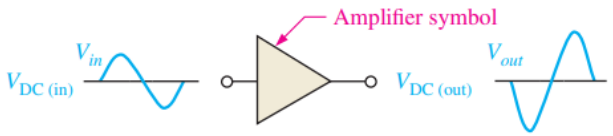
The DC Operaing Point

A transistor must be properly biased with a dc voltage in order to operate as a linear amplifier. A dc operating point must be set so that signal variations at the input terminal are amplified and accurately reproduced at the output terminal. The dc operating point is often referred to as the Q-point (quiescent point).

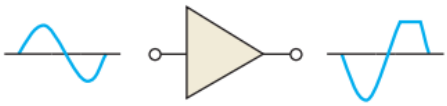
Bias establishes the dc operating point (Q-point) for proper linear operation of an amplifier. If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied. Figures shows the effects of proper and improper dc biasing of an inverting amplifier.

- In part (a), the output signal is an amplified replica of the input signal except that it is inverted, which means that it is 180° out of phase with the input. The output signal swings equally above and below the dc bias level of the output, VDC(out).



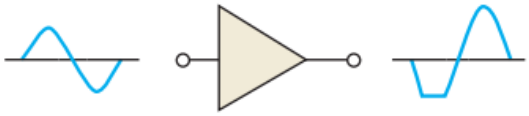
(a) Linear operation: larger output has same shape as input except that it is inverted

- Improper biasing can cause distortion in the output signal, as illustrated in parts (b) and (c). Part (b) illustrates limiting of the positive portion of the output voltage as a result of a Q-point (dc operating point) being too close to cutoff.



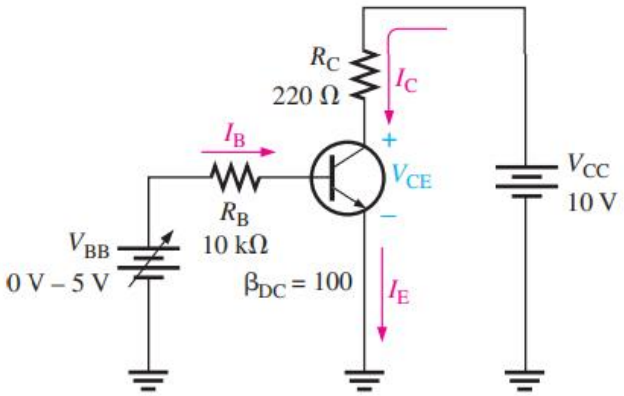
(b) Nonlinear operation: output voltage limited (clipped) by cutoff

- Part (c) shows limiting of the negative portion of the output voltage as a result of a dc operating point being too close to saturation.

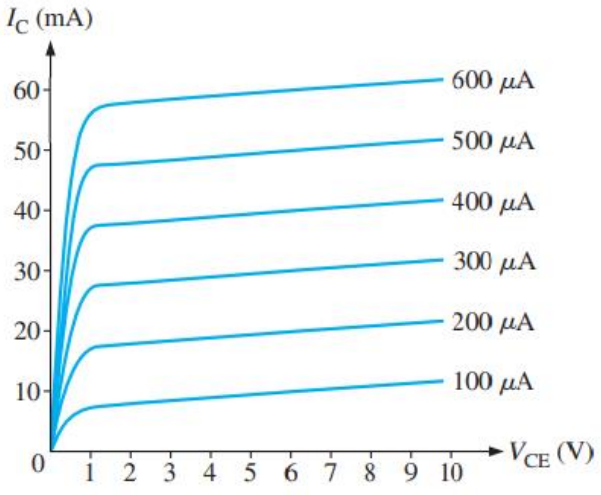


(c) Nonlinear operation: output voltage limited (clipped) by saturation

Graphical Analysis The transistor in Figure 5–2(a) is biased with V_{CC} and V_{BB} to obtain certain values of I_B, I_C, I_E, and V_{CE}. The collector characteristic curves for this particular transistor are shown in Figure 5–2(b); we will use these curves to graphically illustrate the effects of dc bias.



(a) DC biased circuit



(b) Collector characteristic curves

In Figure 5–3, we assign three values to I_B and observe what happens to I_C and V_{CE}. First, V_{BB} is adjusted to produce an I_B of 200 μA, as shown in Figure 5–3(a). Since $I_C = \beta_{DC} I_B$, the collector current is 20 mA, as indicated, and

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (20\text{ mA})(220\ \Omega) = 10\text{ V} - 4.4\text{ V} = 5.6\text{ V}$$

This Q-point is shown on the graph of Figure 5–3(a) as Q_1.

Next, as shown in Figure 5–3(b), V_{BB} is increased to produce an I_B of 300 μA and an I_C of 30 mA.

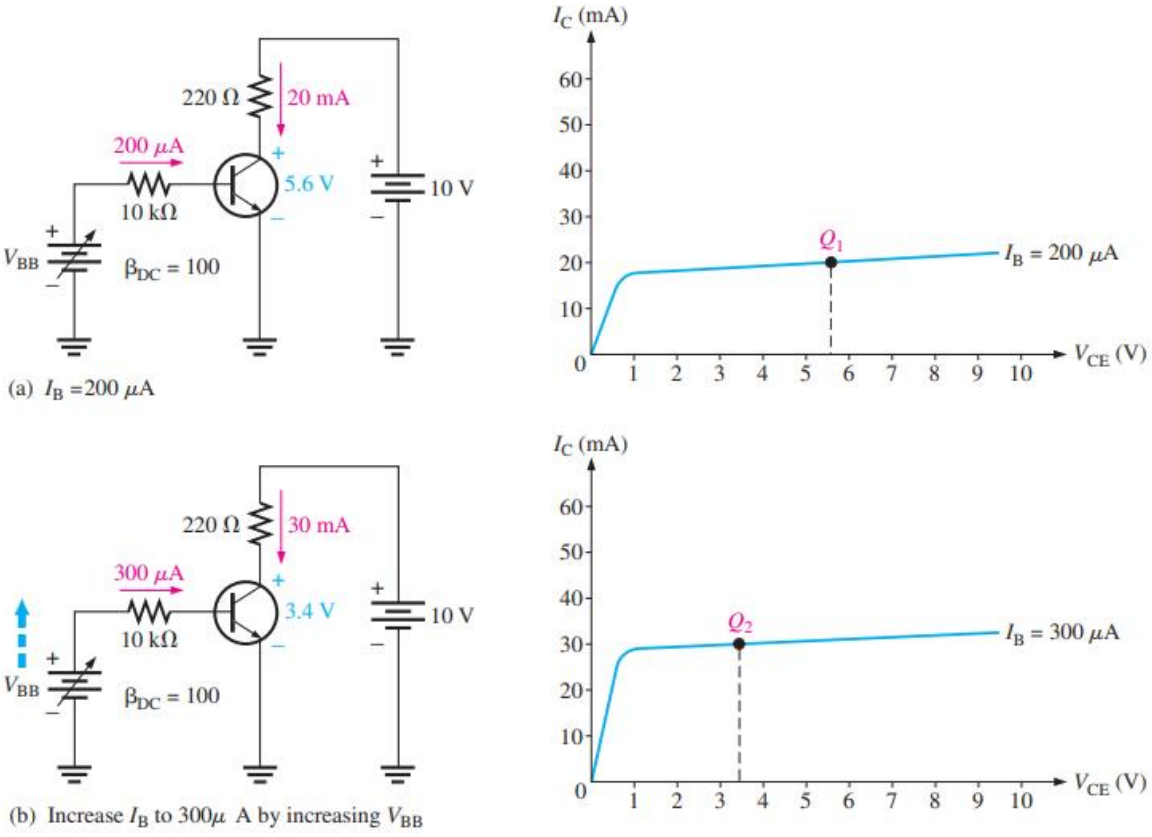
$$V_{CE} = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 10\text{ V} - 6.6\text{ V} = 3.4\text{ V}$$

The Q-point for this condition is indicated by Q_2 on the graph.

Finally, as in Figure 5–3(c), V_{BB} is increased to give an I_B of 400 μA and an I_C of 40 mA.

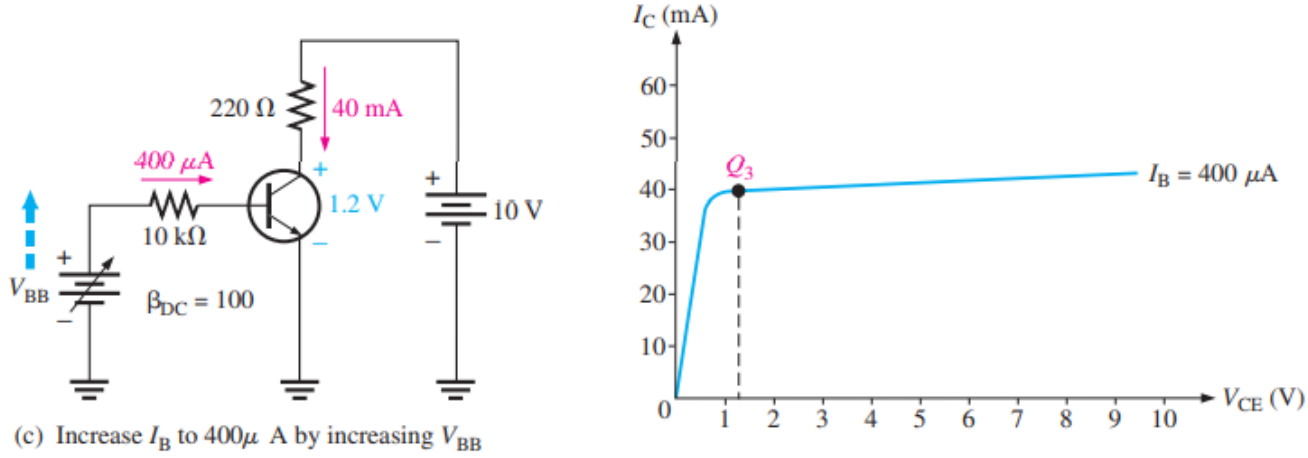
$$V_{CE} = 10\text{ V} - (40\text{ mA})(220\ \Omega) = 10\text{ V} - 8.8\text{ V} = 1.2\text{ V}$$

Q_3 is the corresponding Q-point on the graph.



(a) I_B =200 μA

(b) Increase I_B to 300μ A by increasing V_{BB}

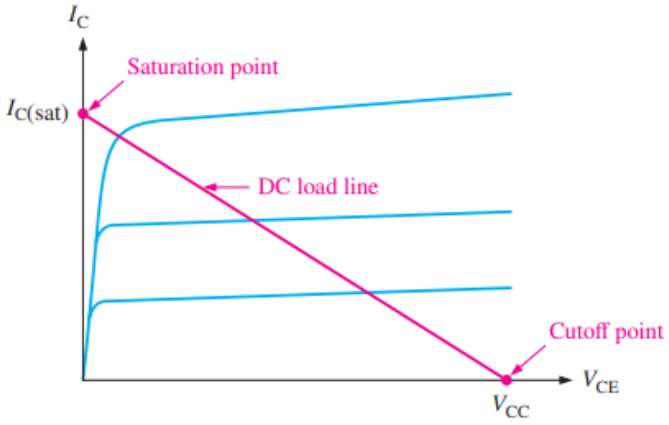


(c) Increase I_B to 400μ A by increasing V_{BB}

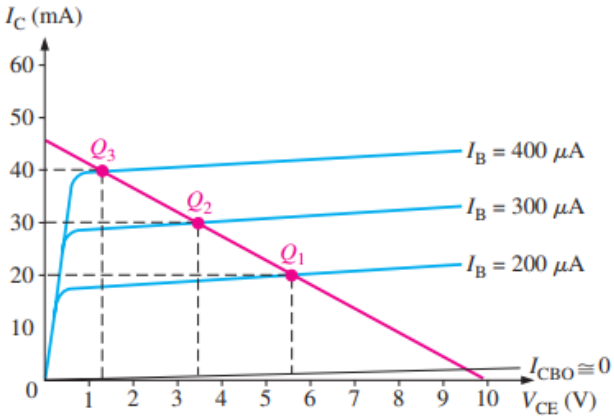
▲ FIGURE 5–3

Illustration of Q-point adjustment.

Linear Operation The region along the load line including all points between saturation and cutoff is generally known as the **linear region** of the transistor's operation. As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input.



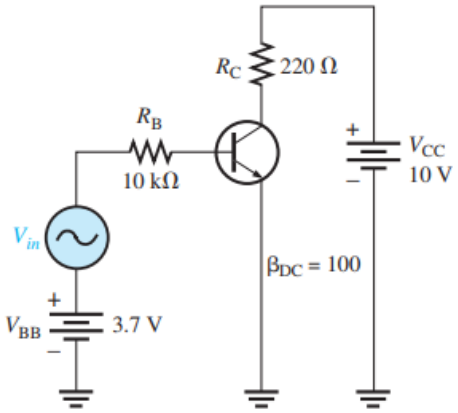
(a)

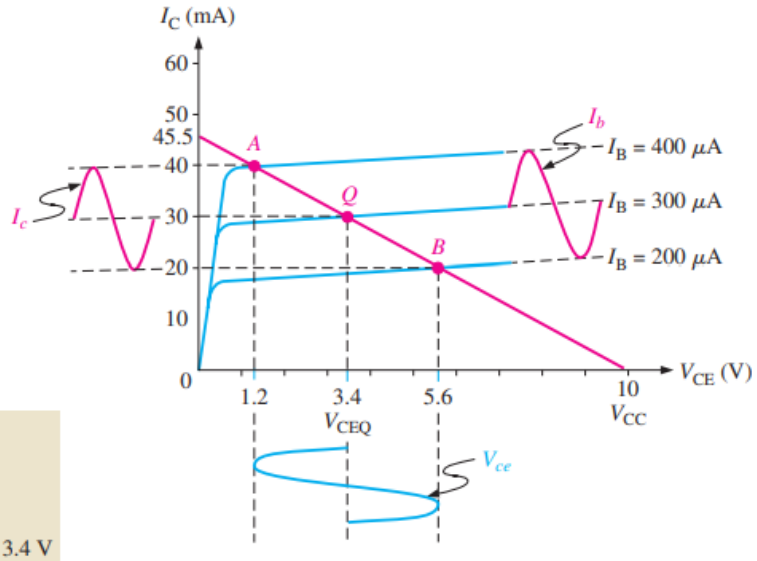


(b)

▲ FIGURE 5–4

The dc load line.





$$I_{BQ} = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{3.7\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 300\ \mu\text{A}$$

$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\ \mu\text{A}) = 30\text{ mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 3.4\text{ V}$$

▲ **FIGURE 5–5**

Variations in collector current and collector-to-emitter voltage as a result of a variation in base current.

EXAMPLE 5–1

Determine the Q-point for the circuit in Figure 5–7 and draw the dc load line. Find the maximum peak value of base current for linear operation. Assume $\beta_{DC} = 200$.

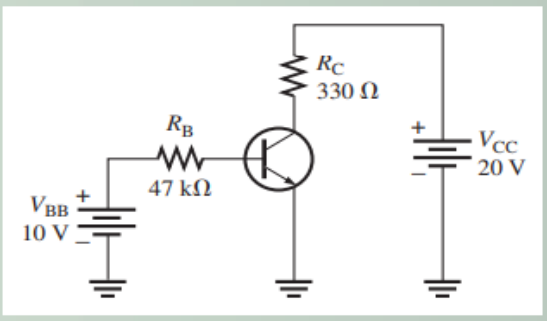
Solution The Q-point is defined by the values of I_C and V_{CE}.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{47\text{ k}\Omega} = 198\ \mu\text{A}$$

$$I_C = \beta_{DC} I_B = (200)(198\ \mu\text{A}) = \mathbf{39.6\text{ mA}}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - 13.07\text{ V} = \mathbf{6.93\text{ V}}$$

▶ **FIGURE 5–7**



The Q-point is at $I_C = 39.6$ mA and at $V_{CE} = 6.93$ V.

Since $I_{C(cutoff)} = 0$, you need to know $I_{C(sat)}$ to determine how much variation in collector current can occur and still maintain linear operation of the transistor.

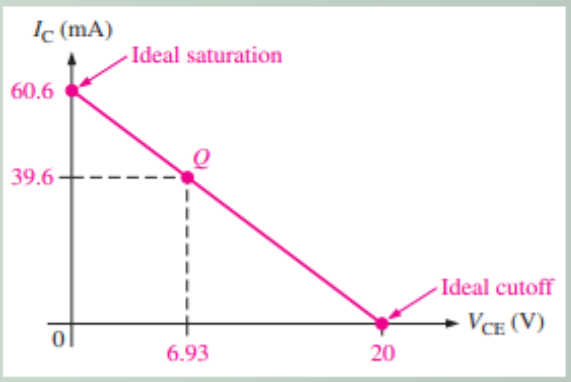
$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20\text{ V}}{330\ \Omega} = 60.6\text{ mA}$$

The dc load line is graphically illustrated in Figure 5–8, showing that before saturation is reached, I_C can increase an amount ideally equal to

$$I_{C(sat)} - I_{CQ} = 60.6\text{ mA} - 39.6\text{ mA} = 21.0\text{ mA}$$

However, I_C can decrease by 39.6 mA before cutoff ($I_C = 0$) is reached. Therefore, the limiting excursion is 21 mA because the *Q-point is closer to saturation than to cutoff.* The 21 mA is the maximum peak variation of the collector current. Actually, it would be slightly less in practice because $V_{CE(sat)}$ is not quite zero.

▶ FIGURE 5–8



Determine the maximum peak variation of the base current as follows:

$$I_{b(peak)} = \frac{I_{c(peak)}}{\beta_{DC}} = \frac{21\text{ mA}}{200} = \mathbf{105\ \mu A}$$

Homework

Find the Q-point for the circuit in Figure 5–7, and determine the maximum peak value of base current for linear operation for the following circuit values: β_{DC} = 100, R_C =1.0 kΩ, and VCC = 24 V.