Real Time System

Third Level

8255A Programmable Peripheral Interface PPI

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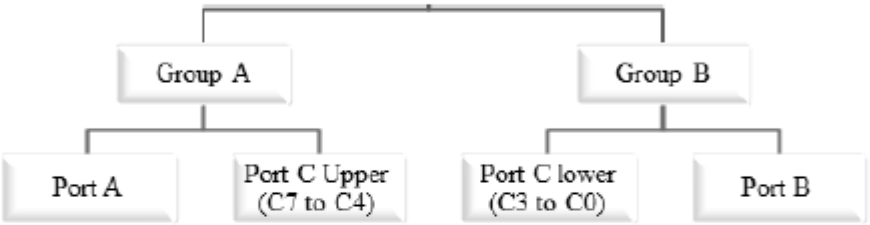
Goals
Up-on completing this lecture, the student should be able to:

1- Understand the internal archi. of 8255A PPI
2- Use 8255A in RT designs.

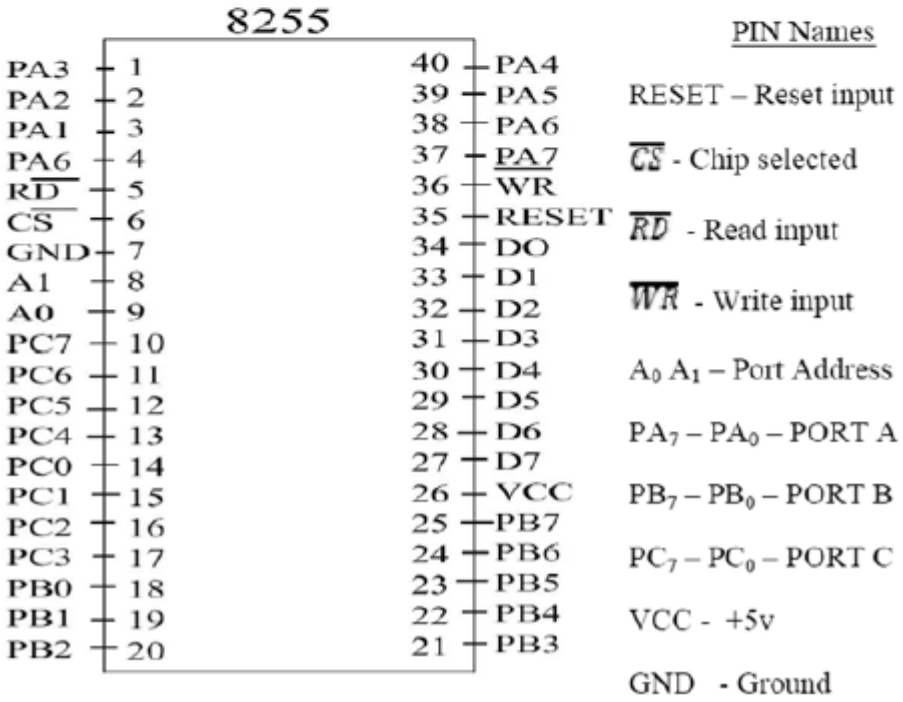
8255A PPI:

The 8255A is a general purpose programmable I/O device designed for use with microprocessors. It can be programmed to transfer data under various conditions. It consists of three 8-bit bidirectional I/O ports (24 I/O lines) that can be configured to meet different system I/O needs.

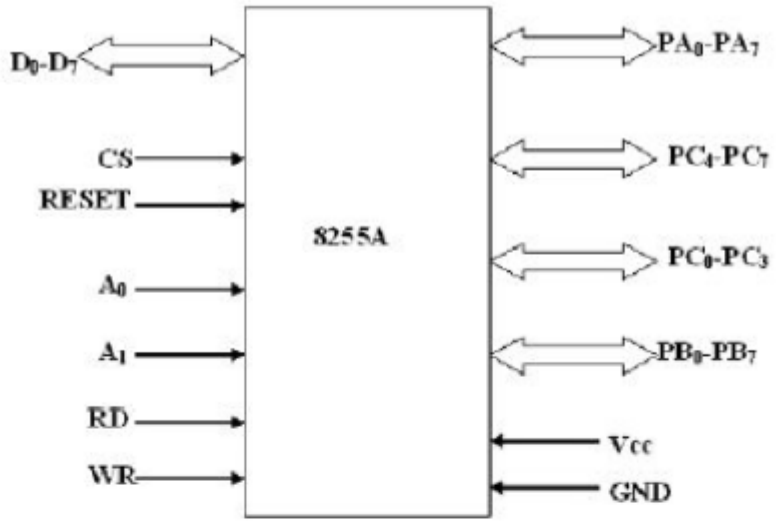
The 8255A contains three 8-bit ports (A, B and C). These ports are used to control the external devices and it can be configured as I/O ports. The 8 bits of port C can be used as individual bits or be grouped in two 4-bit ports: C upper (CU) and C $_{lower}$ (C_L). The three ports are divided in two groups Group A (Port A and upper Port C) Group B (Port B and lower Port C).



The 8255 is contained in a 40-pin, whose pin out is shown below:



Signals of 8255A:-

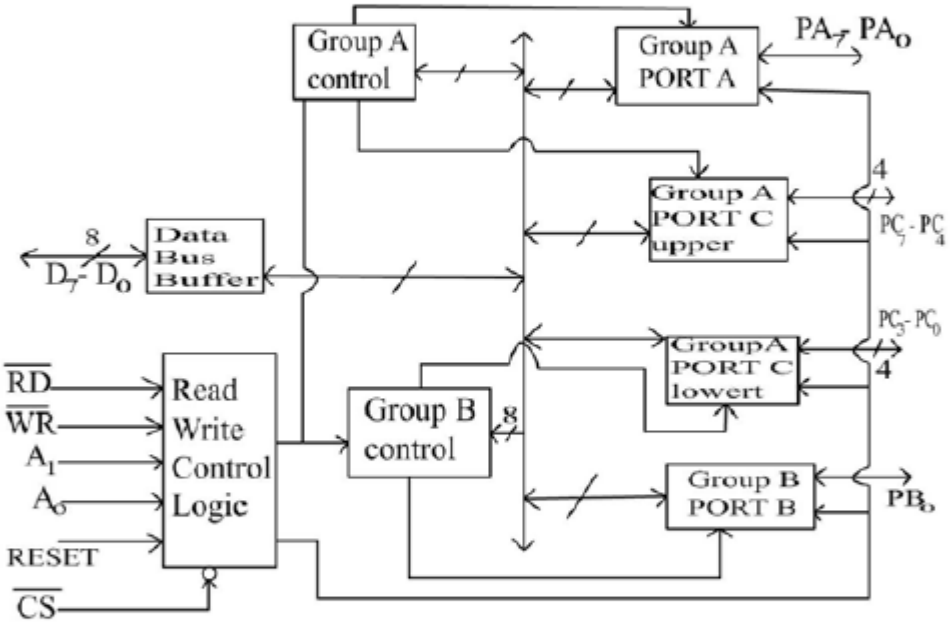


Function of Pins:

- **Data bus (D_0-D_7):** These are 8-bit bi-directional buses, connected to µP data bus for transferring data.
- **VCC and GND:** +5V power supply and 0V.
- **(CS) Chip Select:** A "low' on this input pin enables the communication between the 8255A, and the CPU.
- **(RD) Read:** A "low" on this Input pin enables the 8255A to send the data or status information to the CPU, it allows the CPU to "read from the 8255A.
- **(WR) Write:** A. " low" on the input pin enables the CPU to write data or control words into the 8255A.
- **RESET:** This is used to reset the device. That means clear control registers and all the ports are set to the input mode.
- **PA_0-PA_7**: It is the 8-bit bi-directional I/O pins used to send the data to peripheral or to receive the data from peripheral.
- **PB_0-PB_7**: Similar to PA
- **PC_0-PC_7**: This is also 8-bit bidirectional I/O pins. These lines are divided into two groups: PC_0 to PC_3 (Lower Groups), PC_4 to PC_7 (Higher groups), these two groups working in separately use 4 data's.
- **(A0 and A1):** The selection of input port and control word register is done by using A0 and A1.

CS	A_1	A_0	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	8255 is not selected

The block diagram is shown below:



It has 4 groups:-

1. Data bus buffer.
2. Read Write control logic.
3. Group A and Group B controls.
4. Port A, B and C.

- **Data bus buffer:** It is an 8-bit bidirectional used to interface the internal data bus of 8255 to the system data bus by reading and writing operations. The direction of data buffer is decided by Read Write Control Logic.

- **Read Write control logic:** This is getting the input signals from control bus and Address bus:

  Control signal are RD and WR.

  Address signals are A0, A1, and CS.

  8255 operation is enabled or disabled by CS.
- **Group A and Group B controls:** Group A and B get the Control Signal from CPU and send the command to the individual control blocks.

  Group A send the control signal to port A and Port C (Upper) PC_7-PC_4.

  Group B send the control signal to port B and Port C (Lower) PC_3-PC_0.
- **Port A, B and C:** The 8255A contains three 8-bit ports (A, B and C).

  Port A: This has an 8 bit latched/buffered O/P and 8 bit input latch. It can be programmed in 3 modes – mode 0, mode 1 & mode 2.

  Port B: This has an 8 bit latched / buffered O/P and 8 bit input latch. It can be programmed in mode 0 & mode1.

  Port C: This has an 8 bit latched input buffer and 8 bit output latched/buffer. This port can be divided into two 4 bit ports and can be used as control signals for port A and port B. It can be programmed by bit set/reset operation.

Control word:-

- The contents of the control register called the control word specify an I/O function for each port.
- This register can be accessed to write a control word when A0 & A1 are at logic 1.
- Control word register can only be written into and no read operation of the CW register is allowed.
- Bit D7 of the control register specifies either the I/O function or the Bit Set/Reset function.
- If Bit D7 =1, bits D6- D1 determine I/O functions in various mode.
- If bit D7 = 0, port C operates in the Bit Set/Reset (BSR) mode.

Modes of Operation:

There are two basic modes of operation of 8255A.

- Bit Set-Reset mode – this mode is used to set or reset the bits of port C.
- I/O mode – In this mode, the 8255A ports work as programmable I/O ports.

MODE 0 (Simple input / Output): In this mode, port A, port B and port C is used as input or output.

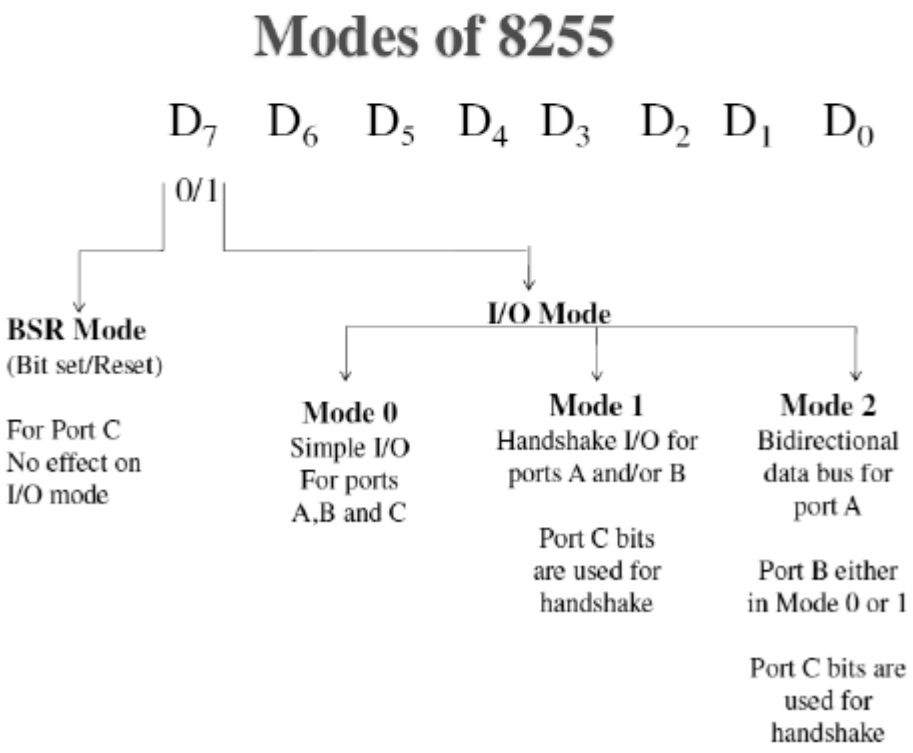
MODE 1 (Input/output with Hand shake): In this mode, input or output is transferred by hand shaking Signals. Port A and/or B are used input or output with handshake of port C.

Handshaking signals is used to transfer data between whose data transfer is not same.

MODE 2 (bi-directional I/O data transfer): This mode allows bidirectional data transfer over a single 8-bit data bus using handshake signals.

This feature is possible only Group A, Port A is working as 8-biy bidirectional, PC_3-PC_7 is used for handshaking purpose. Port B can be setup either in mode 0 or 1.

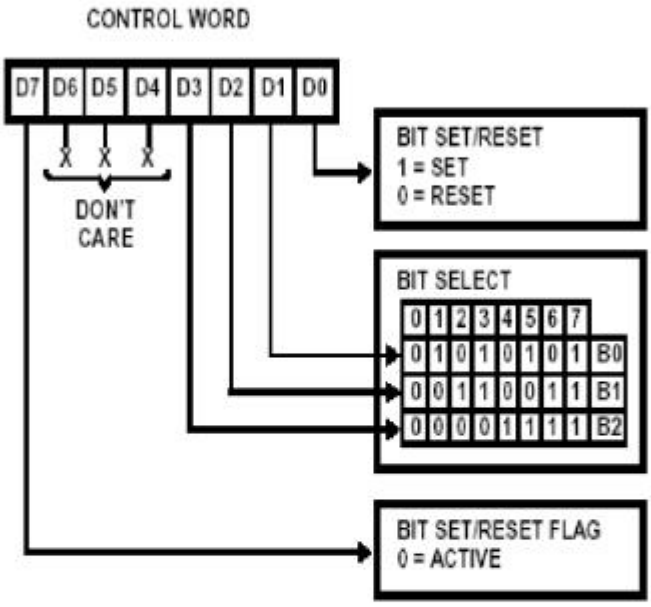
8255 Control Word:-

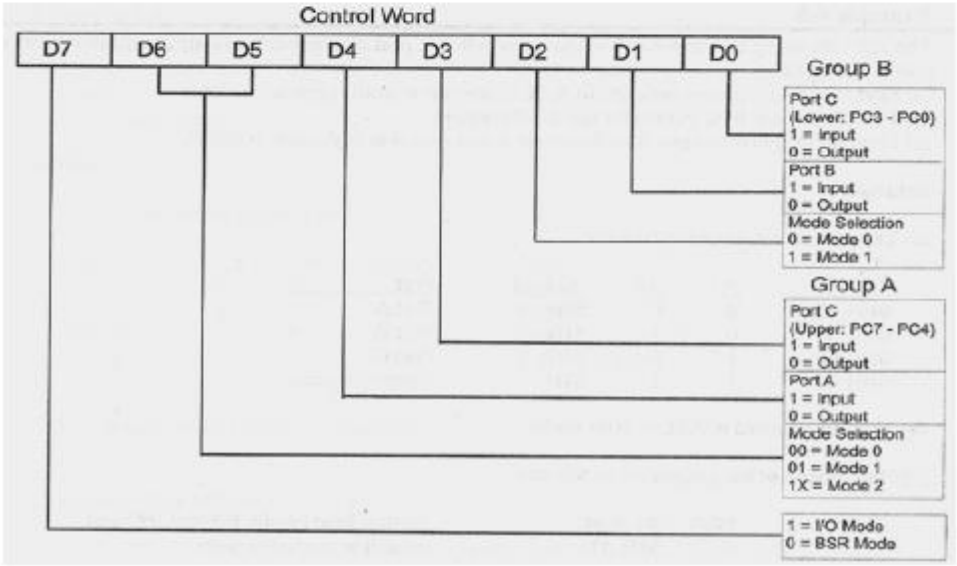


D_3	D_2	D_1	Selected bits of port C
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

BSR Mode : CWR Format

Control Word Format in the BSR Mode





I/O (Input/output) Mode:

Mode 0: Simple Input or Output

In this mode, ports A and B are used as two simple 8 bit ports and port C as two 4 bit ports.

Any port can be used as an input or output port (each port can be programmed to function as simply an input port or an output port).

The input/output features in Mode 0 are:-

- Output ports are latched.
- Input ports are buffered.
- 16 different Input/output configurations are possible.

Mode 1: Input or Output with handshake

The features of this mode are

- Two ports (A and B) function as 8 bit I/O ports. They can be configured either as input or output ports.
- Each port uses three lines from port C as handshake signals. The remaining two lines of port C can be used for simple I/O functions.
- Input and output data are latched.
- Interrupt logic is supported.

Mode 1: Input Control Signals:

Port A used 3 upper lines PC3, 4, 5, while Port B used PC0, 1, 2. The functions of these signals are as follows:

- Strobe STB.
- Input Buffer Full IBF.
- Interrupt Request INTR.
- Interrupt Enable INTE.