Introduction to Field-Effect Transistors (FETs)
Junction FET (JFET)

Field-effect transistors (FETs): Field-effect transistors (FETs) are fundamental semiconductor devices used for amplification and switching in electronic circuits. FETs are **voltage-controlled devices** that use an electric field to modulate the conductivity of a semiconductor channel.

Unlike bipolar junction transistors (BJTs), which rely on current flow into the base for control, FETs regulate the current flowing between the source and drain by controlling the voltage applied to the gate terminal. **Because the gate is insulated from the channel,** FETs draw extremely little current at their input; they behave as high-input-impedance devices.

FETs come in several families, most notably:

1. **junction FETs (JFETs)**
2. **metal-oxide-semiconductor FETs (MOSFETs)**.

Their unipolar nature – carriers are either electrons (n-channel) or holes (p-channel) – and low power consumption make them the foundation of modern analog and digital electronics.

Major Features of FETs

- **Voltage-controlled:** The drain current is controlled by the gate-source voltage rather than by a base current.
- **High input resistance:** Because the gate is reverse-biased or insulated, there is negligible gate current; this leads to input resistances in the mega-ohm or higher range.
- **Unipolar conduction:** Only one type of charge carrier (electrons or holes) flows through the channel, reducing noise and making FETs suitable for low-noise amplifiers.
- **Three-terminal device:** FETs have a source (S), drain (D) and gate (G). In some MOSFETs a fourth terminal (body/substrate) is also present.
- **Extensive applications:** MOSFETs form the building blocks of CMOS digital logic, memory, power regulators, analog switches and high-impedance buffers.

1. Junction FET (JFET)

A JFET uses a ***pn*-junction gate** to control current flow through a channel of semiconductor material. There are *n*-channel and *p*-channel varieties, depending on whether electrons or holes are the majority carriers.

JFET Symbols: The schematic symbols for both n-channel and p-channel JFETs are shown in Figure 1. Notice that the arrow on the gate points "in" for *n*-channel and "out" for *p*-channel.

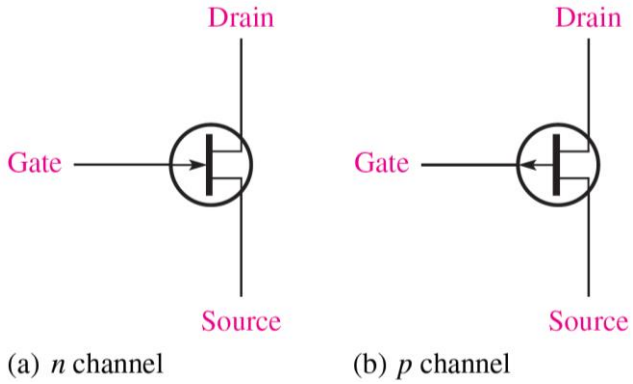

Figure 1: JFET schematic symbols

a) Construction

A typical *n*-channel JFET consists of a bar of n-type semiconductor with ohmic contacts at its ends to form the source (S) and drain (D) terminals. Two heavily doped p-type regions are diffused into opposite sides of the bar to form gate (G) junctions. These gates are usually tied together to form a single gate terminal. The thin region between the p-type gates is the conductive channel through which current flows. A *p*-channel device is constructed similarly but uses *p*-type material for the channel and *n*-type gates (carrier flow is by holes).

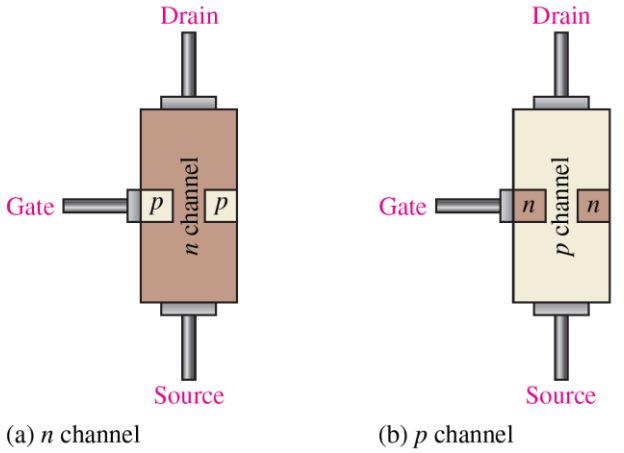

Figure 2: Cross-section of an a) n-channel JFET showing the n-type channel, p-type gate regions, source, drain and the depletion region. b) a) p-channel JFET showing the p-type channel, n-type gate regions, source, drain and the depletion region.

b) Operation and Characteristics

With the gate-source junction reverse-biased (or at zero bias), electrons flow from source to drain through the channel. Because the gate junctions are reverse biased, the depletion region surrounding the gate widens as the drain–source voltage increases. Applying a negative gate-source voltage V_{GS} further widens these depletion regions, narrowing the channel and reducing the drain current. Key operating features include:

- **Drain current control:** The drain current is controlled by the gate-source voltage. As V_{GS} becomes more negative, the channel narrows and the drain current decreases.
- **Pinch-off:** When the depletion regions from both gate sides meet, the channel is "pinched off." Increasing the drain–source voltage beyond this point does not increase the drain current significantly. The maximum drain current at $V_{GS} = 0$ V is called I_{DSS}.
- **Cut-off voltage:** There is a value of V_{GS}, denoted $V_{GS(\text{off})}$, at which the channel is completely closed, and the drain current is nearly zero.
- **Voltage-controlled current source:** In its saturation (or pinch-off) region, the JFET acts as a nearly constant current source; variations in V_{DS} have little effect on I_D.
- **High input resistance:** The reverse-biased gate draws negligible current, giving the device very high input impedance.

The I–V characteristics of a JFET show how I_D varies with V_{DS} for different gate-source voltages. Figure 2 illustrates typical curves for $V_{GS} = 0, -1$ and -2 V. The drain current initially increases linearly (ohmic region) then saturates at I_{DSS} when pinch-off occurs. More negative V_{GS} values reduce both the slope of the curve and the saturation current.

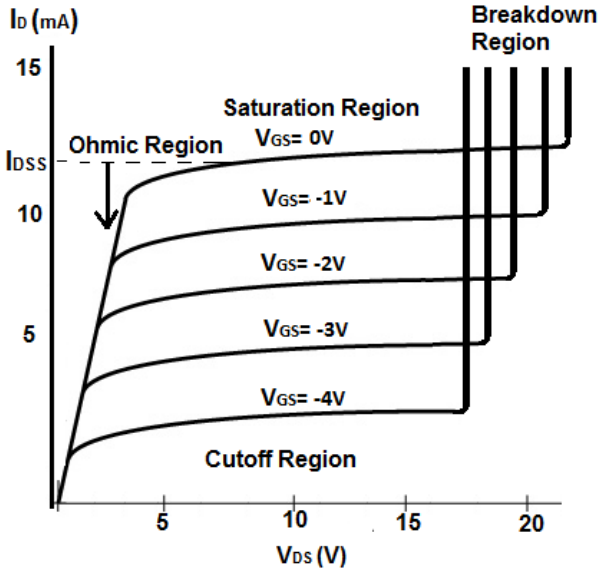

Figure 2: Simulated JFET drain–source characteristics for three gate-source voltages. As V_{GS} becomes more negative, the channel narrows and the drain current saturate at a lower value.