Department of Biomedical Engineering
Bio-Medical circuits and electronics / Third stage
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LECTURE TWO

MULTISTAGE & DIFFERENTIAL AMPLIFIER

2.1MULTISTAGE AMPLIFIERS

Two or more amplifiers can be connected in a **cascaded** arrangement with the output of one amplifier driving the input of the next. Each amplifier in a cascaded arrangement is known as a **stage.** The basic purpose of a multistage arrangement is to increase the overall voltage gain.

Multistage Voltage Gain

The overall voltage gain $A'v$ of cascaded amplifiers, as shown in Figure 2.1, is the product of the individual voltage gains

$$A'_v = A_{v1}A_{v2}A_{v3}\ldots\ldots A_{vn}$$

where ***n*** *is the number of stages.*

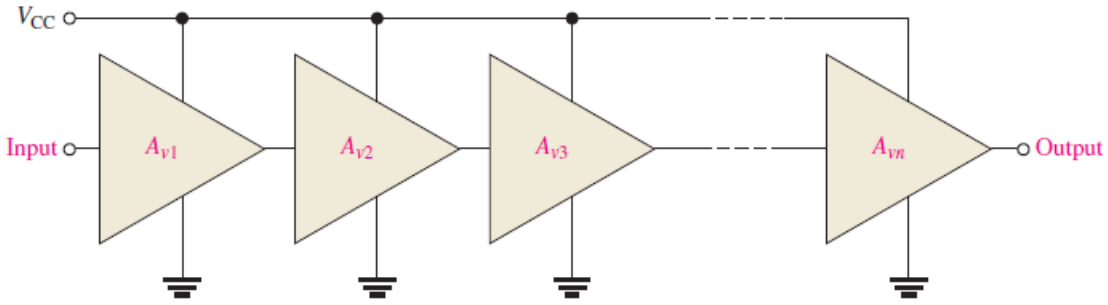


Figure 2. 1: Cascaded amplifiers. Each triangular symbol represents a separate amplifier

Amplifier voltage gain is often expressed in decibels (dB) as follows:

$$A_{v(\text{dB})} = 20 \log A_v$$

This is particularly useful in **multistage** systems because the overall voltage gain in dB is the *sum* of the individual voltage gains in dB.

$$A'_{v(\text{dB})} = A_{v1(\text{dB})} + A_{v2(\text{dB})} + \ldots + A_{vn(\text{dB})}$$

EXAMPLE 2-1: A certain cascaded amplifier arrangement has the following voltage gains: $A_{v1} = 10$, $A_{v2} = 15$, and $A_{v3} = 20$. What is the overall voltage gain? Also express each gain in decibels (dB) and determine the total voltage gain in dB.

Solution

$$A'_v = A_{v1}A_{v2}A_{v3} = (10)(15)(20) = \mathbf{3000}$$

$$A_{v1(\text{dB})} = 20 \log 10 = \mathbf{20.0\ dB}$$

$$A_{v2(\text{dB})} = 20 \log 15 = \mathbf{23.5\ dB}$$

$$A_{v3(\text{dB})} = 20 \log 20 = \mathbf{26.0\ dB}$$

$$A'_{v(\text{dB})} = 20.0\ \text{dB} + 23.5\ \text{dB} + 26.0\ \text{dB} = \mathbf{69.5\ dB}$$

Capacitively-Coupled Multistage Amplifier

For illustrative purposes, we will use the two-stage capacitively coupled amplifier shown in Figure 2.2. Notice that both stages are identical common-emitter amplifiers with the output of the first stage capacitively coupled to the input of the second stage. Capacitive coupling prevents the dc bias of one stage from affecting that of the other, but allows the ac signal to pass without attenuation because of the frequency of operation.

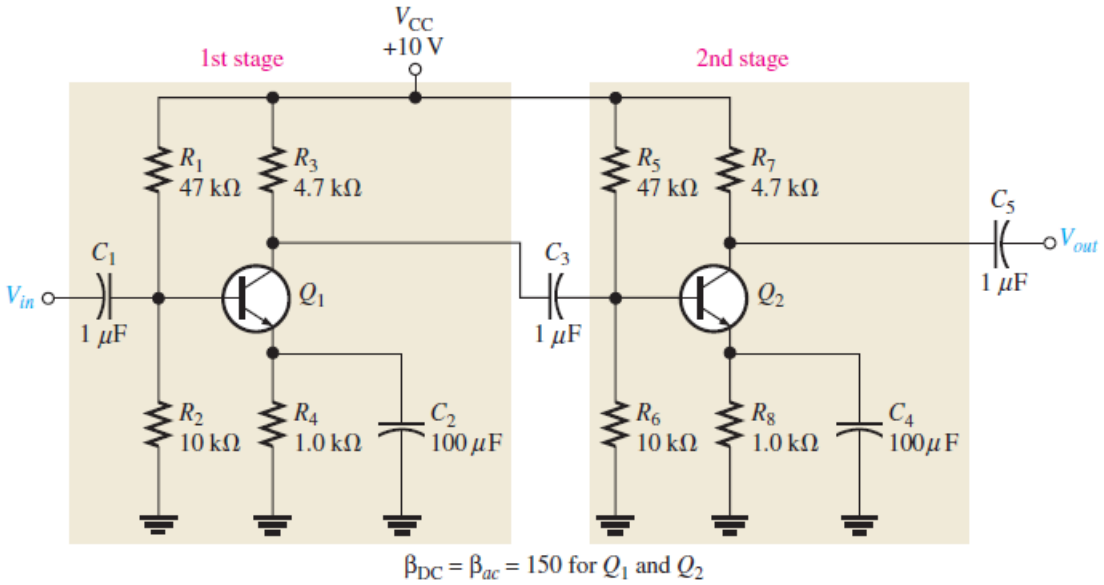


Figure 2. 2: A two-stage common-emitter amplifier.

Loading Effects

In determining the voltage gain of the first stage, you must consider the *loading effect* of the second stage. Because the coupling capacitor *C*3 effectively appears as a short at the signal frequency, *the total input resistance of the second stage presents an ac load to the first stage.*

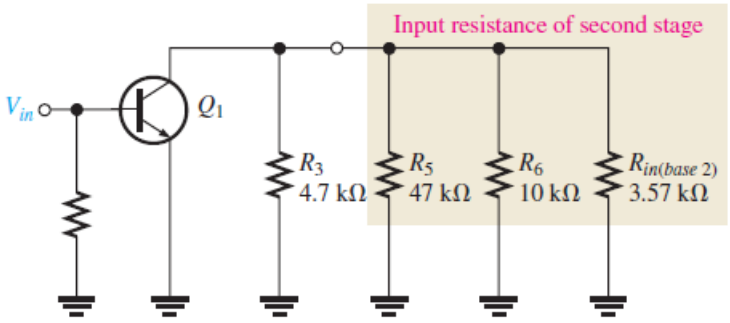


Figure 2. 3: AC equivalent of the first stage in Figure 2–2, showing loading from the second stage input resistance

Voltage Gain of the First Stage

The ac collector resistance of the first stage is $Rc_1 = R3 \,//\, R5 \,//\, R6 \,//\, Rin(base2)$

Remember that lowercase italic subscripts denote ac quantities, such as for Rc.

You can verify that $I_E = 1.05$ mA, $r'e = 23.8\Omega$, $R_{in(base2)} = 3.57$ kΩ. ($= \beta_{ac}.\ r'e$).

The effective ac collector resistance of the first stage is as follows:

$Rc1 = 4.7\ k\Omega \,//\, 47\ k\Omega \,//\, 10\ k\Omega \,//\, 3.57\ k\Omega = 1.63\ k\Omega$

Therefore, the base-to-collector voltage gain of the first stage is

$$A_{v1} = \frac{R_{c1}}{r'_e} = \frac{1.63\ k\Omega}{23.8\ \Omega} = 68.5$$

Voltage Gain of the Second Stage

The second stage has no load resistor, so the ac collector resistance is $R7$, and the gain is

$$A_{v2} = \frac{R_7}{r'_e} = \frac{4.7\ k\Omega}{23.8\ \Omega} = 197$$

Compare this to the gain of the first stage, and notice how much the loading from the second stage reduced the gain.

Overall Voltage Gain: The overall amplifier gain with no load on the output is

$$A'_v = A_{v1}A_{v2} = (68.5)(197) \cong 13{,}495$$

If an input signal of 100 μV, for example, is applied to the first stage, and if there is no attenuation in the input base circuit due to the source resistance, an output from the second stage of (100 μV)(13,495) ≈ 1.35V will result.

The overall voltage gain can be expressed in dB as follows:

$$A'_{v(dB)} = 20 \log (13{,}495) = 82.6\ dB$$

DC Voltages in the Capacitively Coupled Multistage Amplifier

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{10\,k\Omega}{57\,k\Omega}\right)10\,V = 1.75\,V$$

The dc emitter and collector voltages are as follows:

$$V_E = V_B - 0.7\,V = 1.05\,V$$
$$I_E = \frac{V_E}{R_4} = \frac{1.05\,V}{1.0\,k\Omega} = 1.05\,mA$$
$$I_C \cong I_E = 1.05\,mA$$
$$V_C = V_{CC} - I_C R_3 = 10\,V - (1.05\,mA)(4.7\,k\Omega) = 5.07\,V$$

2.2THE DIFFERENTIAL AMPLIFIER

A **differential amplifier** is an amplifier that produces outputs that are a function of the difference between two input voltages. The differential amplifier has two basic modes of operation: differential (in which the two inputs are different) and common mode (in which the two inputs are the same).

Basic Operation

A basic differential amplifier (diff-amp) circuit is shown in Figure 2-4. Notice that the differential amplifier has two inputs and two outputs.

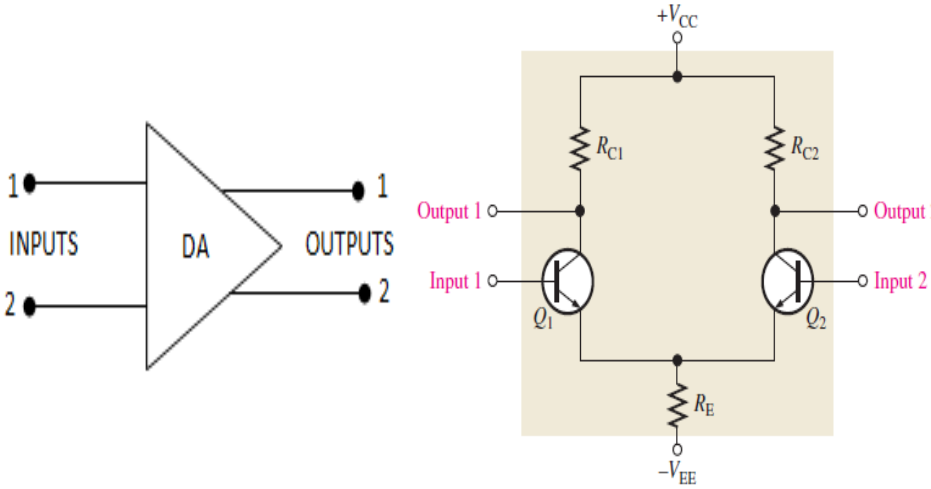


Figure 2. 4: Basic differential amplifier.

The following discussion is in relation to Figure 2–5 and consists of **a basic dc analysis of the diff-amp's operation**. First, when both inputs are grounded (0 V), the emitters are at -0.7 V, as indicated in Figure 2–5(a). It is assumed that the transistors are identically matched by careful process control during manufacturing so that their dc emitter currents are the same when there is no input signal. Thus,

$$I_{E1} = I_{E2}$$

Since both emitter currents combine through R_E,

$$I_{E1} = I_{E2} = \frac{I_{R_E}}{2}$$

Where

$$I_{R_E} = \frac{V_E - V_{EE}}{R_E}$$

Based on the approximation that $I_C \approx I_E$

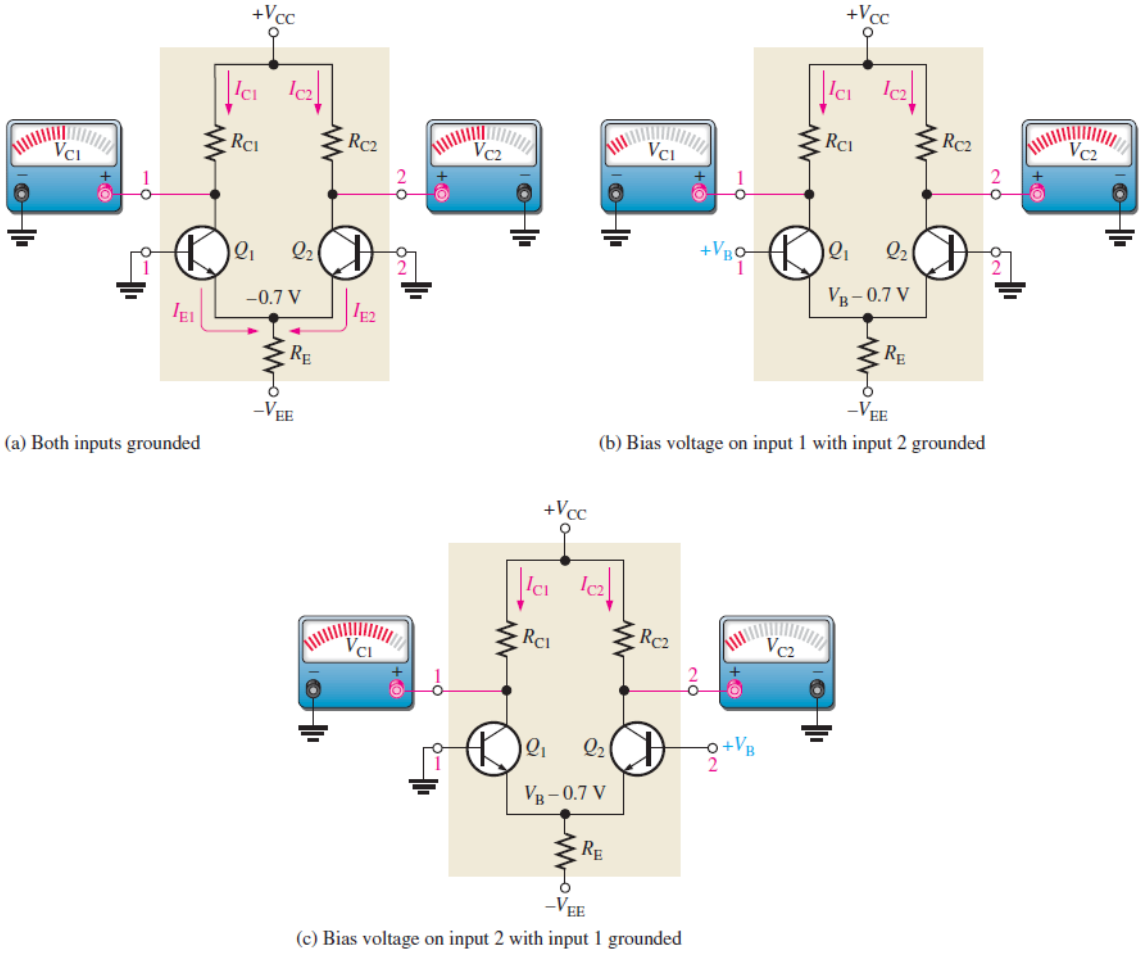
$$I_{C1} = I_{C2} \cong \frac{I_{R_E}}{2}$$

Since both collector currents and both collector resistors are equal (when the input voltage is zero),

$$V_{C1} = V_{C2} = V_{CC} - I_{C1}R_{C1}$$

$$V_E = V_B - 0.7\,\text{V}$$

This action reduces the forward bias (V_{BE}) of Q_2 because its base is held at 0 V (ground), thus causing I_{C2} to decrease. The net result is that the increase in I_{C1} causes a decrease in V_{C1}, and the decrease in I_{C2} causes an increase in V_{C2}, as shown.



(a) Both inputs grounded

(b) Bias voltage on input 1 with input 2 grounded

(c) Bias voltage on input 2 with input 1 grounded

Figure 2. 5: Basic operation of a differential amplifier (ground is zero volts) showing relative changes in voltages.

Modes of Signal Operation

Single-Ended Differential Input

When a diff-amp is operated with this input configuration, one input is grounded, and the signal voltage is applied only to the other input, as shown in Figure 2–6. In the case where the signal voltage is applied to input 1, as in part (a), an inverted, amplified signal voltage appears at output 1 as shown. Also, a signal

voltage appears in phase at the emitter of $Q1$. Since the emitters of $Q1$ and $Q2$ are common, the emitter signal becomes an input to $Q2$, which functions as a common-base amplifier. The signal is amplified by $Q2$ and appears, noninverted, at output 2.

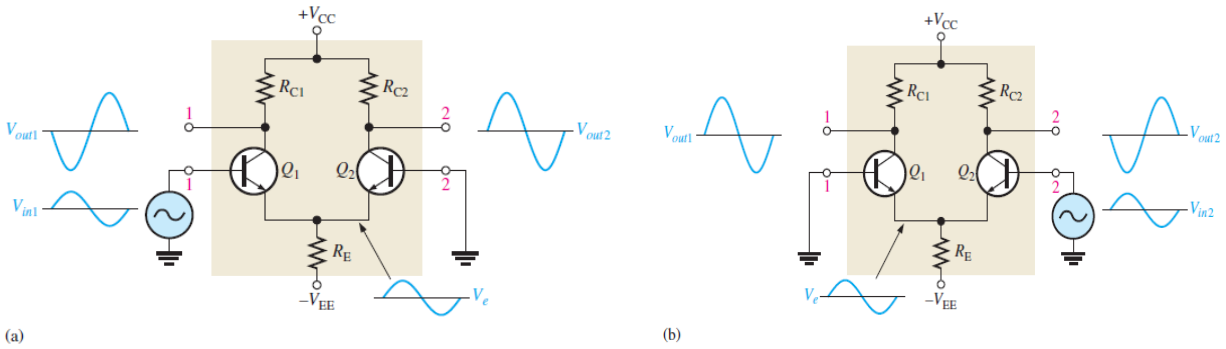
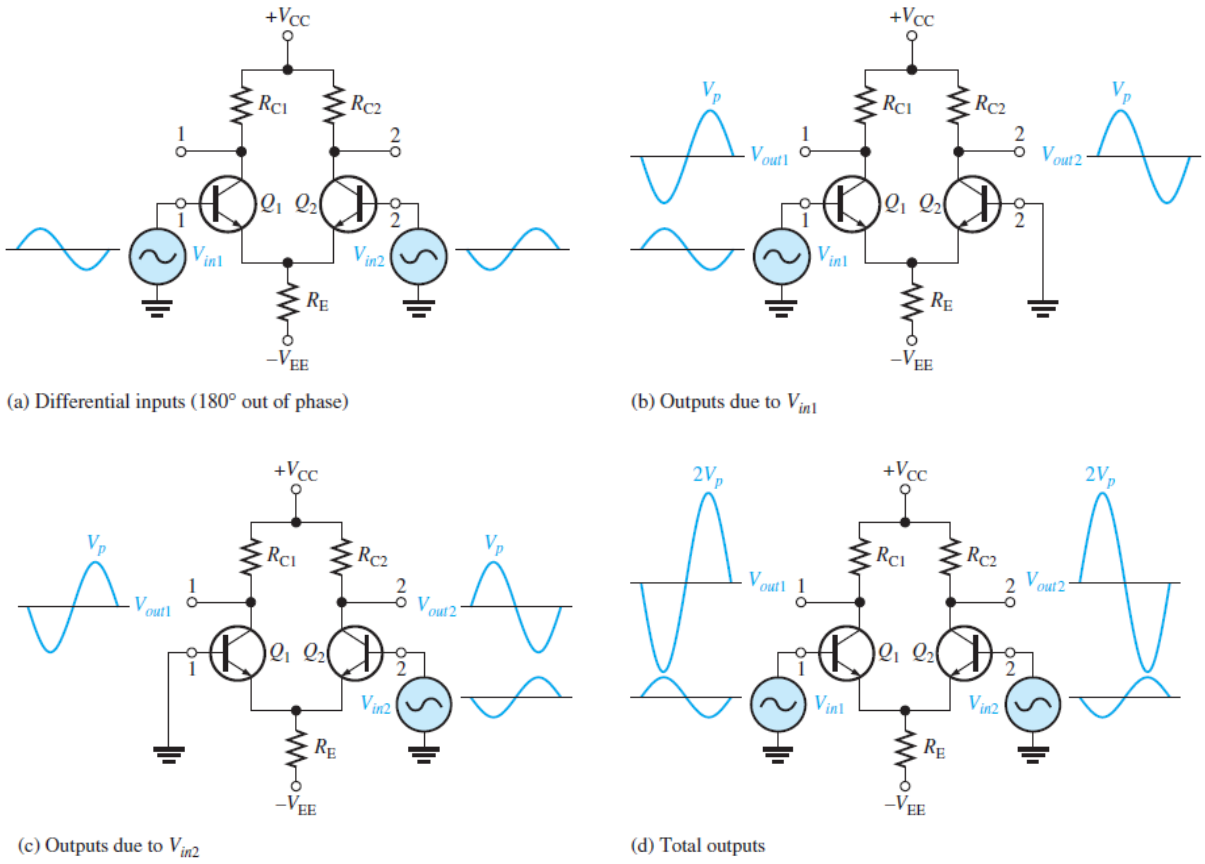


Figure 2. 6: Single-ended differential input operation.

Double-Ended Differential Inputs

In this input configuration, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in Figure 2–7(a). Each input affects the outputs, as you will see in the following discussion. Figure 2–7(b) shows the output signals due to the signal on input 1 acting alone as a single-ended input. Figure 2–7(c) shows the output signals due to the signal on input 2 acting alone as a single-ended input. Notice in parts (b) and (c) that the signals on output 1 are of the same polarity. The same is also true for output 2. By superimposing both output 1 signals and both output 2 signals, you get the total output signals, as shown in Figure 2–7(d).



(a) Differential inputs (180° out of phase)

(b) Outputs due to V_{in1}

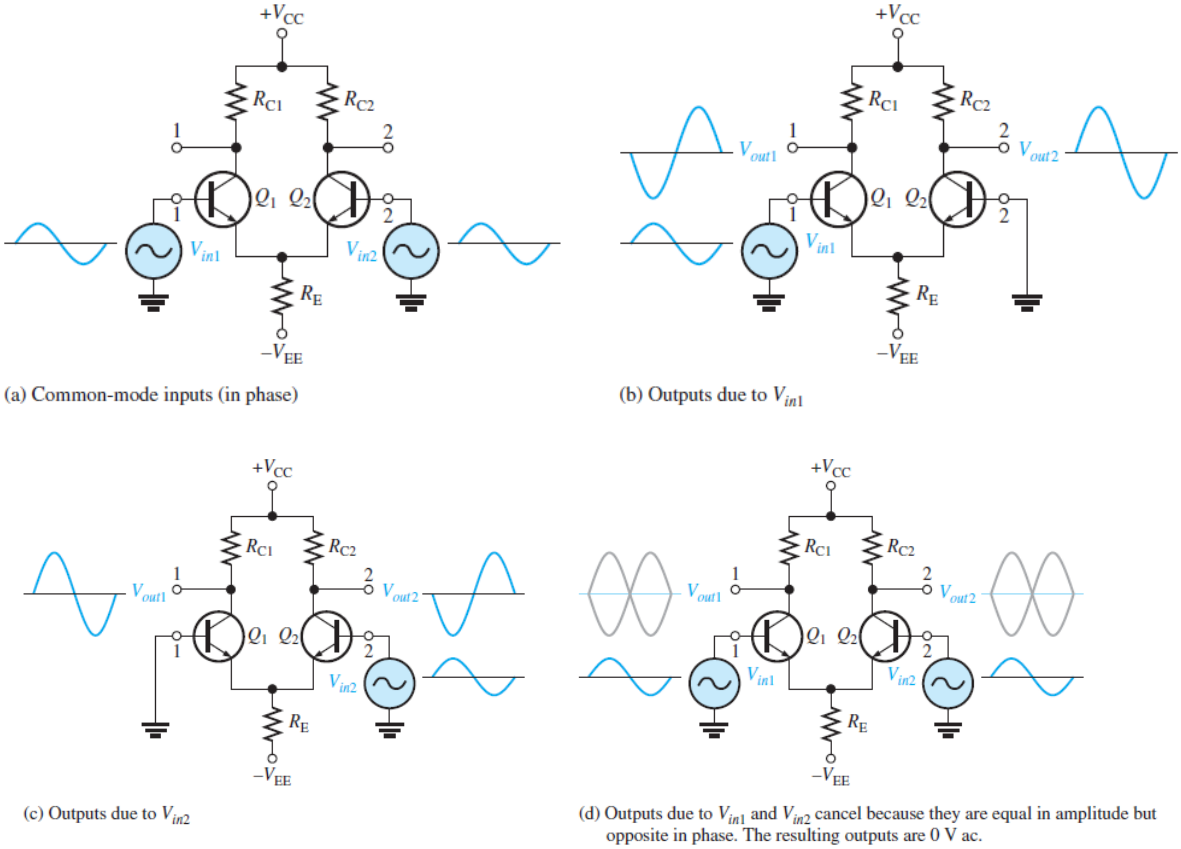
(c) Outputs due to V_{in2}

(d) Total outputs

Figure 2. 7: Double-ended differential operation.

Common-Mode Inputs

One of the most important aspects of the operation of a diff-amp can be seen by considering the **common-mode** condition where two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in Figure 2–8(a). Again, by considering each input signal as acting alone, you can understand the basic operation



(a) Common-mode inputs (in phase)

(b) Outputs due to V_{in1}

(c) Outputs due to V_{in2}

(d) Outputs due to V_{in1} and V_{in2} cancel because they are equal in amplitude but opposite in phase. The resulting outputs are 0 V ac.

Figure 2. 8: Common-mode operation of a differential amplifier.

Figure 2–8(b) shows the output signals due to the signal on only input 1, and Figure 2–8(c) shows the output signals due to the signal on only input 2. Notice that the corresponding signals on output 1 are of the opposite polarity, and so are the ones on output 2.

When the input signals are applied to both inputs, the outputs are superimposed, and they cancel, resulting in a zero-output voltage, as shown in Figure 2–8(d).