1. Pretest

Q. give the steps of obtaining ac equivalent of a JFET network

2. Theory

Introduction

Field-effect transistor amplifiers provide an excellent voltage gain with th added feature of a high input impedance. They are also low-power-consumption configurations with good frequency range and minimal size and weight. JFETs, depletion MOSFETs, and MESFETs can be used to design amplifiers having similar voltage gains. The depletion MOSFET (MESFET) circuit, however, has a much higher input impedance than a similar JFET configuration. Whereas a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. Whereas the BJT has an amplification factor, b (beta), the FET has a transconductance factor, $g\,m$.

JFET SMALL-SIGNAL MODEL

The ac analysis of a JFET configuration requires that a small-signal ac model for the JFET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of a JFET.

Recall from Chapter 7 that a dc gate-to-source voltage controls the level of dc drain current through a relationship known as Shockley's equation: $ID = IDSS\,(1 - VGS/VP)^2$. The *change* in drain current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta ID = g_m \Delta VGS \qquad (1)$$

The prefix *trans* - in the terminology applied to $g\,m$ reveals that it establishes a relationship between an output and an input quantity. The root word *conductance*

was chosen because $g\ m$ is determined by a current-to-voltage ratio similar to the ratio that defines the conductance of a resistor, $G = 1/R = I/V$.
Solving for $g\ m$ in Eq. (1), we have

$$gm = \frac{\Delta ID}{\Delta VGS} \qquad (2)$$

Graphical Determination of gm

If we now examine the transfer characteristics of Fig. 8.1 , we find that g m is actually the slope of the characteristics at the point of operation. That is,

$$gm = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}} \qquad (3)$$

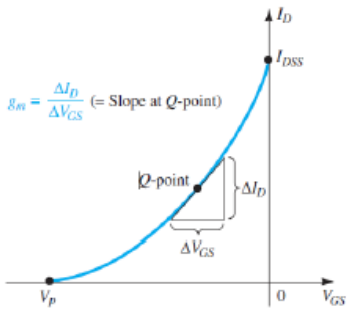

FIG. 8.1
Definition of g_m using transfer characteristic.

Mathematical Definition of g m

The graphical procedure just described is limited by the accuracy of the transfer plot and the care with which the changes in each quantity can be determined. Naturally, the larger the graph, the better is the accuracy, but this can then become a cumbersome problem. An alternative approach to determining $g\ m$ employs the approach used to find the ac resistance of a diode in Chapter 1 , where it was stated that:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

EXAMPLE 1 Determine the magnitude of $g\ m$ for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V at the following dc bias points:

a. V_{GS} = -0.5 V.
b. V_{GS} = -1.5 V.
c. V_{GS} = -2.5 V.

Solution: The transfer characteristics are generated as Fig. 8.2 using the procedure defined in Chapter 7. Each operating point is then identified and a tangent line is drawn at each point to best reflect the slope of the transfer curve in this region. An appropriate increment is then chosen for V_{GS} to reflect a variation to either side of each Q-point. Equation (8.2) is then applied to determine g_m.

a. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{2.1\text{ mA}}{0.6\text{ V}} = \mathbf{3.5\text{ mS}}$

b. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{1.8\text{ mA}}{0.7\text{ V}} \cong \mathbf{2.57\text{ mS}}$

c. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{1.5\text{ mA}}{1.0\text{ V}} = \mathbf{1.5\text{ mS}}$

Note the decrease in g_m as V_{GS} approaches V_P.

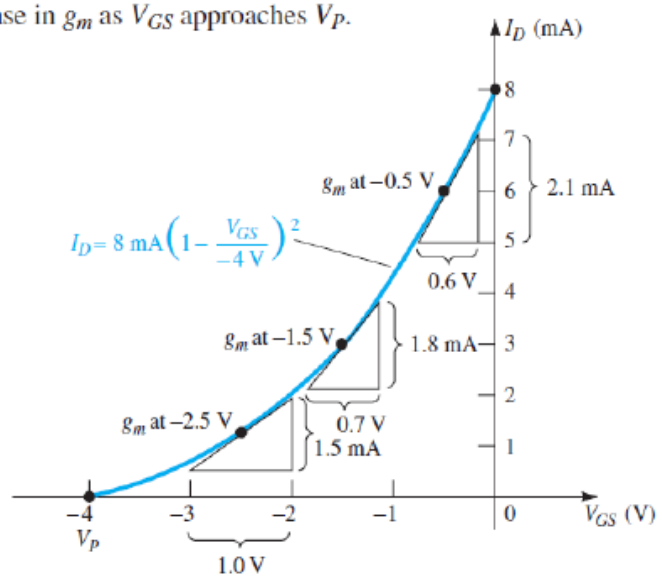

FIG. 8.2
Calculating g_m at various bias points.

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, we can derive an equation for g_m as follows:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$
$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$
$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

and

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right] \tag{4}$$

where $|V_P|$ denotes magnitude only, to ensure a positive value for g_m.

It was mentioned earlier that the slope of the transfer curve is a maximum at $V_{GS} = 0$ V. Plugging in $V_{GS} = 0$ V into Eq. (4) results in the following equation for the maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

and

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} \tag{5}$$

where the added subscript 0 reminds us that it is the value of g_m when $V_{GS} = 0$ V. Equation (4) then becomes

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] \tag{6}$$

EXAMPLE 2 For the JFET having the transfer characteristics of Example 1 :
a. Find the maximum value of $g\,m$.
b. Find the value of $g\,m$ at each operating point of Example 8.1 using Eq. (6) and compare
with the graphical results.

Solution: The transfer characteristics are generated as Fig. 8.2 using the procedure defined in Chapter 7. Each operating point is then identified and a tangent line is drawn at each point to best reflect the slope of the transfer curve in this region. An appropriate increment is then chosen for V_{GS} to reflect a variation to either side of each Q-point. Equation (8.2) is then applied to determine g_m.

a. $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{2.1\text{ mA}}{0.6\text{ V}} = \mathbf{3.5\text{ mS}}$$

b. $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{1.8\text{ mA}}{0.7\text{ V}} \cong \mathbf{2.57\text{ mS}}$$

c. $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1.5\text{ mA}}{1.0\text{ V}} = \mathbf{1.5\text{ mS}}$$

Note the decrease in g_m as V_{GS} approaches V_P.

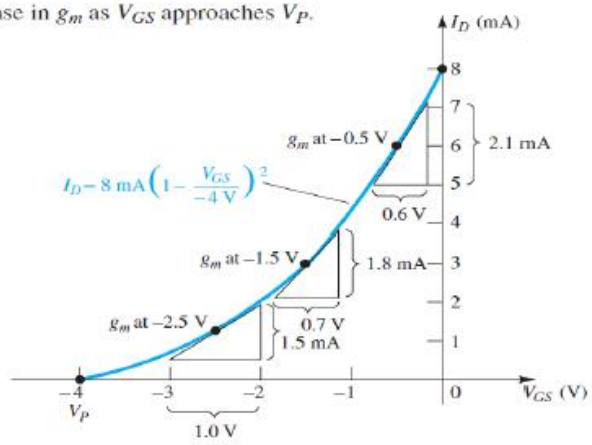

FIG. 8.2
Calculating g_m at various bias points.

Plotting g_m versus V_{GS}

Since the factor $\left(1 - \frac{V_{GS}}{V_P}\right)$ of Eq. (8.6) is less than 1 for any value of V_{GS} other than 0 V, the magnitude of g_m will decrease as V_{GS} approaches V_P and the ratio $\frac{V_{GS}}{V_P}$ increases in magnitude. At $V_{GS} = V_P$, $g_m = g_{m0}(1 - 1) = 0$. Equation (8.6) defines a straight line with a minimum value of 0 and a maximum value of g_m, as shown by the plot of Fig. 8.3.

In general, therefore

the maximum value of g_m occurs where $V_{GS} = 0$ V and the minimum value at $V_{GS} = V_P$. The more negative the value of V_{GS} the less the value of g_m.

Figure 8.3 also shows that when V_{GS} is one-half the pinch-off value, g_m is one-half the maximum value.

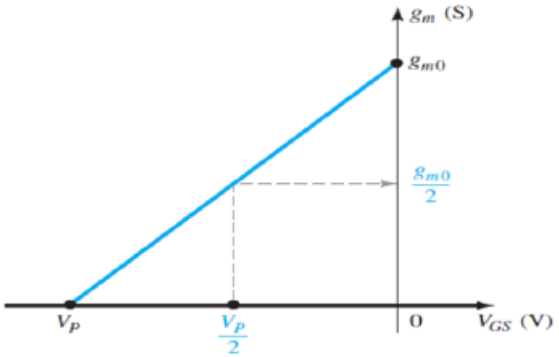

FIG. 8.3
Plot of g_m versus V_{GS}.

Effect of I_D on g_m

A mathematical relationship between g_m and the dc bias current I_D can be derived by noting that Shockley's equation can be written in the following form:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \tag{8.8}$$

Substituting Eq. (8.8) into Eq. (8.6) results in

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}} \tag{8.9}$$

Using Eq. (8.9) to determine g_m for a few specific values of I_D, we obtain the following results:

a. If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = \mathbf{g_{m0}}$$

b. If $I_D = I_{DSS}/2$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = \mathbf{0.707g_{m0}}$$

c. If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = \mathbf{0.5g_{m0}}$$

JFET Input Impedance Zi

The input impedance of all commercially available JFETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i\,(\text{JFET}) = \infty\,\Omega \tag{8.10}$$

For a JFET a practical value of $10^9\ \Omega$ (1000 MΩ) is typical, whereas a value of $10^{12}\ \Omega$ to $10^{15}\ \Omega$ is typical for MOSFETs and MESFETs.

JFET Output Impedance Zo

The output impedance of JFETs is similar in magnitude to that of conventional BJTs. On JFET specification sheets, the output impedance will typically appear as g_{os} or y_{os} with the units of μS. The parameter y_{os} is a component of an *admittance equivalent circuit*, with the subscript *o* signifying an *o*utput network parameter and *s* the terminal (*s*ource) to which it is attached in the model. For the JFET of Fig. 6.20, g_{os} has a range of 10 μS to 50 μS or 20 kΩ ($R = 1/G = 1/50\ \mu S$) to 100 kΩ ($R = 1/G = 1/10\ \mu S$).

In equation form,

$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}} \tag{8.11}$$

The output impedance is defined on the characteristics of Fig. 8.6 as the slope of the horizontal characteristic curve at the point of operation. The more horizontal the curve, the greater is the output impedance. If it is perfectly horizontal, the ideal situation is on hand with the output impedance being infinite (an open circuit)—an often applied approximation.

In equation form,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}} \tag{8.12}$$

Note the requirement when applying Eq. (8.12) that the voltage V_{GS} remain constant when r_d is determined. This is accomplished by drawing a straight line approximating the V_{GS} line at the point of operation. A ΔV_{DS} or ΔI_D is then chosen and the other quantity measured off for use in the equation.

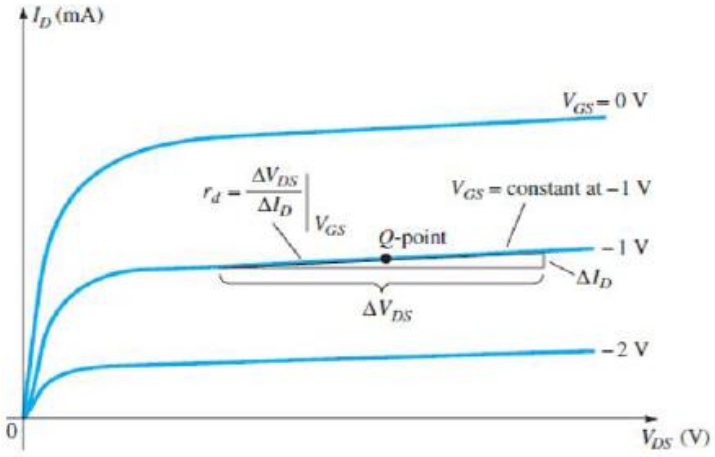

FIG. 8.6
Definition of r_d using JFET drain characteristics.

JFET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the JFET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 8.8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

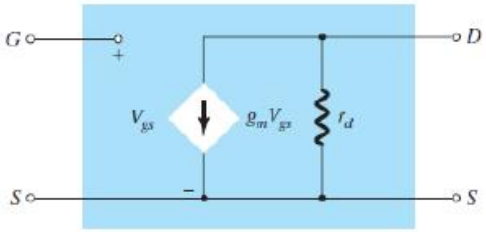

FIG. 8.8
JFET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate-to-source voltage is now represented by V_{gs} (lowercase subscripts) to distinguish it from dc levels. In addition, note that the source is common to both input and output circuits, whereas the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$. In situations where r_d is ignored (assumed sufficiently large in relation to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal V_{gs} and parameter g_m —clearly a voltage-controlled current source.

EXAMPLE 4

Given $\mathbf{g}_{fs} = 3.8$ mS and $\mathbf{g}_{os} = 20$ mS, sketch the FET ac equivalent model.

Solution:

$$g_m = g_{fs} = 3.8 \text{ mS} \qquad \text{and} \qquad r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = 50\ \text{k}\Omega$$

resulting in the ac equivalent model of Fig. 8.9.

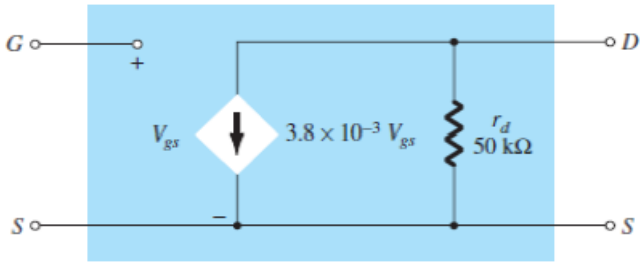

FIG. 8.9
JFET ac equivalent model for Example 8.6.

FIXED-BIAS CONFIGURATION

Now that the JFET equivalent circuit has been defined, a number of fundamental JFET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of ***Zi*** , ***Zo*** , and ***Av*** for each configuration. The *fixed-bias* configuration of Fig. 8.10 includes the coupling capacitors $C1$ and $C2$, which isolate the dc biasing arrangement from the applied signal and load; they act as shortcircuit equivalents for the ac analysis.

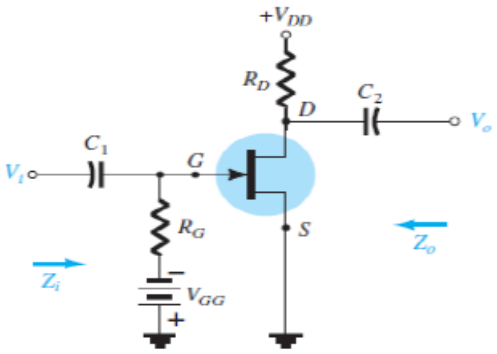

FIG. 8.10
JFET fixed-bias configuration.

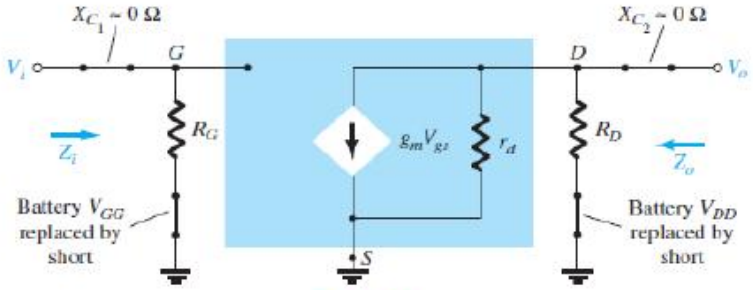

FIG. 8.11
Substituting the JFET ac equivalent circuit unit into the network of Fig. 8.10.

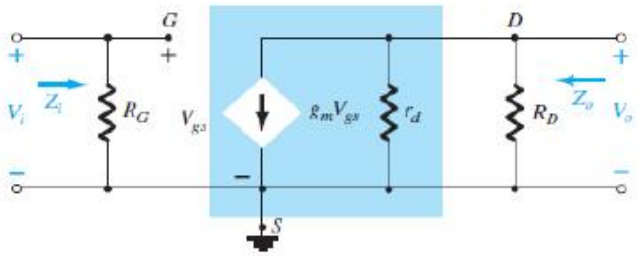

FIG. 8.12
Redrawn network of Fig. 8.11.

Z_i Figure 8.12 clearly reveals that

$$\boxed{Z_i = R_G} \tag{8.13}$$

because of the infinite input impedance at the input terminals of the JFET.

Z_o Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 8.13. The output impedance is

$$\boxed{Z_o = R_D \| r_d} \tag{8.14}$$

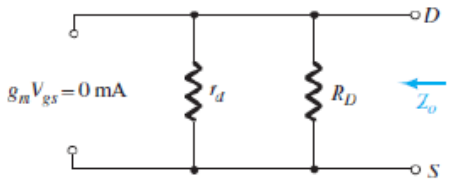

FIG. 8.13
Determining Z_o.

If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation $r_d \| R_D \cong R_D$ can often be applied and

$$\boxed{Z_o \simeq R_D}_{r_d \geq 10R_D} \tag{8.15}$$

A_v Solving for V_o in Fig. 8.12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $$V_{gs} = V_i$$

and $$V_o = -g_m V_i (r_d \| R_D)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{8.16}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m R_D}_{r_d \geq 10R_D} \tag{8.17}$$

Phase Relationship The negative sign in the resulting equation for A_v clearly reveals a phase shift of 180° between input and output voltages.

EXAMPLE 8.7 The fixed-bias configuration of Example 7.1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 8.14 with an applied signal V_i. The value of y_{os} is provided as 40 μS.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o.
e. Determine the voltage gain A_v.
f. Determine A_v ignoring the effects of r_d.

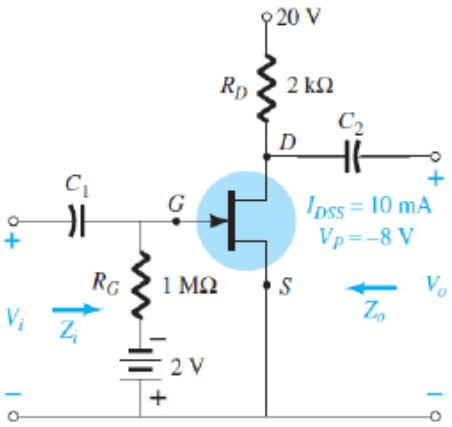

FIG. 8.14
JFET configuration for Example 8.7.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$

c. $Z_i = R_G = \mathbf{1\ M\Omega}$

d. $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

e. $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$
$= \mathbf{-3.48}$

f. $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D results in a difference of 8% in the solution.

SELF-BIAS CONFIGURATION

Bypassed R_S

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 8.15 requires only one dc supply to establish the desired operating point.

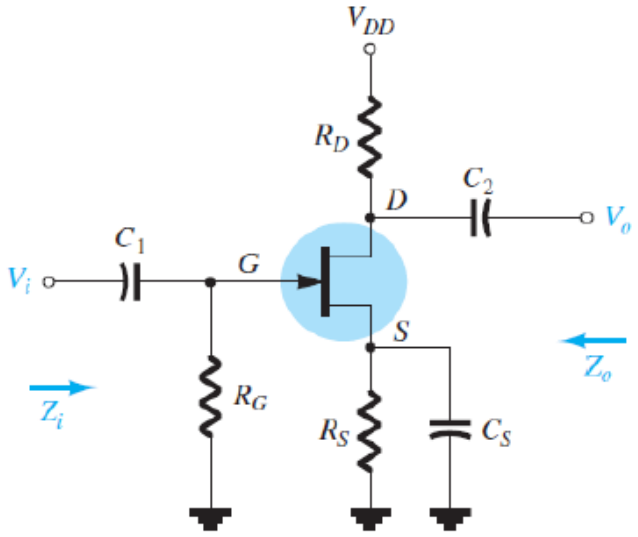

FIG. 8.15
Self-bias JFET configuration.

The JFET equivalent circuit is established in Fig. 8.16 and carefully redrawn in Fig. 8.17 . Since the resulting configuration is the same as appearing in Fig. 8.12 , the resulting equations for *Zi* , *Zo* , and *Av* will be the same

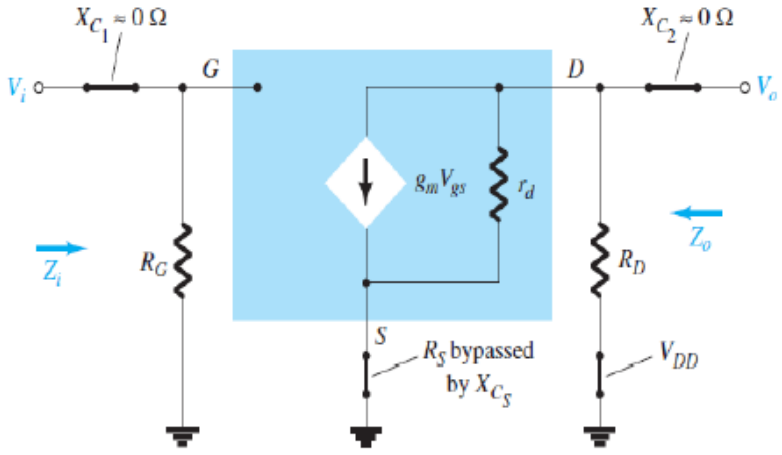

FIG. 8.16
Network of Fig. 8.15 following the substitution of the JFET ac equivalent circuit.

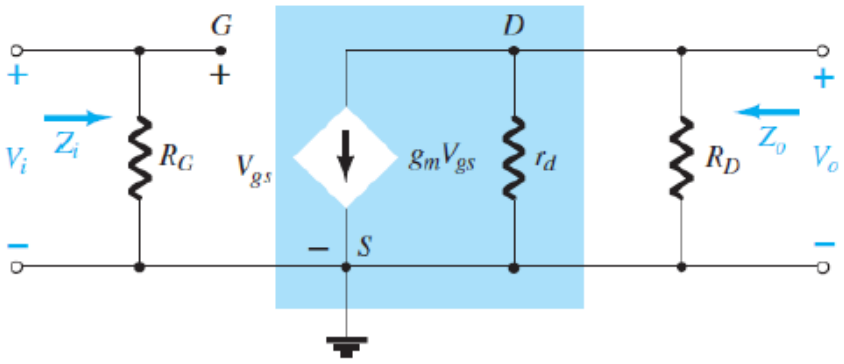

FIG. 8.17
Redrawn network of Fig. 8.16.

Z_i

$$Z_i = R_G \tag{8.18}$$

Z_o

$$Z_o = r_d \| R_D \tag{8.19}$$

If $r_d \geq 10R_D$,

$$Z_o \cong R_D \quad _{r_d \geq 10R_D} \tag{8.20}$$

A_v

$$A_v = -g_m(r_d \| R_D) \tag{8.21}$$

If $r_d \geq 10R_D$,

$$A_v = -g_m R_D \quad _{r_d \geq 10R_D} \tag{8.22}$$

Phase Relationship The negative sign in the solutions for A_v again indicates a phase shift of 180° between V_i and V_o.

EXAMPLE 8.8 The self-bias configuration of Example 7.2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 8.20 with an applied signal V_i. The value of g_{os} is given as 20 μS.

a. Determine g_m.
b. Find r_d.
c. Find Z_i.
d. Calculate Z_o with and without the effects of r_d. Compare the results.
e. Calculate A_v with and without the effects of r_d. Compare the results.

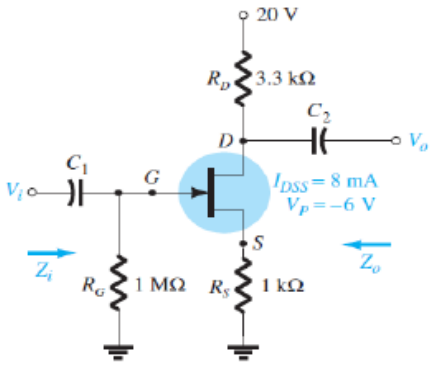

FIG. 8.20
Network for Example 8.8.

3. Self-test

Draw the ac equivalent network of fixed bias network?

VOLTAGE-DIVIDER CONFIGURATION

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 8.21 .

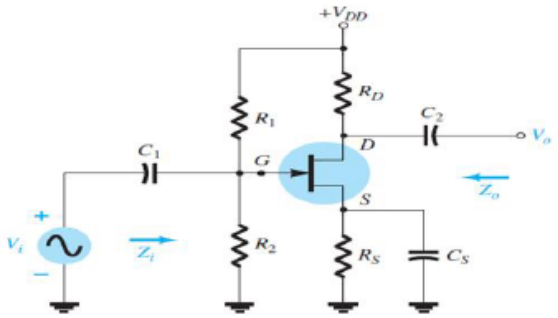

FIG. 8.21
JFET voltage-divider configuration.

Z_i R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET, resulting in

$$Z_i = R_1 \| R_2 \tag{8.28}$$

Z_o Setting $V_i = 0$ V sets V_{gs} and $g_m V_{gs}$ to zero, and

$$Z_o = r_d \| R_D \tag{8.29}$$

For $r_d \geq 10R_D$,

$$Z_o \cong R_D \quad r_d \geq 10R_D \tag{8.30}$$

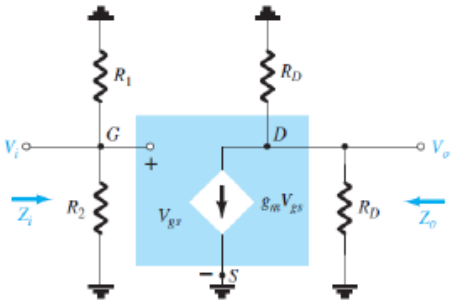

FIG. 8.22
Network of Fig. 8.21 under ac conditions.

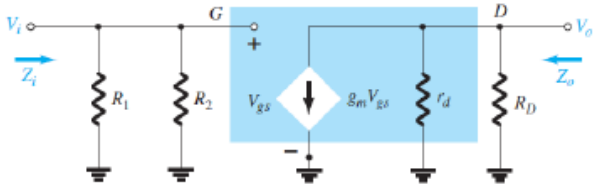

FIG. 8.23
Redrawn network of Fig. 8.22.

A_v

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \tag{8.31}$$

If $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \quad r_d \geq 10R_D \tag{8.32}$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i, which is now sensitive to the parallel combination of R_1 and R_2.