COMMON-GATE CONFIGURATION

The last JFET configuration to be analyzed in detail is the **common-gate configuration** of Fig. 8.24, which parallels the common-base configuration employed with BJT transistors. Substituting the JFET equivalent circuit results in Fig. 8.25. Note the continuing requirement that the controlled source g_m V_{gs} be connected from drain to source with r_d in parallel. The isolation between input and output circuits has obviously been lost since the gate terminal is now connected to the common ground of the network, and the controlled current source is connected directly from drain to source. In addition, the resistor connected between the input terminals is no longer R_G, but the resistor R_S connected from the source to ground. Note also the location of the controlling voltage Vgs and the fact that it appears directly across the resistor R_S

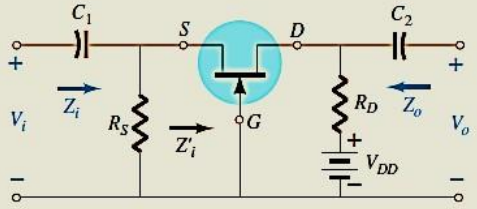

FIG. 8.24
JFET common-gate configuration.

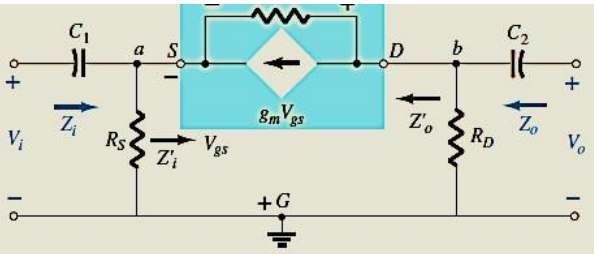

FIG. 8.25
Network of Fig. 8.24 following substitution of JFET ac equivalent model.

Z_i The resistor R_S is directly across the terminals defining Z_i. Let us therefore find the impedance Z_i' of Fig. 8.24, which will simply be in parallel with R_S when Z_i is defined.

The network of interest is redrawn as Fig. 8.26. The voltage $V' = -V_{gs}$. Applying Kirchhoff's voltage law around the output perimeter of the network results in

$$V' - V_{r_d} - V_{R_D} = 0$$

and

$$V_{r_d} = V' - V_{R_D} = V' - I'R_D$$

Applying Kirchhoff's current law at node *a* results in

$$I' + g_m V_{gs} = I_{r_d}$$

and

$$I' = I_{r_d} - g_m V_{gs} = \frac{(V' - I'R_D)}{r_d} - g_m V_{gs}$$

or

$$I' = \frac{V'}{r_d} - \frac{I'R_D}{r_d} - g_m[-V']$$

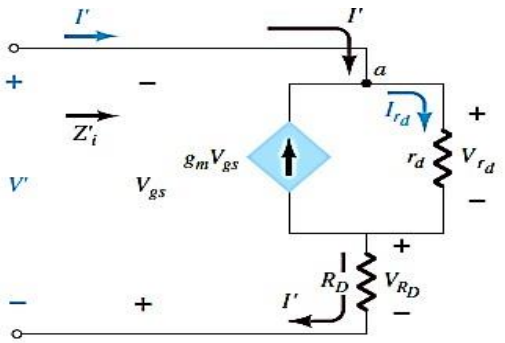

FIG. 8.26
Determining Z_i' for the network of Fig. 8.24.

so that
$$I'\left[1 + \frac{R_D}{r_d}\right] = V'\left[\frac{1}{r_d} + g_m\right]$$

and
$$\boxed{Z_i' = \frac{V'}{I'} = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]}} \qquad (8.33)$$

or
$$Z_i' = \frac{V'}{I'} = \frac{r_d + R_D}{1 + g_m r_d}$$

and
$$Z_i = R_S \| Z_i'$$

which results in
$$\boxed{Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right]} \qquad (8.34)$$

If $r_d \geq 10R_D$, Eq. (8.33) permits the following approximation since $R_D/r_d \ll 1$ and $1/r_d \ll g_m$:

Z_o Substituting $V_i = 0$ V in Fig. 8.25 will "short-out" the effects of R_S and set V_{gs} to 0 V. The result is $g_m V_{gs} = 0$, and r_d will be in parallel with R_D. Therefore,

$$\boxed{Z_o = R_D \| r_d} \qquad (8.36)$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \qquad (8.37)$$

A_v Figure 8.25 reveals that

$$V_i = -V_{gs}$$

and
$$V_o = I_D R_D$$

The voltage across r_d is

$$V_{r_d} = V_o - V_i$$

Applying Kirchhoff's current law at node b in Fig. 8.25 results in

$$I_{r_d} + I_D + g_m V_{gs} = 0$$

and

$$I_D = -I_{r_d} - g_m V_{gs}$$

$$= -\left[\frac{V_o - V_i}{r_d}\right] - g_m[-V_i]$$

$$I_D = \frac{V_i - V_o}{r_d} + g_m V_i$$

so that

$$V_o = I_D R_D = \left[\frac{V_i - V_o}{r_d} + g_m V_i\right] R_D$$

$$= \frac{V_i R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m$$

and

$$V_o\left[1 + \frac{R_D}{r_d}\right] = V_i\left[\frac{R_D}{r_d} + g_m R_D\right]$$

with

$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]} \qquad \textbf{(8.38)}$$

For $r_d \geq 10R_D$, the factor R_D/r_d of Eq. (8.38) can be dropped as a good approximation, and

$$A_v \cong g_m R_D \quad {}_{r_d \geq 10R_D} \qquad \textbf{(8.39)}$$

EXAMPLE 8.9 Although the network of Fig. 8.27 may not initially appear to be of the common-gate variety, a close examination will reveal that it has all the characteristics of Fig. 8.24. If $V_{GS_Q} = -2.2$ V and $I_{D_Q} = 2.03$ mA:

a. Determine g_m.
b. Find r_d.
c. Calculate Z_i with and without r_d. Compare results.
d. Find Z_o with and without r_d. Compare results.
e. Determine V_o with and without r_d. Compare results.

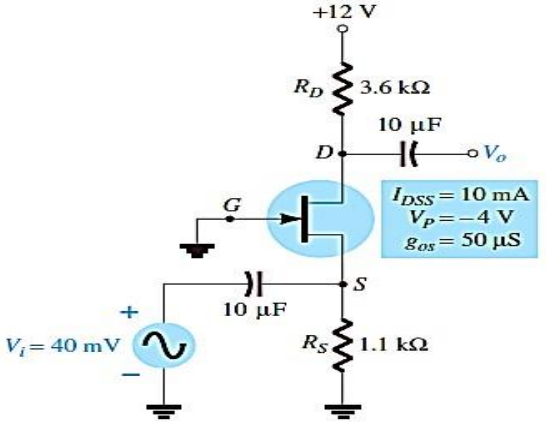

FIG. 8.27
Network for Example 8.9.

ENHANCEMENT-TYPE MOSFETs

The enhancement-type MOSFET (E-MOSFET) can be either an n-channel (nMOS) or p-channel (pMOS) device, as shown in Fig. 8.36. The ac small-signal equivalent circuit of either device is shown in Fig. 8.36, revealing an open-circuit between gate and drain–source channel and a current source from drain to source having a magnitude dependent on the gate-to-source voltage. There is an output impedance from drain to source, rd, which is usually provided on specification sheets as a conductance, gos, or admittance, yos. The device transconductance gm is provided on specification sheets as the forward transfer admittance y_{fs}.In our analysis of JFETs, an equation for gm was derived from Shockley's equation. For E-MOSFETs, the relationship between output current and controlling voltage is defined by:

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

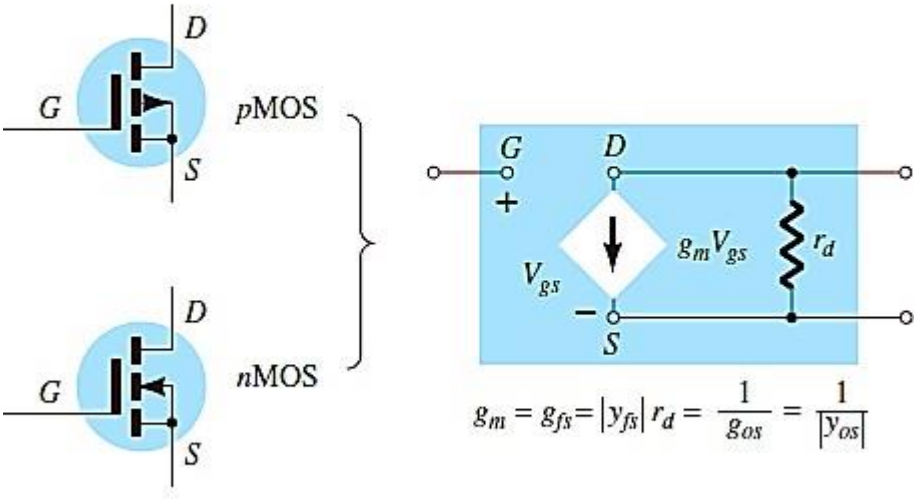

FIG. 8.36
Enhancement MOSFET ac small-signal model.

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Since g_m is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine g_m as an operating point. That is,

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

and

$$\boxed{g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})} \qquad (8.45)$$

Recall that the constant k can be determined from a given typical operating point on a specification sheet. In every other respect, the ac analysis is the same as that employed for JFETs or D-MOSFETs. Be aware, however, that the characteristics of an E-MOSFET are such that the biasing arrangements are somewhat limited.

E-MOSFET DRAIN-FEEDBACK CONFIGURATION

The E-MOSFET drain-feedback configuration appears in Fig. 8.37. Recall from dc calculations that R_G could be replaced by a short-circuit equivalent since $I_G = 0$ A and therefore

$$V_{R_G} = 0\,\text{V}.$$

However, for ac situations, it provides an important high impedance between V_o and V_i. Otherwise, the input and output terminals would be connected directly and $V_o = V_i$.

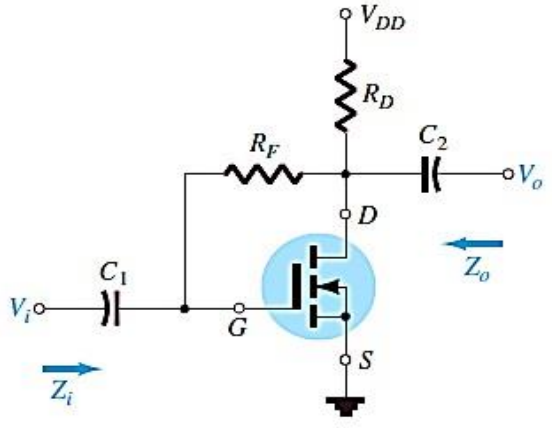

FIG. 8.37
E-MOSFET drain-feedback configuration.

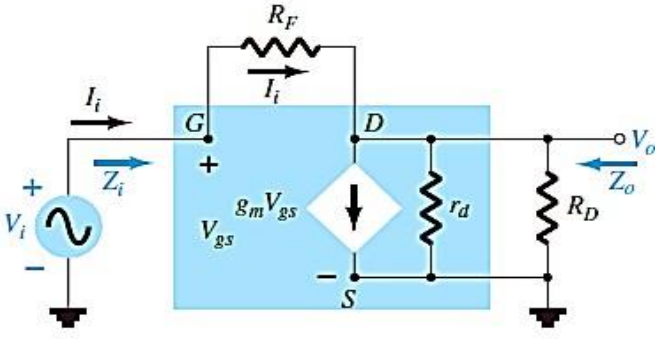

FIG. 8.38
AC equivalent of the network of Fig. 8.37.

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Substituting the ac equivalent model for the device results in the network of Fig. 8.38.

Note that R_F is not within the shaded area defining the equivalent model of the device, but does provide a direct connection between input and output circuits.

Z_i Applying Kirchhoff's current law to the output circuit (at node D in Fig. 8.38) results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

and $$V_{gs} = V_i$$

so that $$I_i = g_m V_i + \frac{V_o}{r_d \| R_D}$$

or $$I_i - g_m V_i = \frac{V_o}{r_d \| R_D}$$

Therefore, $$V_o = (r_d \| R_D)(I_i - g_m V_i)$$

with $$I_i = \frac{V_i - V_o}{R_F} = \frac{V_i - (r_d \| R_D)(I_i - g_m V_i)}{R_F}$$

and $$I_i R_F = V_i - (r_d \| R_D) I_i + (r_d \| R_D) g_m V_i$$

so that $$V_i[1 + g_m(r_d \| R_D)] = I_i[R_F + r_d \| R_D]$$

and finally,

$$\boxed{Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}} \qquad (8.46)$$

Typically, $R_F \gg r_d \| R_D$, so that

$$Z_i \cong \frac{R_F}{1 + g_m(r_d \| R_D)}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_i \cong \frac{R_F}{1 + g_m R_D}} \qquad (8.47)$$

$R_F \gg r_d \| R_D,\ r_d \geq 10R_D$

Z_o Substituting $V_i = 0$ V results in $V_{gs} = 0$ V and $g_m V_{gs} = 0$, with a short-circuit path from gate to ground as shown in Fig. 8.39. R_F, r_d, and R_D are then in parallel and

$$\boxed{Z_o = R_F \| r_d \| R_D} \qquad (8.48)$$

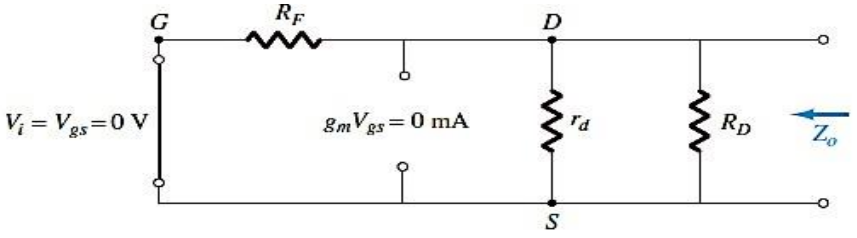

FIG. 8.39
Determining Z_o for the network of Fig. 8.37.

Normally, R_F is so much larger than $r_d \| R_D$ that

$$Z_o \cong r_d \| R_D$$

and with $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D} \quad R_F \gg r_d \| R_D,\ r_d \geq 10R_D \tag{8.49}$$

A_v Applying Kirchhoff's current law at node D of Fig. 8.38 results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

but $V_{gs} = V_i$ and $I_i = \dfrac{V_i - V_o}{R_F}$

so that $$\frac{V_i - V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

and $$\frac{V_i}{R_F} - \frac{V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

so that $$V_o\left[\frac{1}{r_d \| R_D} + \frac{1}{R_F}\right] = V_i\left[\frac{1}{R_F} - g_m\right]$$

and $$A_v = \frac{V_o}{V_i} = \frac{\left[\dfrac{1}{R_F} - g_m\right]}{\left[\dfrac{1}{r_d \| R_D} + \dfrac{1}{R_F}\right]}$$

but $$\frac{1}{r_d \| R_D} + \frac{1}{R_F} = \frac{1}{R_F \| r_d \| R_D}$$

and $$g_m \gg \frac{1}{R_F}$$

so that $$\boxed{A_v = -g_m(R_F \| r_d \| R_D)} \tag{8.50}$$

Since R_F is usually $\gg r_d \| R_D$ and if $r_d \geq 10R_D$,

$$\boxed{A_v \cong -g_m R_D} \quad R_F \gg r_d \| R_D,\ r_d \geq 10R_D \tag{8.51}$$

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EXAMPLE 8.12 The E-MOSFET of Fig. 8.40 was analyzed in Example 7.10, with the result that $k = 0.24 \times 10^{-3}$ A/V^2, $V_{GS_Q} = 6.4$ V, and $I_{D_Q} = 2.75$ mA.

a. Determine g_m.
b. Find r_d.
c. Calculate Z_i with and without r_d. Compare results.
d. Find Z_o with and without r_d. Compare results.
e. Find A_v with and without r_d. Compare results.

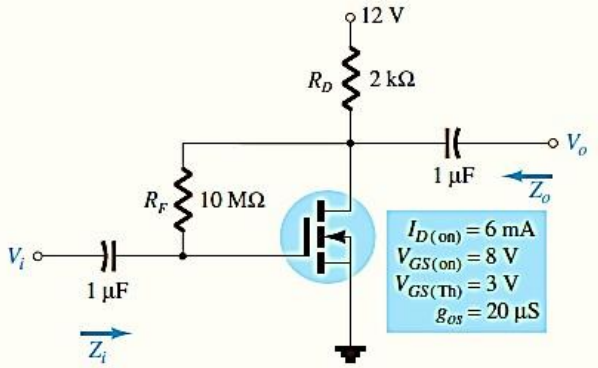

FIG. 8.40
Drain-feedback amplifier from Example 8.11.

Solution:

a. $g_m = 2k(V_{GS_Q} - V_{GS(Th)}) = 2(0.24 \times 10^{-3}\ \text{A/V}^2)(6.4\ \text{V} - 3\ \text{V})$
$= \mathbf{1.63\ mS}$

b. $r_d = \dfrac{1}{g_{os}} = \dfrac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$

c. With r_d,

$$Z_i = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)} = \frac{10\ \text{M}\Omega + 50\ \text{k}\Omega \| 2\ \text{k}\Omega}{1 + (1.63\ \text{mS})(50\ \text{k}\Omega \| 2\ \text{k}\Omega)}$$
$$= \frac{10\ \text{M}\Omega + 1.92\ \text{k}\Omega}{1 + 3.13} = \mathbf{2.42\ M\Omega}$$

Without r_d,

$$Z_i \cong \frac{R_F}{1 + g_m R_D} = \frac{10\ \text{M}\Omega}{1 + (1.63\ \text{mS})(2\ \text{k}\Omega)} = \mathbf{2.53\ M\Omega}$$

which shows that since the condition $r_d \geq 10R_D = 50\ \text{k}\Omega \geq 40\ \text{k}\Omega$ is satisfied, the results for Z_o with or without r_d will be quite close.

d. With r_d,

$$Z_o = R_F \| r_d \| R_D = 10\ \text{M}\Omega \| 50\ \text{k}\Omega \| 2\ \text{k}\Omega = 49.75\ \text{k}\Omega \| 2\ \text{k}\Omega$$
$$= \mathbf{1.92\ k\Omega}$$

E-MOSFET VOLTAGE-DIVIDER CONFIGURATION

The last E-MOSFET configuration to be examined in detail is the voltage-divider network of Fig. 8.41. The format is exactly the same as appearing in a number of earlier discussions.

Substituting the ac equivalent network for the E-MOSFET results in the configuration of Fig. 8.42, which is exactly the same as Fig. 8.23. The result is that Eqs. (8.28) through (8.32) are applicable, as listed below for the E-MOSFET.

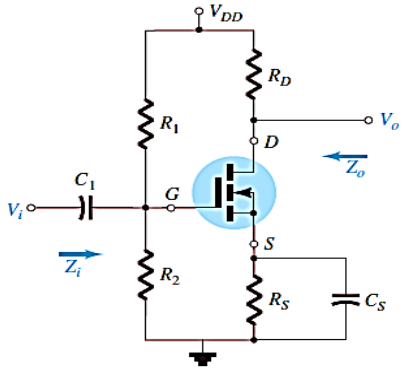

FIG. 8.41
E-MOSFET voltage-divider configuration.

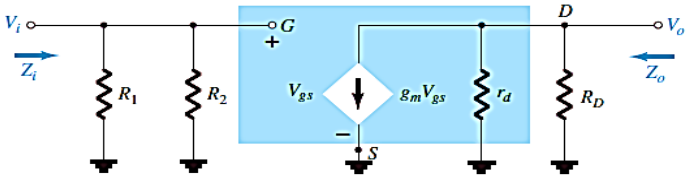

FIG. 8.42
AC equivalent network for the configuration of Fig. 8.41.

Z_i

$$Z_i = R_1 \| R_2 \tag{8.52}$$

Z_o

$$Z_o = r_d \| R_D \tag{8.53}$$

For $r_d \geq 10R_D$,

$$Z_o \cong R_d \quad r_d \geq 10R_D \tag{8.54}$$

A_v

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \tag{8.55}$$

and if $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \tag{8.56}$$

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