

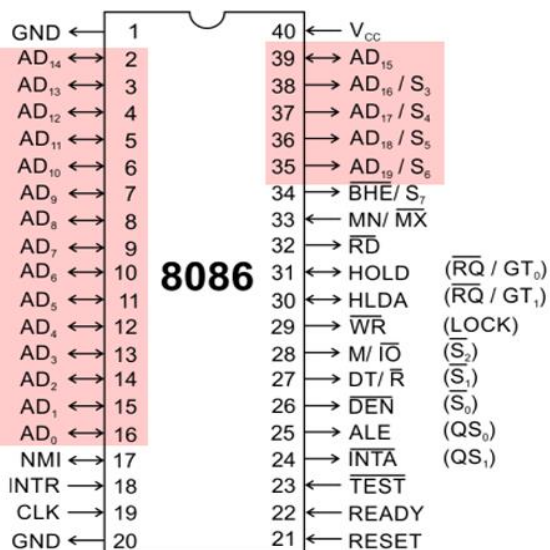


Al-Mustaqbal University / College of Engineering & Technology  
Department of Electrical Engineering Techniques Class (3)  
Subject (microprocessor) / Code (رمز المادة)  
Lecturer (م.م أسماء ضياء سعيد)  
1<sup>st</sup> term –lab Lecture 1. & (Identify various pins of the given Microprocessor)

Lab 1: Identify various pins of the given Microprocessor.

8086 Microprocessor

Microprocessor Pin



AD<sub>0</sub>-AD<sub>15</sub> (Bidirectional)

Address/Data bus

Low order address bus; these are multiplexed with data.

When AD lines are used to transmit memory address the symbol A is used instead of AD, for example A<sub>0</sub>-A<sub>15</sub>.

When data are transmitted over AD lines the symbol D is used in place of AD, for example D<sub>0</sub>-D<sub>7</sub>, D<sub>8</sub>-D<sub>15</sub> or D<sub>0</sub>-D<sub>15</sub>.

A<sub>16</sub>/S<sub>3</sub>, A<sub>17</sub>/S<sub>4</sub>, A<sub>18</sub>/S<sub>5</sub>, A<sub>19</sub>/S<sub>6</sub>

High order address bus. These are multiplexed with status signals



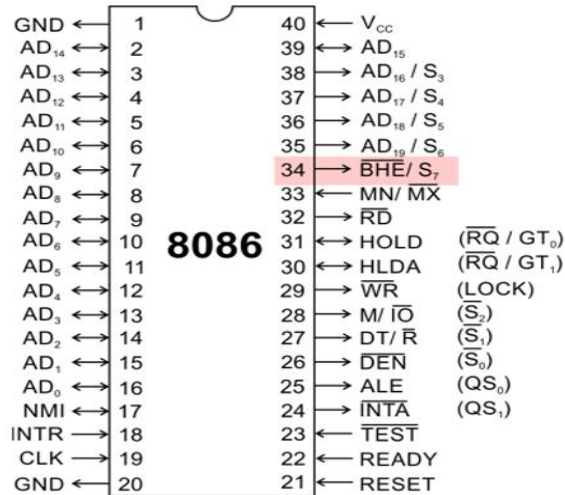
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### BHE (Active Low)/S<sub>7</sub> (Output)

#### Bus High Enable/Status

It is used to enable data onto the most significant half of data bus, D<sub>8</sub>-D<sub>15</sub>. 8-bit device connected to upper half of the data bus use BHE (Active Low) signal. It is multiplexed with status signal S<sub>7</sub>.

### MN/ MX

#### MINIMUM / MAXIMUM

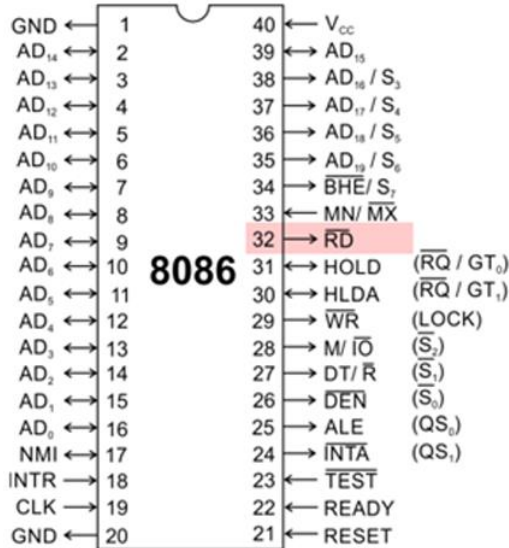
This pin signal indicates what mode the processor is to operate in.

### RD (Read) (Active Low)

The signal is used for read operation.  
It is an output signal.  
It is active when low.



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### TEST

$\overline{TEST}$  input is tested by the 'WAIT' instruction.

8086 will enter a wait state after execution of the WAIT instruction and will resume execution only when the  $\overline{TEST}$  is made low by an active hardware.

This is used to synchronize an external activity to the processor internal operation.

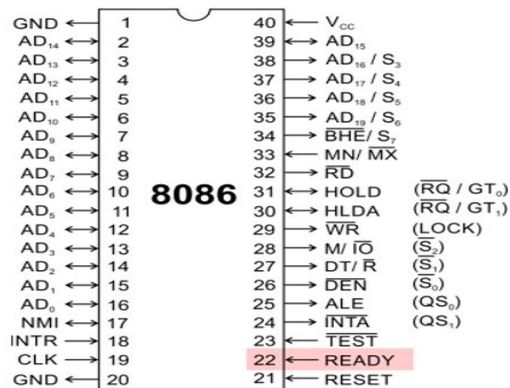
### READY

This is the acknowledgement from the slow device or memory that they have completed the data transfer.

The signal made available by the devices is synchronized by the 8284A clock generator to provide ready input to the 8086.

The signal is active high.

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### RESET (Input)

Causes the processor to immediately terminate its present activity.

The signal must be active HIGH for at least four clock cycles.

### CLK

The clock input provides the basic timing for processor operation and bus control activity. Its an asymmetric square wave with 33% duty cycle.

### INTR Interrupt Request

This is a triggered input. This is sampled during the last clock cycles of each instruction to determine the availability of the request. If any interrupt request is pending, the processor enters the interrupt acknowledge cycle.

This signal is active high and internally synchronized.